

# Study of Influence of Channel Length Variation in Nano Range on Power and Delay of 3T DRAM Cell

Saradindu Panda<sup>1</sup>, B.Maji<sup>2</sup>, Dr.A.K.Mukhopadhyay<sup>3</sup>

<sup>1</sup>Dept. of Electronics and Communication Engineering, Narula Institute of Technology, Kolkata, India

<sup>2</sup>Dept. of Electronics and Communication Engineering, NIT, Durgapur, India.

<sup>3</sup>Director, BITM, Santiniketan, Birbhum. West Bengal, India

Email: [saradindupanda@gmail.com](mailto:saradindupanda@gmail.com)<sup>1</sup>, [bmajiecenit@yahoo.com](mailto:bmajiecenit@yahoo.com)<sup>2</sup>, [askm55@gmail.com](mailto:askm55@gmail.com)<sup>3</sup>

**Abstract:** This paper describes the design issues of DRAM, simulation of 3T DRAM cell, and measurement of its power and delay, for various channel length. Varying the parameters such as channel length, we observe different results being reflected in its power and delay which is described in this paper. Waveforms are plotted as per our observations.

**Keywords:** 3T DRAM, Power, Delay, Channel Length.

## I. INTRODUCTION

THE ever increasing demand for reliable electronic equipment of smaller size and low power requirement in communication, computers and aerospace industries has led to the growth of circuit microminiaturization. Semiconductor memory is an electronic device to store the data, often used as the memory of computer, implemented on a semiconductor based integrated circuit. A three transistor DRAM cell consist of column pull up (pre-charge) transistors and the column read/write circuitry. Here the binary information is stored in the form of charge in the parasitic node capacitance C1. The storage transistor M2 is turned on or off depending on the charge stored in C1, and the pass transistors M1 and M3 act as access switches for data read and write operations. The cell has two separate bit lines data read and data write, and two separate word line to control the access transistors. A simplified 3T DRAM Cell is shown in Fig 1.

## II. OPERATING PRINCIPLES OF 3T DRAM CELL

The operation of the 3T dram cell and its peripheral circuitry is based on a two phase non-overlapping clock scheme. Every data read and data write operation is preceded by a pre charge cycle, which is initiated with the pre charge signal PC going high. During the pre charge cycle the column pull transistors are activated and the corresponding column capacitances are charged up to logic –high level.

All data read and write operations are performed during the active phase i.e. when PC is low.

For the write one operation the inverse data input is at the logic-low level, because the data to be written onto the DRAM cell is logic “1”. Consequently, the “data write” transistor MD is turned off, and the voltage level on column Din remains high.

Now, the “write select” signal Ws is pulled high during the active phase. As a result, the write access transistor M1 turned on. With M1 on, the charge on C2 is now shared with C1. Since the capacitance C2 is very large compared to C1, the storage node capacitance C1 attains approximately the same logic –high level as the column capacitance C2 at the end of the charge –sharing process.

After the write “1” operation is completed, the write access transistor M1 is turned off. With the storage capacitance C1 charged up to a logic –high level, the transistor M2 is now conducting. In order to read this “1”, the “read select” signal RS must be pulled up, following a pre charge cycle. As the read access transistor M3 turns on, M2 and M3 create a conducting path between

the “read data” column capacitance C3 and the ground. The capacitance C3 discharges through M2 and M3, and the falling column voltage is interpreted by the “data read” circuitry as stored logic “1”.

For the write “0” operation the inverse data input is at the logic-high level, because the data to be written into DRAM cell is logic “0”. Consequently, the data write transistor is turned on, and the voltage level on column Din is pulled to logic 0. Now the write select signal WS is pulled high. As a result, the write access transistor M1 is turned on. The voltage level on C2, as well as the write access transistor M1 is turned on. The voltage level on C2, as well as that on the storage node C1, is pulled to logic “0” through M1 and the data write transistor. Thus at end of the write “0” sequence, the storage capacitor C1, contains a very low charge, and the transistor M2 is turned off since its gate voltage is approximately equal to “0”.

In order to read this stored zero the “read select” signal RS must be pulled high, following a pre charge cycle. The read access transistor M3 turns on, but since M2 is off, there is no conduction path between C3 and ground. Consequently, C3 doesn’t discharge, and the logic –high level on the Dout column is interpreted by the data read circuitry as a stored “0” bit.

### III. MEASUREMENT OF POWER AND DELAY OF 3T DRAM CELL USING NMOS WITH DIFFERENT CHANNEL LENGTH IN READ AND WRITE OPERATION

#### A. Delay for ‘WRITE-1’ operation

During write-1 operation as there is only one transistor operating while writing ‘one’ into the cell, so delay is less.

#### B. Delay for ‘READ-1’ operation

During read-1 operation as there are two transistors operating while reading one from the cell, so delay is more compare to write one operation.

Comparative Power and Delay analysis with Different Channel length MOSFET with different Vdd is described in Table I:

TABLE I  
COMPARATIVE DELAY AND POWER ANALYSIS FOR ‘READ 1’ AND ‘WRITE 1’ OPERATION WITH DIFFERENT CHANNEL LENGTH OF MOSFET AND VDD

Channel Length (nm)	Operation	Vdd (volt)	Power(watt)	Delay(sec)
L=150nm	READ 1	0.6	1.73E-09	2.97E-06
		0.7	1.90E-09	2.28E-06
		0.8	2.49E-09	1.67E-06
		0.9	3.06E-09	1.16E-06
		1	3.69E-09	7.05E-07
	WRITE 1	0.6	3.37E-09	3.93E-12
		0.7	4.31E-09	3.77E-12
		0.8	5.36E-09	3.44E-12
		0.9	6.51E-09	2.94E-12
		1	7.77E-09	2.21E-12
L=175nm	READ 1	0.6	2.70E-09	4.52E-11
		0.7	3.73E-09	3.57E-11
		0.8	4.90E-09	2.59E-11
		0.9	6.21E-09	2.13E-11
		1	7.67E-09	1.80E-11
	WRITE 1	0.6	7.69E-07	4.46E-12
		0.7	1.23E-06	3.99E-12
		0.8	1.87E-06	3.55E-12
		0.9	2.12E-06	3.05E-12
		1	2.54E-06	2.85E-12
L=150nm	READ 1	0.6	7.63E-07	2.20E-08
		0.7	1.33E-06	8.75E-09
		0.8	1.88E-06	5.16E-09
		0.9	2.52E-06	3.80E-09
		1	3.09E-06	3.22E-09
	WRITE 1	0.5	2.39E-07	2.29E-11
		0.6	7.62E-07	3.77E-11
		0.7	1.33E-06	3.95E-11
		0.8	1.88E-06	3.92E-11
		0.9	2.52E-06	3.94E-11
		1	3.25E-06	3.88E-11

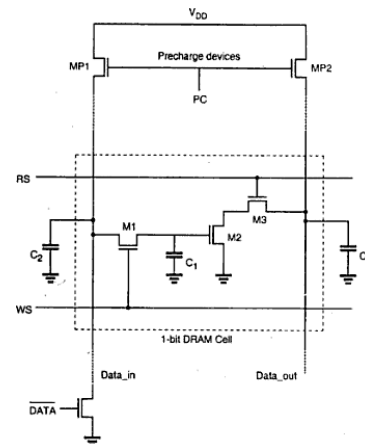


Fig. 1. Three- transistor DRAM cell with the pull-up and read/write circuitry.

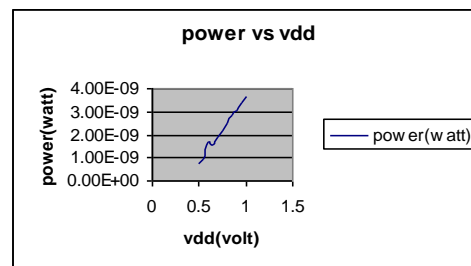


Fig.2. Power with varying Vdd when L=250nm for READ 1 Operation.

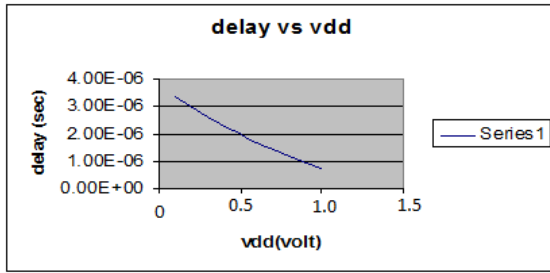


Fig.3. Delay with varying Vdd when L=250nm for READ 1 Operation.

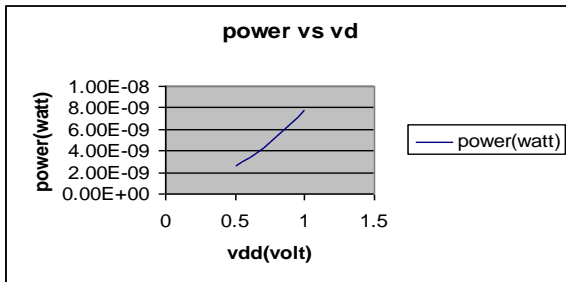


Fig.4. Power with varying Vdd when L=250nm for WRITE 1 Operation.

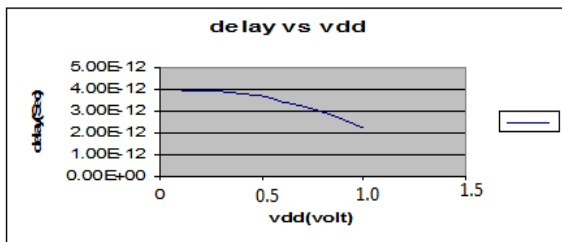


Fig.5. Delay with varying Vdd when L=250nm for WRITE 1 Operation.

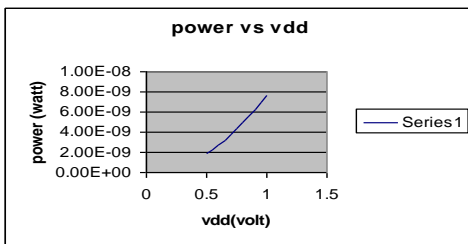


Fig.6. Power with varying Vdd when L=175nm for READ 1 Operation.

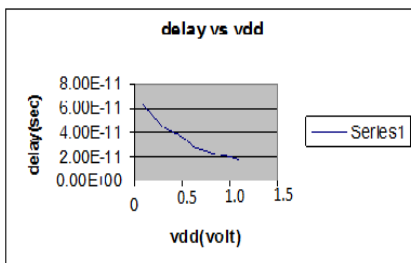


Fig.7. Delay with varying Vdd when L=175nm for READ 1 Operation.

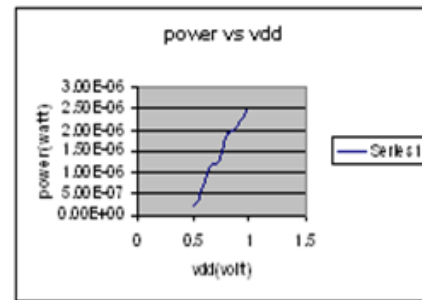


Fig.8. Power with varying Vdd when L=175nm for WRITE 1 Operation.

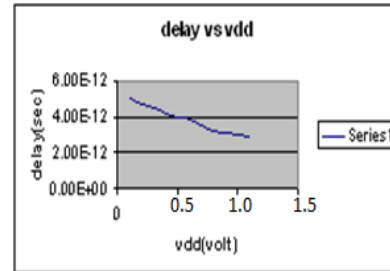


Fig.9. Delay with varying Vdd when L=175nm for WRITE 1 Operation.

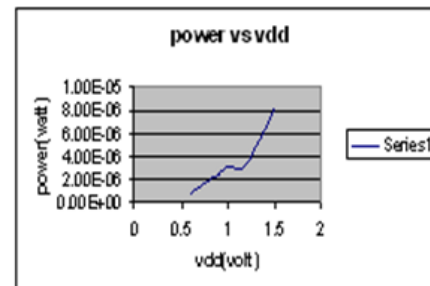


Fig.10. Power with varying Vdd when L=150nm for READ 1 Operation.

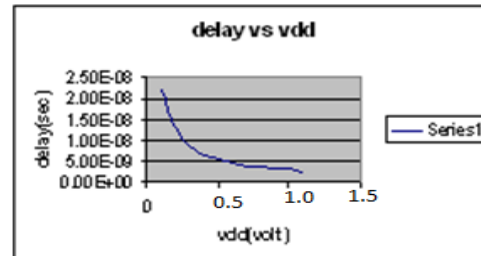


Fig.11. Delay with varying Vdd when L=150nm for READ 1 Operation.

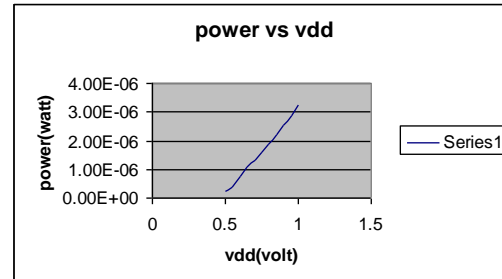


Fig.12. Power with varying Vdd when L=150nm for WRITE 1 Operation.

#### IV. RESULT ANALYSIS

In this paper, we described the simulated result of 3T DRAM cell, and from the results which we have given in TABLE I, we have observed that: During WRITE-1 operation as there is only one transistor operating while writing 'one' into the cell, so delay is less. During READ-1 operation as there are two transistors operating while reading 'one' from the cell, so delay is more compare to write one operation. We also observed that when we have varied Vdd from 1 volt to 0.5 volt, the power gradually decreased, and the delay is gradually increased. As we have varied the channel length from 250nm to 150nm, the power has decreased.

#### V. CONCLUSION

In our work we have varied values of VDD from 1 volt to 0.5 volt. At the same time we have observed the power and delay output for channel lengths 250nm, 175nm, and 150nm with varying VDD. During this work we have observed that power consumption gradually decreases with decreasing values of VDD. Even power consumption decreases with decreasing channel length values. But delay increases with decreasing VDD values. Now while designing a circuit we have to keep in mind that power consumption, delay and cost should be minimum. From the theory, it is clear that power consumption and delay of DRAM cell is not only dependent on VDD but also on load capacitance (Cload), threshold voltage (Vth), and oxide thickness. Therefore for better performance of the device in nano range optimization is needed.

#### ACKNOWLEDGMENT

The authors would like to thank Prof. (Dr.) M.R.Kanjilal and Faculty Members, Department of Electronics and Communication Engineering, Narula Institute of Technology, WBUT, for many insightful discussions.

#### REFERENCES

- [1] Sung-Mo Kang, Yusuf Leblebici, "Cmos Digital Integrated Circuits", 3<sup>rd</sup> ed., Page-415.
- [2] J. M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits, 2nd ed. Copyright 2003 Prentice Hall/Pearson.
- [3] Ki Chul Chun, Jain, P.; Jung Hwa Lee; Kim, C.H. "A 3T Gain Cell Embedded DRAM Utilizing Preferential Boosting for High Density and Low Power On-Die Caches", Solid-State Circuits, IEEE, Volume:46 Issue:6, Page(s): 1495 – 1505.
- [4] Xiaoyao Liang, Ramon Canal, Gu-Yeon Wei, David Brooks, "REPLACING 6T SRAMS WITH 3T 1D DRAMS IN THE L1 DATA CACHE TO COMBAT PROCESS VARIABILITY", Published by the IEEE Computer Society, 2008, Page No-60-68.
- [5] W.K. Luk et al., "A 3-Transistor DRAM Cell with Gated Diode for Enhanced Speed and Retention Time," Proc. Symp. VLSI Circuits, IEEE Press, 2006, pp. 184-185.
- [6] A.J. Bhavnagarwala, X. Tang, and J.D. Meindl, "The Impact of Intrinsic Device Fluctuations on CMOS SRAM Cell Stability," IEEE J. Solid-State Circuits, vol. 36, no. 4, Apr. 2001, pp. 658-665.

#### Biography

##### **Saradindu Panda**

He received M.Tech from Jadavpur University in 2007 in VLSI Design and Microelectronics Technology. He is pursuing his PhD at NIT, Durgapur, West Bengal, India. Presently, he is involved in design and management of low-power and high speed integrated circuits with Solid State Devices in Nano Regime. He is now faculty in ECE Department at Narula Institute of Technology, Kolkata, India. He has 7 years teaching experience. He is author and Co-author of more than 15 publications in different International and National Journals and Conference Proceedings.

##### **Prof. (Dr.) Bansibadan Maji**

He is now a senior Professor of ECE Department in NIT, Durgapur, West Bengal, India. He is now Head of The Department of ECE at NIT. His main research area on Microwave, Antenna, VLSI Design and Low power Device and Circuits. He is author and Co-author of more than 50 publications in different International and National Journals and Conference Proceedings.

##### **Prof.(Dr.) A. K. Mukhopadhyay**

He received M.Tech from IIT, Kharagpur, and Ph.D(Engg) from Jadavpur University, India. Currently, he is the Director of BITM, Santiniketan, Birbhum, West Bengal, India. He was the Principal of BCET, Durgapur. Previously he served as the Dean (Academic) and Head of Department of ECE, Dr. B. C. Roy Engineering College, Durgapur. He also worked at Narula Institute of Technology, Kolkata, College of Engineering & Management, Kolaghat, NERIST, Itanagar and IIT, Kharagpur. His current area of research includes Wireless and Mobile Networks and Overlay-based heterogeneous networks. He has 43 publications mostly in international journal and conference proceedings. He is a Life Fellow of the Institution of Engineers (I), Member, IEEE, Member, IEEE ComSoc, Global Member, ISOC; Sr. Life Member, CSI; Life Member, ISTE, IETE, SSI etc.