Design and Implement Low Power in Different type of Adders

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ABSTRACT: In this paper 1-bit adder has been designed and simulated using 180 nm CMOS technology in tanner tool at a various supply voltage from 1.0V to 1.8 V & compare their results with respect to various parameters like delay, area & power consumption. The adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance and power optimization is of utmost importance. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly.

Due to continuous scaling of the transistor size and reduction of the operating voltage has led to a significant performance improvement of integrated circuits. Low power consumption and smaller area are some of the most important criteria for the fabrication of DSP systems and high performance systems. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip.

I. INTRODUCTION

Rapid growth in semiconductor technology has led to shrinking of feature sizes of transistors using deep submicron (DSM) process. Modern portable battery operated devices such as cell phones, laptops; PDAs are particularly affected by this as high power dissipation reduces battery service life. The adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance and power optimization is of utmost importance. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip. Therefore, in realizing modern Very Large Scale Integration (VLSI) circuits, low-power and high-speed are the two predominant factors which need to be considered. Like any other circuits' design, the design of high-performance and low-power adders can be addressed at different levels, such as architecture, logic style, layout, and the process technology. As the result, there always exists a trade-off between the design parameters such as speed, power consumption, and area. Recently, the requirement of probability and the moderate improvement in battery performance indicate power dissipation is one of the most critical design parameters day by day the demand of probability and mobility is increasing.

Adders are commonly used in the critical path of many building blocks of microprocessors and digital signal processing chips. Adders are critical component not only for addition, but also for subtraction, multiplication, and division. Addition is one of the fundamental arithmetic operations. A fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders. The most important parameter for measuring the quality of adder designs is propagation delay, and area.

Adder or summer is a digital circuit that performs addition of numbers. In modern computers adders reside in the arithmetic logic unit (ALU) where other operations are performed. Although adders can be constructed for many numerical representations, such as Binary-coded decimal or excess-3, the most common adders operate on binary numbers.

II. APPLICATION OF ADDERS

- Used in CPU side
- Used in networking side
- Used in DSP oriented system
- In application-specific processors
- In biomedical applications
- In image processing and video processing.

Types of Adder

For single bit adders, there are two general types of adders which are given below

1. Half Adder
2. Full Adder

Carry Look Ahead Adder circuit

A carry-look ahead adder (CLA) is a type of adder used in digital logic that improves speed by reducing the amount of computation time required to determine carry bits. It works by creating two signals P and G known as Carry Propagator signal and Carry Generator signal. The carry propagator signal is propagated to the next level whereas the carry generator is used to generate the output carry, regardless of input carry. Carry signal will be generated in two cases:

1. When both bits A_i and B_i are 1, or

2. When one of the two bits is 1 and the carry-in (carry of the previous stage) is 1.

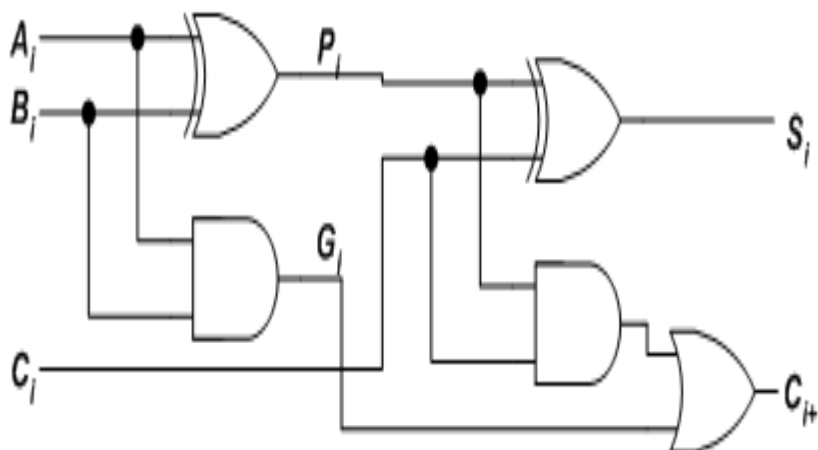Gate level diagram of 1-bit CLA is shown in fig below in fig 3.5.

Fig 1 : Gate Level Diagram of CLA

In this circuit, there are 2 internal signals P_i and G_i which are given

$$P_i = A_i \oplus B_i$$

$$G_i = A_i B_i$$

The output sum and carry can be defined as:

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + P_i C_i$$

G_i is known as the **carry Generate** signal since a carry (C_{i+1}) is generated whenever $G_i = 1$, regardless of the input carry (C_i).

P_i is known as the **carry propagate** signal since whenever $P_i = 1$, the input carry is propagated to the output carry, i.e.

$$C_{i+1} = C_i \ \text{(Whenever } P_i = 1, G_i = 0)$$

The Boolean expression of the carry outputs of various stages can be written as follows:

$C_1 = G_0 + P_0 C_0$

$C_2 = G_1 + P_1 C_1 = G_1 + P_1(G_0 + P_0 C_0) = G_1 + P_1 G_0 + P_1 P_0 C_0$

$C_3 = G_2 + P_2 C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$

$C_4 = G_3 + P_3 C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$

The disadvantage of the CLA adders is that the carry expressions (and hence logic) become quite complex for more than 4 bits.

FULL ADDER TOPOLOGY

In microprocessor and DSP`s, addition is the most commonly used arithmetic operation and it is often one of the speed-limiting elements. Hence optimization of the adder both in terms of speed and/or power consumption should be pursued. During the design of an adder two choices are made in regard to different design abstraction levels. One is responsible for the adder's architecture implemented with the one-bit full adder as a building block. The other defines the specific design style at transistor level to implement the one-bit full adder.

DGTAL ADDER

The fig 2 shows the CMOS transistor level implementation of Modified conventional CMOS full adder design using 20 Transistor model which is the heart of the arithmetic unit. This type of CMOS full adder configuration has been widely used in numerous applications. It often exhibits a critical delay that actually limits the system performance. Two or more full adders are cascaded together to perform multiple bit addition .
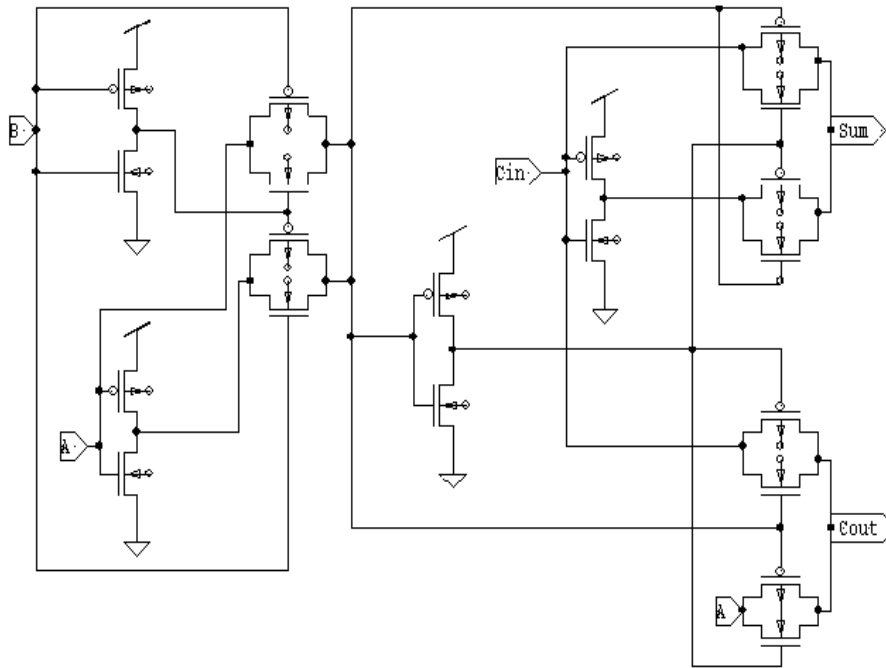
Fig 2: Circuit Diagram of DGTAL Adder

DGTAL ADDER

20 transistor full adder based on transmission gate produces buffered outputs of proper polarity for both sum and carry. In this circuit 2 inverters are followed by two transmission gates which act as 8-T XOR. Subsequently 8-T XNOR module follows. To has 4 transistors XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used generate sum; C in and $\overline{C}_{in}$ are multiplexed which can simultaneously to generate sum. The signals c in is controlled either by (a. b) or (a $\otimes$ b). Similarly the c out can be calculated by multiplexing a and cincontrolled by (a b).The power dissipation in this circuit is more than the 28 transistor. Schematic diagram of DGTAL based adder.
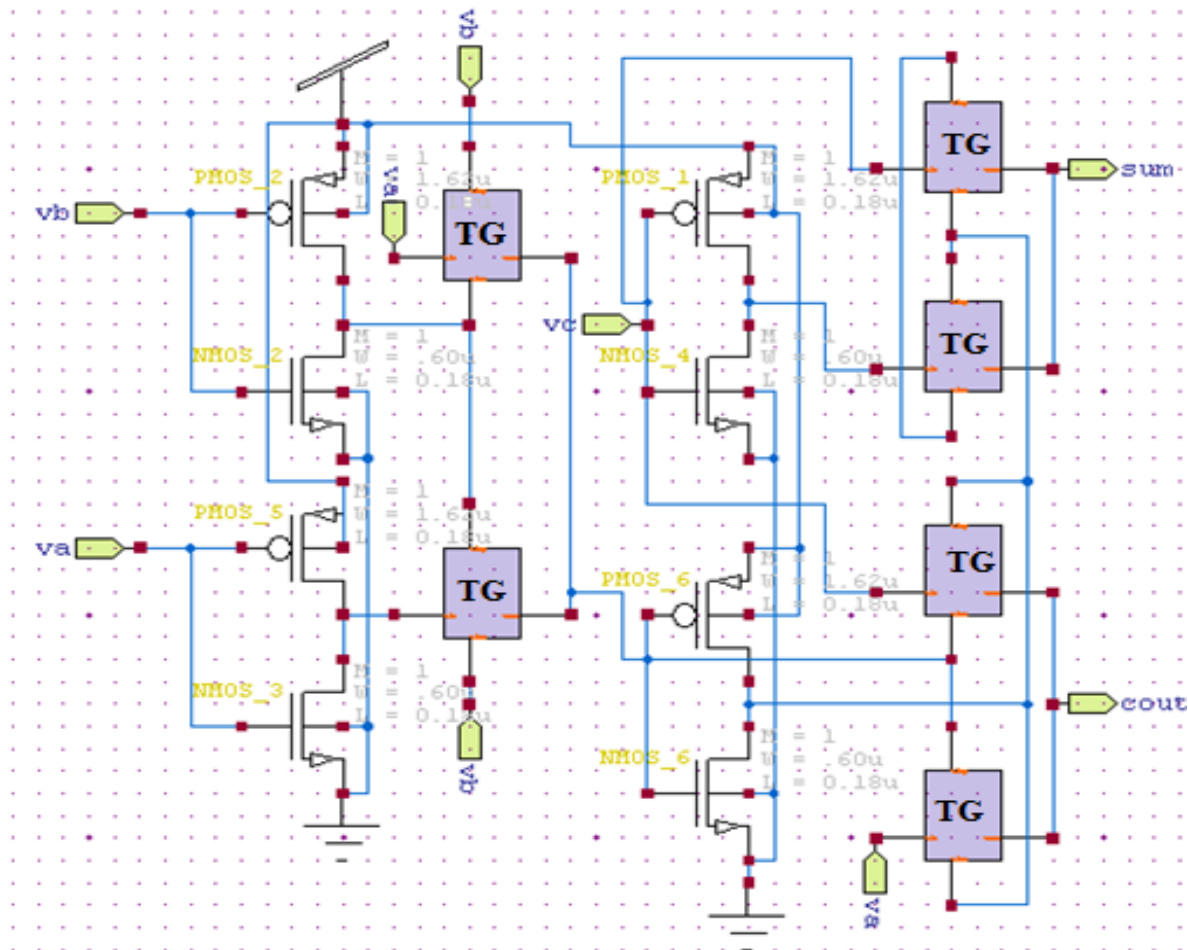
Fig 3: Schematic Diagram of DGTAL Adder

III. SIMULATION RESULTS

DGTAL ADDER

Working principle: In the circuit we have 2 inverters followed by two transmission gates which act as 8-T XOR. Subsequently8-T XNOR module follows. To generate sum, c in and c in b are multiplexed which can controlled either by (a b) or (a $\otimes$ b).Similarly the c out can be calculated by multiplexing a and c in which is controlled by (a b). Simulated waveform of DGTAL full adder is shown in fig 3.
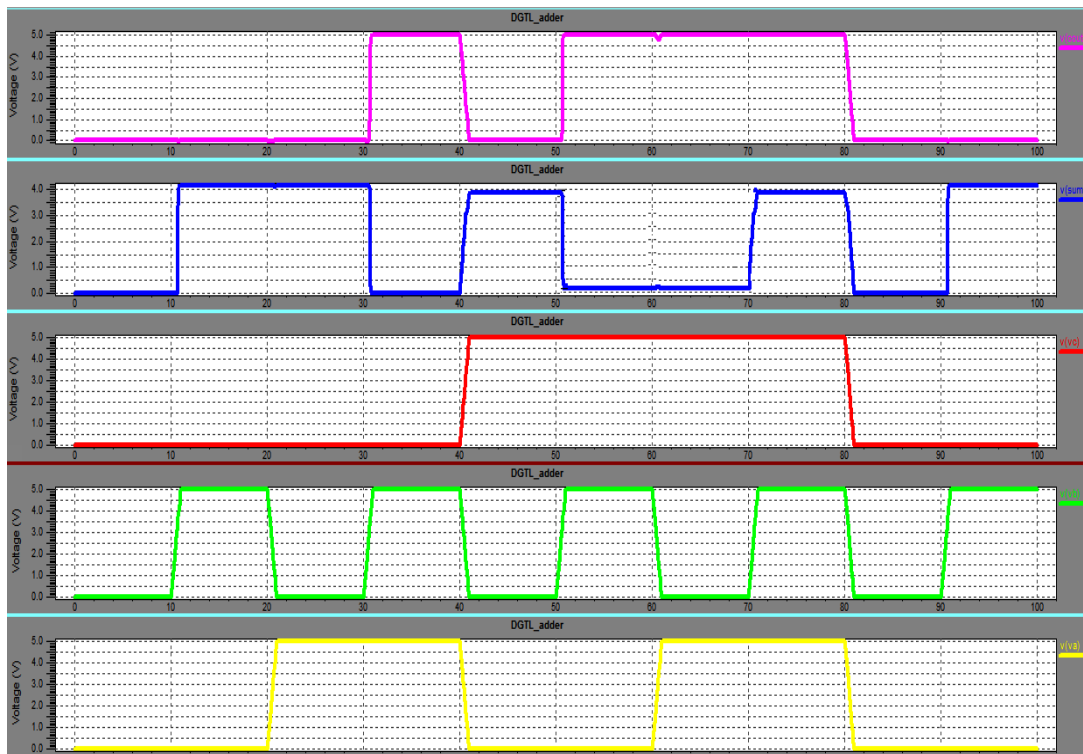
Fig 3: Simulated waveform of DGTAL Adder

Advantage: It is the fastest adder.

The circuit is simpler than the conventional adder.

Disadvantage: The power dissipation in this circuit is more than the 28T adder.

Parameters like delay and power dissipation is calculated at different V_{DD} and at different V_{TH}, which is shown in table 1 and 2 respectively.

Table 2: Parameters of DGTAL adder at different V_{DD}

$V_{DD}(V)$	Power Dissipation (μW)	Delay(nS)	
		Sum	**Cout**
1.8	129.585	4.040	5.211
1.6	109.165	4.948	6.068
1.4	87.255	5.383	6.316
1.2	69.955	6.138	6.968
1.0	40.635	6.954	7.367

Table 2: Parameters of DGTAL adder at different V_{TH}

V_{TH}(V)	Power Dissipation (µW)	Delay(nS)	
		Sum	**Cout**
0.17	66.08	1.8710	5.0996
0.27	95.06	2.1715	5.7000
0.37	129.58	3.5799	6.2117
0.47	147.52	3.9199	6.8693
0.57	179.90	5.6646	7.0703

IV. CONCLUSION

In this paper adder has been designed and simulated using 180 nm CMOS technology of tanner tool at a various supply voltage from 1.0V to 1.8 V& compare their results with respect to various parameter. The comparison has been carried out both assuming circuits with minimum transistors size, to minimize the power consumption. Power consumption is a function of load capacitance, frequency of operation, and supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heat sinks. This provides the consumer with a product that costs less. In this paper we conclude that

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