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Design and Analysis of Boost DC-DC Converter with Interleaved Inductor using MPPT Algorithm

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ABSTRACT: Boost converters are widely used in the low to high dc-dc applications. In the recent years, prominent efforts have been made on improving the performance and efficiency of high power boost converters. In this project, an isolated high step-up dc-dc converter with low voltage stress is explained. The proposed converter achieves extremely high voltage conversion ratio with appropriate duty cycle and reduction of voltage stress on the power devices. The topology utilizes coupled inductor. The leakage inductance energy can be efficiently discharged. Since the device stresses are low in this topology, low voltage MOSFETs with small values of R_{DS} (on) can be selected to reduce the conduction losses. The Perturb and Observe algorithm was implemented for tracking the maximum power from the PV panel. These features improve the converter efficiency and performance. When compared to other topologies the proposed converter contain single switch which simplify the circuit configuration and improves the system reliability. All these factors improve the circuit performance in the high step-up applications.

KEYWORDS: Boost DC-DC Converter, Interleaved Inductor, MPPT Algorithm

I. INTRODUCTION

The mass usage of conventional fossil energy has resulted in reduction of fuel deposit and has affected the atmosphere causing pollution and greenhouse effect. There upraises the problem of energy shortage due to the non-renewable nature of fossil fuel energy. There is a necessity for the development of clean and renewable energy in order to replace conventional fossil energy. Solar energy is promising with its abundance availability and photovoltaic generation, as the utilization method has a large scale applications. Therefore, many methods have been implemented in order to improve the efficiency of the standalone PV system. Due to the non-linear characteristics of the PV panel, the maximum power from the PV panel is tracked by specific control algorithms implemented within the converter known as maximum power point tracking algorithm.

Nowadays, the renewable-energy grid-connected systems with photovoltaic (PV) and fuel cells call for high step-up and high-current DC-DC topologies, because of the low voltage generated by the PV panel and fuel cells should be boosted to a relatively high dc bus voltage for the grid-connected generation systems. For example, in order to deliver the energy to a single-phase 220V utility grid, a 380V DC bus voltage is required with a full-bridge inverter. Unfortunately, the output voltage of most fuel cell stacks or the individual PV cells is lower than 40V due to the safety and reliability issues in the household applications. Large voltage conversion ratio with over ten times of voltage gain is necessary for the front-end DC-DC converters. As a result, non-isolated high-step-up converters are desirable to reduce the system cost and to improve the power density by removing the isolated voltage or current sensors and additional auxiliary power supply in the isolated conversion systems. The converter having an interleaved inductor achieves extremely large voltage conversion ratio with appropriate duty cycle and reduction in voltage stress on the power devices. The leakage inductance energy can be efficiently discharged by using coupled inductor. Since, the device stresses are low in this topology, low voltage MOSFETs with small values of R_{DS}(on) can be selected to reduce the conduction losses. These features improves the converter efficiency. When compared to other topologies the

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proposed converter contain single switch which simplify the circuit configuration and improve the system reliability. All these factors improve the circuit performance in the high step-up applications.

II. METHODOLOGY OF THE PROJECT

There is one coupled inductor with four windings in the converter. For the ease of understanding, it is shown in the figure 2.1 as if there are two cores, $T_1$and T_2. However, in real circuit, all coils are wound on the same core. Each coupled inductor has two windings. Turns ratios of these windings are taken as N_1 and N_2. Primary and secondary inductances of the coupled inductors are indicated as L_1 and L_2. The detailed representation of the modified converter is shown in Fig.2.1. The equivalent model of the coupled inductors includes the magnetizing inductors L_m, the primary leakage inductor L_{lk1}, the summation secondary leakage inductor L_{lk2}.

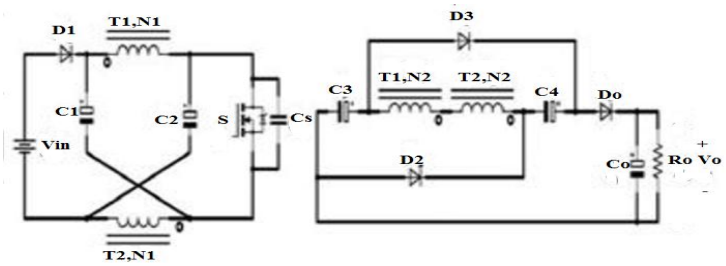

Fig 2.1: Circuit Diagram

The circuit also employs five capacitors (C_0, C_1, C_2, C_3 and C_4), four diodes (D_0, D_1, D_2 and D_3), and a power switch (S). When the power switch is turned ON, the diodes D_1, D_2 and D_3 are OFF while the diode D_o conducts. The capacitors C_1, C_2, C_3 and C_4 are discharged, while the load capacitor C_o is being charged. When the power switch is turned OFF, the diodes D_1, D_2 and D_3 starts conducting and the diode D_0 is OFF. The capacitors C_1, C_2, C_3 and C_4 are charged. While the load capacitor C_o is being discharged. While the primary leakage inductance energy is discharged through the capacitors C_1, C_2 and the diode D_1, the secondary leakage inductance energy is discharged through the load. In the meantime, the switch and the diodes do not experience extra stresses.

Basic operating principle

Before taking up this section, there are some assumptions that are to be made,

1) The turn's ratio of the coupled inductor is low
2) The leakage inductance energy does not create stress on the switches or diodes
3) Switch voltage rating is low
4) Isolation exists between input and output

III. OPERATIONAL ANALYSIS OF DC-DC CONVERTER

Figure 3.1 indicates the step up DC-DC converter system. This system basically consists of Z-source topology with the help of coupled inductors, coils L_1 and L_2 and capacitors C_1 and C_2. These coils are wound on core T_1 and T_2, in practice, all the coils are wound on same core T with turn's ratio N_1:N_2. Coupled inductors provide isolation between input and output as well as it forms resonance tank circuit with capacitor C_1 and C_2 which reduces the stress on switch S. The circuit is controlled by single MOSFET switch S, so the control circuit is simple. The leakage inductance can be recovered by freewheeling diodes D_{f1} and D_{f2}. The D_{in} is used for blocking the reverse voltage at the input side. The load capacitor C_o provides constant voltage to load.

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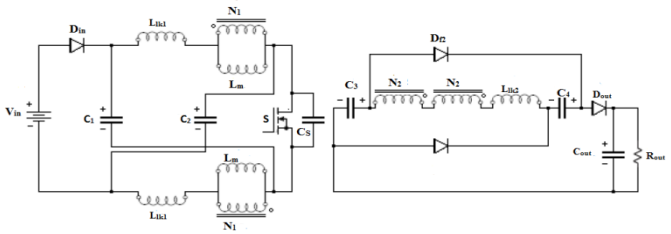

Fig 3.1 High step-up chopper with interleaved inductor

The operational analysis of the proposed DC-DC Converter can be simplified with the help of some assumptions, such as; all devices are ideal, except stray capacitance of MOSFET (C_s). The equivalent model of coupled inductor is represented by magnetizing inductance (L_{m1}= L_{m2}= L_m), leakage inductance (L_{lk1}, L_{lk2}) and an ideal transformer on the basis of cantilever model. Coupling co-efficient ($K_1 = K_2 = K$) and turn's ratio $N_1/N_2 = n$. The values of capacitors (C_o, C_1, C_2, C_3 and C_4) and magnetizing inductance (L_m) are too large for providing constant voltage and current over one switching period.

3.1 Continuous conduction mode (CCM)

In CCM operation, the working of circuit is divided into seven intervals. The Figure 3.2, and Figure 3.3, indicates equivalent circuit for each interval and their waveforms respectively. For CCM operation, assume that the capacitors C_1, C_2, C_3 and C_4 are charged initially.

MODE 1 : Interval [t_0-t_1]: In this interval, switch S is ON at $t=t_0$, the stray capacitance C_s of S is discharged quickly. The Capacitors C_1 and C_2 start discharging through magnetizing inductance L_m and leakage inductance L_{lk1}. The L_m and L_{lk1} are charged by voltage V_c. The currents I_{Lm} and I_{L1} increases linearly. The leakage inductance L_{lk2} discharges its energy through the capacitors C_3 and C_4 along with freewheeling diodes D_{f1} and D_{f2}. The figure 3.2(a), indicates the equivalent circuit for this interval. The load capacitor C_o is discharged through the load. In this interval input diode D_{in} and output diode D_o are off. This interval ends at $t=t_1$ when $I_{Df1} = I_{Df2} = 0$.

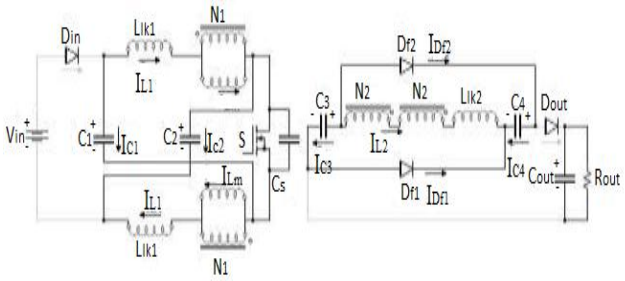

Fig 3.2(a): Operation in Mode 1

MODE 2 : Interval [t_1-t_2]: In this interval, switch S is ON. The capacitors C_1 and C_2 are discharged linearly through magnetizing inductance L_m and leakage inductance L_{lk1}. The currents I_{Lm} and I_{L1} increases linearly. The Fig. 3.2(b), indicates the equivalent circuit for this interval. The capacitors C_3 and C_4 are discharged through D_o, load and C_o. In this interval, D_1, D_{f1}, D_{f2} remains OFF. This interval ends at $t=t_2$ when $V_{l2} = nV_{l1}$.

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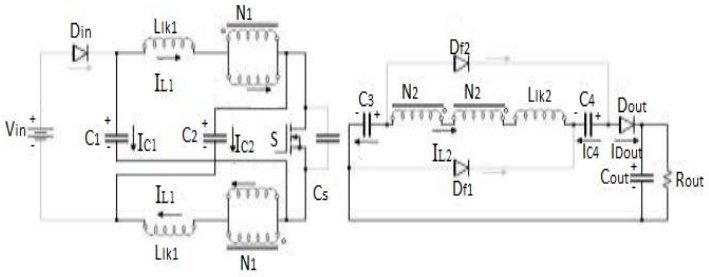

Fig 3.2(b): Operation in Mode 2

MODE 3 : Interval [t_2-t_3]: In this interval, switch S is ON. The diodes D_1, D_{f1}, D_{f2} remains off and diode D_o conduct. All devices are retained in the same states as in interval [t_1-t_2]. The magnetizing inductor L_m transfers the stored energy to secondary side of coupled inductors. These coupled inductors are in series with capacitors C_3 and C_4. They pass energy to load through diode D_o. The Fig.3.2(c), indicates the equivalent circuit for this interval. This interval ends at $t=t_3$ when switch S is turned OFF.

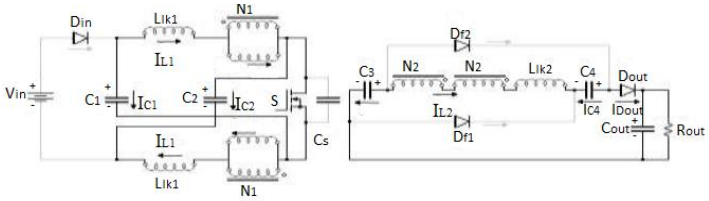

Fig 3.2(c): Operation in Mode 3

MODE 4 : Interval [t_3-t_4]: When switch S is OFF, the stray capacitor Cs charge quickly. All other devices keep their state as in interval [t_2-t_3]. This interval ends at $t=t_4$, when diode D_{in} starts conducting. The Fig.3.2(d), indicates the equivalent circuit for this interval.

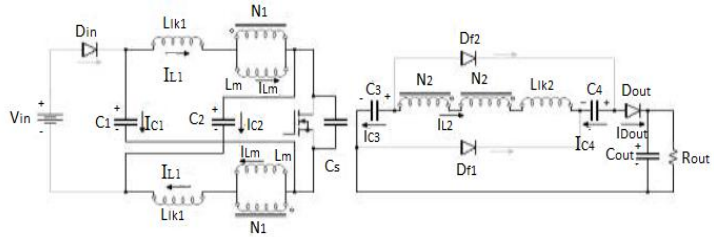

Fig 3.2(d): Operation in Mode 4

MODE 5 : Interval [t_4-t_5]: In this interval, energy stored in inductors L_m and L_{lk1} is discharged through source to capacitors C_1 and C_2. The current I_{Lm} decrease linearly. The leakage inductance L_{lk2} discharges its energy through capacitors C_3, C_4, diode D_o and load. The Fig. 3.2(e), indicates the equivalent circuit for this interval. The capacitor C_o is charged. In this interval, diodes D_{in} and D_o are conducting and freewheeling diodes D_{f1} and D_{f2} are off. This interval ends at $t=t_5$ when diode D_o is off.

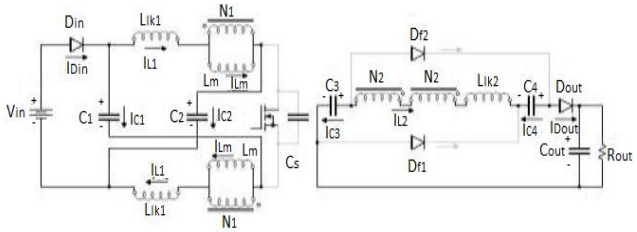

Fig 3.2(e): Operation of converter in Mode 5

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MODE 6: Interval [t_5-t_6]: In this interval, energy stored in inductors L_m and L_{lk1} are still discharged through source to capacitors C_1 and C_2. The I_{L2} current flows through capacitors C_3, C_4 and freewheeling diodes D_{f1}, D_{f2}. The Fig. 3.2(f), indicates the equivalent circuit for this interval. The capacitors C_1, C_2, C_3, and C_4 are charged. The capacitor C_o discharges its energy through load. This interval ends at $t=t_6$ when $V_{l2} = nV_{11}$.

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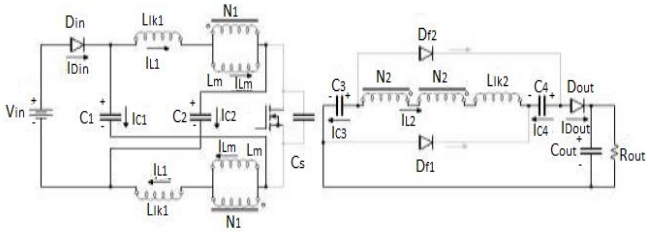

Fig 3.2(f): Operation of converter in Mode 6

MODE 7: Interval [t_6-t_7]: In this interval, switch S is OFF. In this interval all devises are in same state as in interval [t_5-t_6]. The magnetizing inductor L_m transfers its storage energy to the secondary side of coupled inductors. The capacitors C_3 and C_4 are charged. The capacitor C_o still discharges its energy through load. This interval ends at $t=t_7$, when switch S is turned ON. The fig. 3.2(g)," indicate equivalent circuit for this interval.

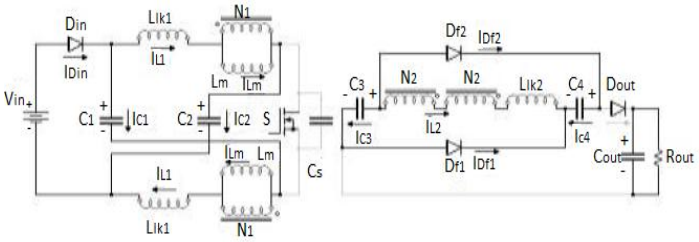

Fig 3.2(g): Operation of converter in Mode 7

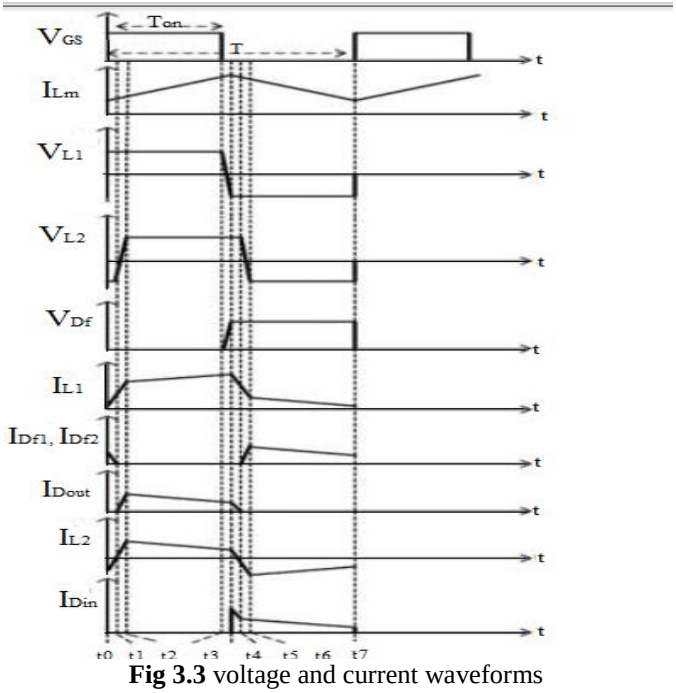

Fig 3.3 voltage and current waveforms

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3.2 STEADY STATE ANALYSIS OF DC-DC CONVERTER

Voltage gain in CCM intervals

The CCM is divided into seven intervals, but only two intervals is for long time. The interval [t_2-t_3] when switch S is ON and interval [t_6-t_7] switch S is OFF. The remaining intervals assume as a transient states. The one switching period is represent by T_s and D is a duty cycle. The voltage gain equation can be obtained from "Fig. 3.2(b)," and "Fig. 3.3(e)*"*.In CCM, each capacitor voltage Vc_1=Vc_2=V_c and Vc_3= Vc_4 are remain constant (same for each intervals). The primary inductor voltage V_{l1}(on) and V_{l1}(off) represent for ON time and OFF time respectively. Similarly secondary inductor voltage V_{l2}(on) and V_{l2}(off) represent for ON time and OFF time respectively.

Apply KVL for ON time period

At primary side

$$V_{l1}(on) = V_c \quad (1)$$

$$V_{lk1}=V_c-V_l(on) \quad (2)$$

By voltage dividing principle,

$$V_{lm}(on) = V_c\left[\frac{Lm}{Lm+Lk1}\right]$$

Assume

$$\left[\frac{Lm}{Lm+Lk1}\right] = K$$

$$V_l(on) = KV_c \quad (3)$$

$$V_{lk1} = (1-k)_c$$

$$V_{l2}(on) = -nV_{lm}(on)$$

$$V_{l2}(on) = -nKV_c \quad (4)$$

Similarly,

At secondary side

$$V_o = V_{c3} + V_{c4} - 2\,V_{l2}(on) \quad (5)$$

Apply KVL on *"*Fig. 12(e)*,"* for OFF time period

$$V_{in} - V_{l1}(off) = V_c$$

$$V_{l1}(off)=V_{in}-V_c \quad (6)$$

$$V_{c3} = V_{c4} = 2\,V_{l2}(off) \quad (7)$$

$$V_{l2}(off) = -nV_{lm}(off) \quad (8)$$

By applying voltage-second principle on primary inductor,

$$\int_0^{DTs} V_{l1}(on)dt + \int_{DTs}^{Ts} V_{l1}(off)dt = 0$$

$$DTsV_{l1}(on) + (1-D)T_sV_{l1}(off) = 0$$

From (1) and (6)

$$DV_c = -V_{in} + V_c + DV_{in} - DV_c$$

$$V_c = Vin\left(\frac{1-D}{2D-1}\right) \quad (9)$$

By applying voltage-second principle on secondary inductor,

$$\int_0^{DTs} V_{l2}(on)dt + \int_{DTs}^{Ts} V_{l2}(off)dt = 0$$

$$DTsV_{l2}(on) + (1-D)TsV_{l2}(off) = 0$$

From (4) and (8)

$$V_l(off) = -V_c\,[DK(1-D)] \quad (10)$$

From (8) and (10)

$$V_{l2}(off) = nV_c\,[DK(1-D)] \quad (11)$$

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Put value of (11) in (7)

$$V_{c3} = V_{c4} = 2nV_c\,[D(1-D)] \qquad (12)$$

By substituting value of (4) and (12) in (5)

$$V_o = 2nKV_c\left(\frac{1+D}{1-D}\right) \qquad (13)$$

Put value of (9) in (13) for CCM gain,

$$V_o = 2nKV_{in}\left(\frac{1+D}{2D-1}\right)$$

$$G_{ccm} = \frac{Vo}{Vin} = 2nK\left(\frac{1+D}{2D-1}\right) \qquad (14)$$

For perfect coupling K = 1,

$$G_{ccm} = \frac{Vo}{Vin} = \left(\frac{1+D}{2D-1}\right) \qquad (15)$$

VI. MPPT USING P&O ALGORITHM

Since solar cell has a lower output voltage and current, a number of solar cells are connected in series and parallel to form PV arrays for attaining the desired PV voltage and current. Their output characteristic variations depend on ambient temperature and insolation of sun. Figure 4.1 illustrates P-V curve of PV arrays at different insolation of sun, from which it can be seen that each insolation level has a maximum power P_{max} where P_{max1} is the most insolation of sun, while $P_{max3}$is the one at the least insolation. Three maximum power point Pmax1∼Pmax 3 can be connect by a straight line. The operational area is divided into two areas: A area and B area. When operational point of PV arrays locates in A area, output current I_{PV} of PV arrays is decreased to make the operational point close to its maximum power point (MPP). If operational point is set in B area, current I_{PV} will be increased to operate PV arrays at its MPP. The proposed power system adopts perturb and observe method to implement MPPT. Its flowchart is shown in Figure 4.2. In Figure 4.2, V_n and P_p separately represent their old voltage and power, and $P(=V_nI_n)$ is its new power. According to flowchart procedures of MPPT using perturb and observe method, first step is to read new voltage $V_n$and current I_n of PV arrays and then to calculate new PV power P_n.

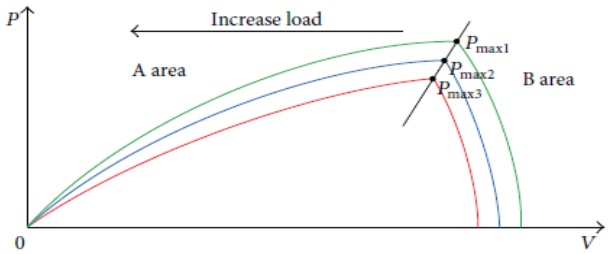

Fig 4.1: Plot of *P-V* curve for PV arrays at different isolation of sun

Next step is to judge relationship of P_n and P_p. Since the relationship of P_n and P_p has three different relationships, they are separatelyP_n>P_p, P_n= P_p, and P_n<P_p. Each relationship can be corresponded to the different relationship of $V_n$and V_p. Therefore, when the relationship of $P_n$and P_p is decided, next step is to find the relationship of $V_n$and V_p. According to the relationship of *P-V* curve of PV arrays, when the relationships of P_n and P_p, V_n and $V_p$are decided, working point of PV arrays can be specified. When working point of PV arrays locates in A area, power system connected in PV arrays to supply load power must decrease output power to close the distance between working point and MPP of PV arrays. On the other hand, when working point sets in B area, power system must increase output power to make working point to approach MPP of PV arrays. Finally, is replaced by V_n and P_p is also substituted by P_n. The procedure of flowchart returns first step to judge next working point of PV arrays. Moreover, when P_n= P_P and V_n= V_P, working point of PV arrays set in the MPP of PV arrays. The maximum power $P_P$of PV arrays is transferred to power management unit for regulating power of battery charging.

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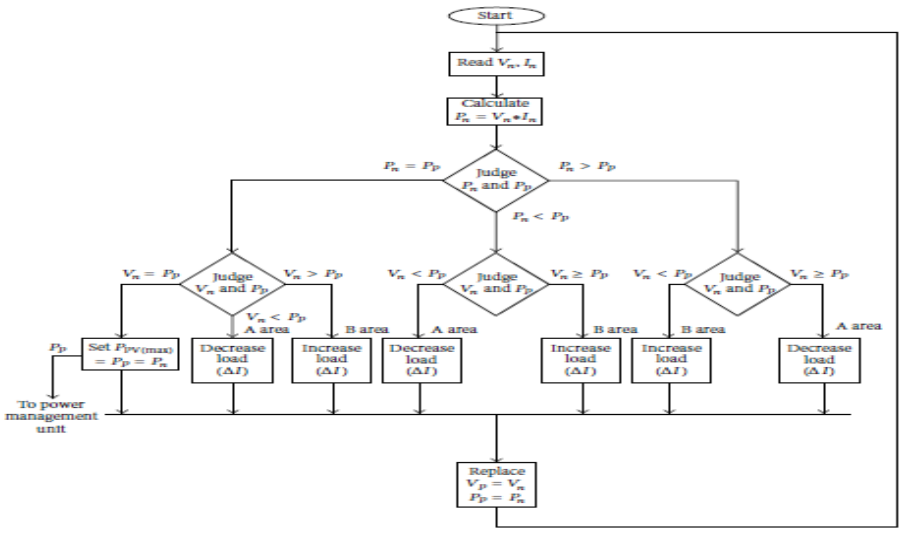

Fig 4.2: Flowchart of MPPT using perturb and observe method for PV arrays system

VI. STATE SPACE ANALYSIS OF THE CONVERTER

The state space analysis is the method of modeling the physical system mathematically. It relates the input, output and the state space variables using the differential equations. These differential and algebraic equations are written down in the form of the matrix. To encode all the information about the system with p inputs and q outputs one has to write down q*p Laplace transforms.

The smallest possible sub-set of system variables that represent the entire state of the system at any given time are called the state variables.

The general state-space representation of a linear system with p inputs, q outputs and n state variables is written in the following form:

$$\dot{\mathbf{x}}(t) = A(t)\mathbf{x}(t) + B(t)\mathbf{u}(t)$$
$$\mathbf{y}(t) = C(t)\mathbf{x}(t) + D(t)\mathbf{u}(t)$$

Where, x (t) = state vector
y (t)= output vector
u (t) = input vector
A= state matrix
B= input matrix
C= output matrix
D= feed forward matrix

The Interleaved Boost converter consists of two single Boost converters connected in parallel. The schematic diagram of Interleaved Boost Converter is shown in Figure 5.1.

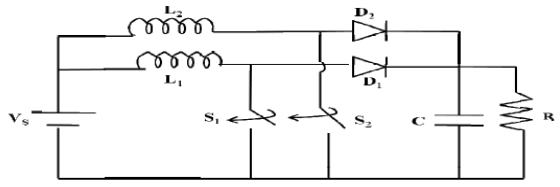

Fig 5.1 Schematic diagram of interleaved Boost converter

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During **mode 1** both the switches S_1 and S_2 are on and the diodes D_1 and D_2 are in the off condition. The equivalent circuit for this mode is shown in Figure 5.1(a).

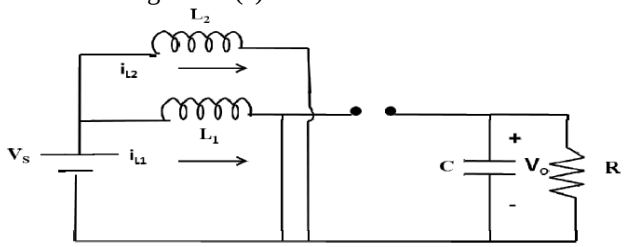

Fig 5.1(a) Operation of interleaved Boost converter for mode 1

Applying Kirchhoff's laws to the above circuit, the equations describing this converter for mode 1 can be obtained as follows,

$$\frac{dil1}{dt} = \frac{Vs}{L1}$$

$$\frac{dil1}{dt} = \frac{Vs}{L1}$$

$$\frac{dVo}{dt} = \frac{-Vo}{RC}$$

The coefficient matrices for this mode can be written as,

$$A_1 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{RC} \end{bmatrix} \qquad B_1 = \begin{bmatrix} \frac{1}{L1} \\ \frac{1}{L2} \\ 0 \end{bmatrix}$$

During **mode 2**, the switch S_1 is in on condition and switch S_2 is in off condition and the corresponding diodes are in the complementary switching states, (i.e.) D_1 is in off condition and D_2 is in on condition respectively. The equivalent circuit for this mode is shown in Figure 5.1(b)

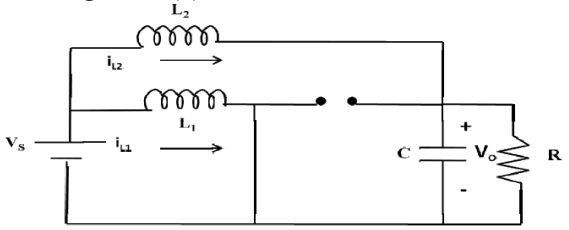

Fig 5.1(b) Operation of interleaved Boost converter for mode 2

Applying Kirchhoff's laws to the above circuit, the equations describing this converter for mode 2 can be obtained as follows,

$$\frac{dil1}{dt} = \frac{Vs}{L1}$$

$$\frac{dil2}{dt} = \frac{Vs}{L2} - \frac{Vo}{L2}$$

$$\frac{dVo}{dt} = \frac{il2}{C} - \frac{-Vo}{RC}$$

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The coefficient matrices for this mode can be written as,

$$A_2=\begin{bmatrix}0 & 0 & 0\\ 0 & 0 & \frac{-1}{L2}\\ 0 & \frac{1}{C} & \frac{-1}{RC}\end{bmatrix} \qquad B_2=\begin{bmatrix}\frac{1}{L1}\\ \frac{1}{L2}\\ 0\end{bmatrix}$$

In **mode 3**, the switch S_1 is in off condition and the switch S_2 is in on condition and the corresponding diodes such as D_1 and D_2 are in on and off conditions respectively. The equivalent circuit for this mode is shown in Figure 5.1(c).

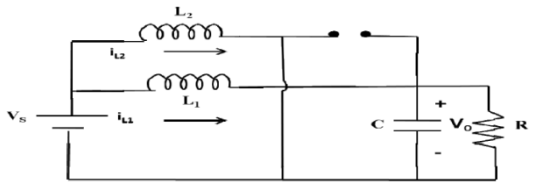

Fig 5.1(c) Operation of interleaved Boost converter for mode 3

Applying Kirchhoff's laws to the above circuit, the equations describing this converter for mode 3 can be obtained as follows,

$$\frac{dil1}{dt}=\frac{Vs}{L1}-\frac{Vo}{L1}$$

$$\frac{dil2}{dt}=\frac{Vs}{L2}$$

$$\frac{dVo}{dt}=\frac{il1}{C}-\frac{-Vo}{RC}$$

The coefficient matrices for this mode can be written as,

$$A_3=\begin{bmatrix}0 & 0 & \frac{-1}{L1}\\ 0 & 0 & 0\\ \frac{1}{C} & 0 & \frac{-1}{RC}\end{bmatrix} \qquad B_3=\begin{bmatrix}\frac{1}{L1}\\ \frac{1}{L2}\\ 0\end{bmatrix}$$

During **mode 4** the semiconductor switches S_1 and S2 are in off condition and the diodes D1 and D2 are in on condition, and the corresponding equivalent circuit for this mode is shown in Figure 5.1(d).

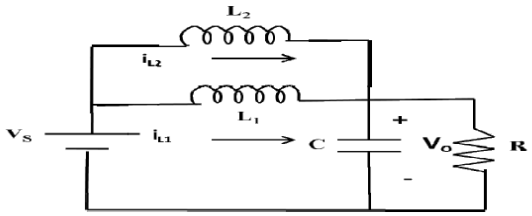

Fig 5.1(d) Operation of interleaved Boost converter for mode 4

Applying Kirchhoff's laws to the above circuit, the equations describing this converter for mode 4 can be obtained as follows,

$$\frac{dil1}{dt}=\frac{Vs}{L1}-\frac{Vo}{L1}$$

$$\frac{dil2}{dt}=\frac{Vs}{L2}-\frac{Vo}{L2}$$

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$$\frac{dVo}{dt} = \frac{il1}{C} + \frac{iL2}{C} - \frac{Vo}{RC}$$

The coefficient matrices for this mode can be written as,

$$A_4 = \begin{bmatrix} 0 & 0 & \frac{-1}{L1} \\ 0 & 0 & \frac{-1}{L2} \\ \frac{1}{C} & \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \quad B_4 = \begin{bmatrix} \frac{1}{L1} \\ \frac{1}{L2} \\ 0 \end{bmatrix}$$

The output equation is defined as follows,

$$Y(t) = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} il1 \\ il2 \\ Vo \end{bmatrix}$$

The coefficient matrix for the interleaved converter is defined as,

$[A] = (A_1*D) + (A_2*D) + (A3*D) + (A_4*D)$

$[B] = (B_1*D) + (B_2*D) + (B_3*D) + (B_4*D)$

D=0.28 , f =50kHz

$L_1 = \frac{VcDTs}{\Delta I} = \frac{12*0.28}{1*50*10\text{^}3} = 67.2\mu H$

$L_2 = L_1 * \frac{(N2)^2}{(N1)} = 67.2\mu H*(3/1)^2 = 604.8\mu H$

Transfer function is given by= $\{C\,[SI-A]^{-1}\,B\} + D$

Inverse of [SI-A] is found by Gauss Jordan Elimination Method

Transfer function = $\frac{C(S)}{R(S)} \Rightarrow \frac{1.967*10^{10}S}{S^3+11.2S^2+518.45*10^3S}$

Using Matlab program to find the bode plot , root locus and nyquist plot

num= [$1.967*10^{10}$ 0];

den= [1 11.2 $518.45*10^3$ 0];

sys= tf(num, den);

bode(sys);

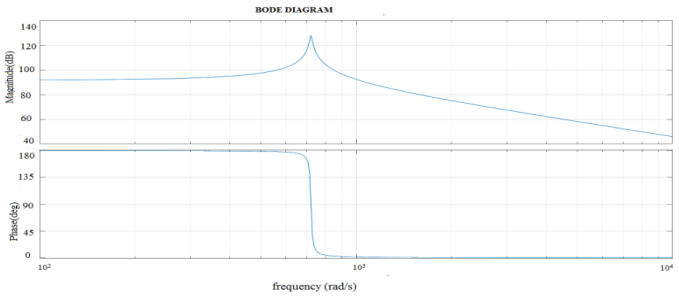

Fig 5.2 Bode plot of the transfer function

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VI. EXPERIMENTAL SETUP

6.1 SOFTWARE IMPLEMENTATION

6.1.1 SIMULATION AND ITS RESULTS

The Simulink model of the open loop of the boost DC-DC converter with interleaved inductors shown in the figure 6.1

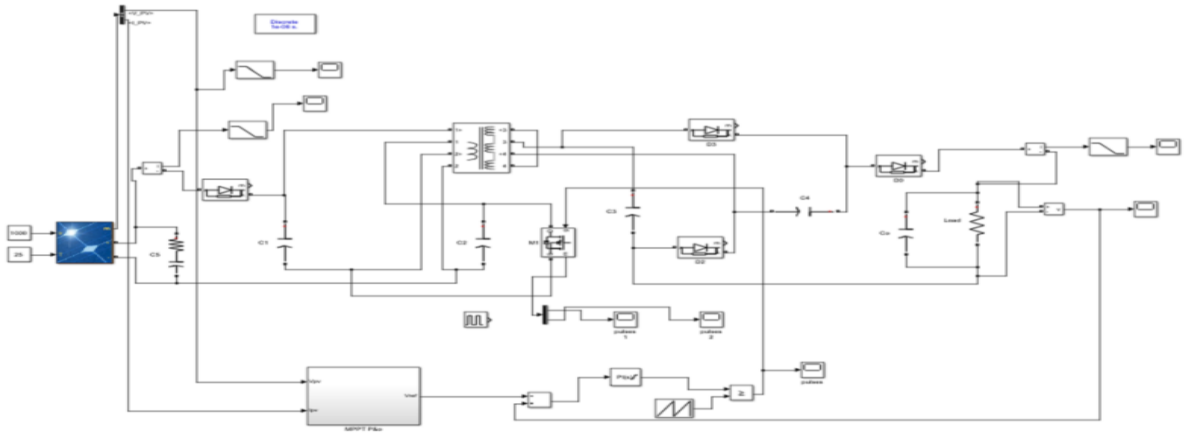

Fig 6.1 : Simulink model of the open loop of the step up DC-DC converter

Table 6.1 Components and parameters used in simulation

Components	Values
PV input voltage	19.2 volts
Irradiation	1000 rad/m^2
Temperature	25^oC
Frequency	50kHz
Capacitances C_1,C_2,C_3,C_4	1µF
Turns ratio of coupled inductor	2.9
Magnetizing Inductance	9.1509µH
Output Capacitance C_o	1000µF
Output Resistance R_o	100Ω
Output Voltage Vo	200 volts

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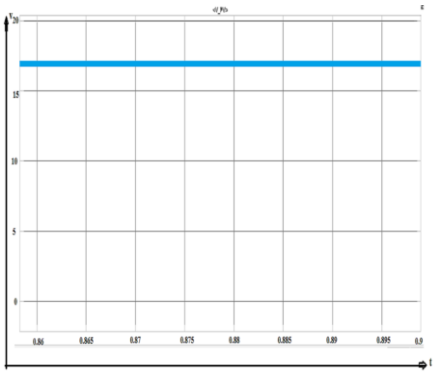

Fig 6.2: Input voltage from PV panel

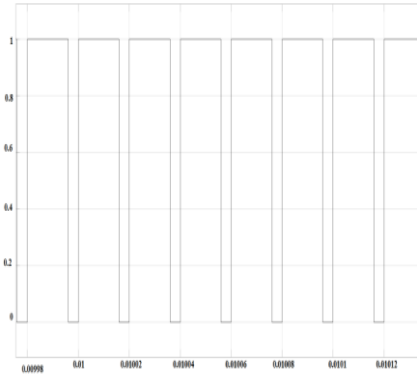

Fig 6.3: switching pulse across MOSFET

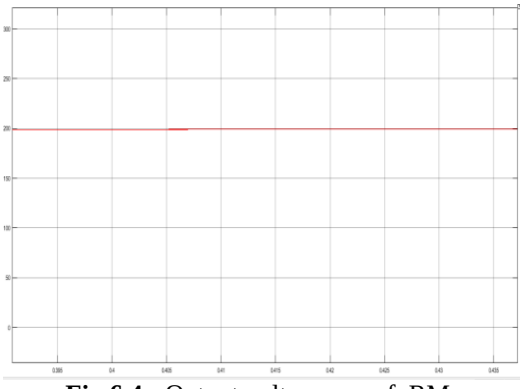

Fig 6.4: Output voltage wavefoRM

6.2 HARDWARE IMPLEMENTATION

6.2.1 System Model

From power distribution across large distances to radio transmissions, coupled inductors are used extensively in electrical applications. Their properties allow for increasing or decreasing voltage and current, transferring impedance through a circuit, and they can isolate two circuits from each other electrically. There are a wide variety of applications which exploit properties of transformers, such as tesla coils, impedance matching in audio frequency applications, potential transformers for reading very high voltages, Scott-T transformers which convert two phase components to three-phase (or vice versa), and many more.

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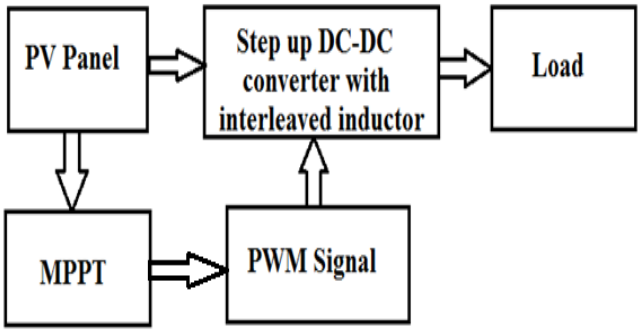

Fig 6.5.: Block Diagram of the DC-DC Converter model

6.3 Hardware description and Working

6.3.1 Circuit Configuration

The proposed high step-up converter, is a two-phase interleaved boost converter composed of a particular magnetic coupled-inductor composed by three windings that can be installed in different core configurations. There are two winding, L_1 and L_2, connected to the power source and a third winding L_c, defined as central winding, located between the cathodes of D_1 and D_2. For convenience, we define the positive terminal of L_c as the node where the cathode of D_1 and the anode of D_3 are connected.

6.4 Working Principle

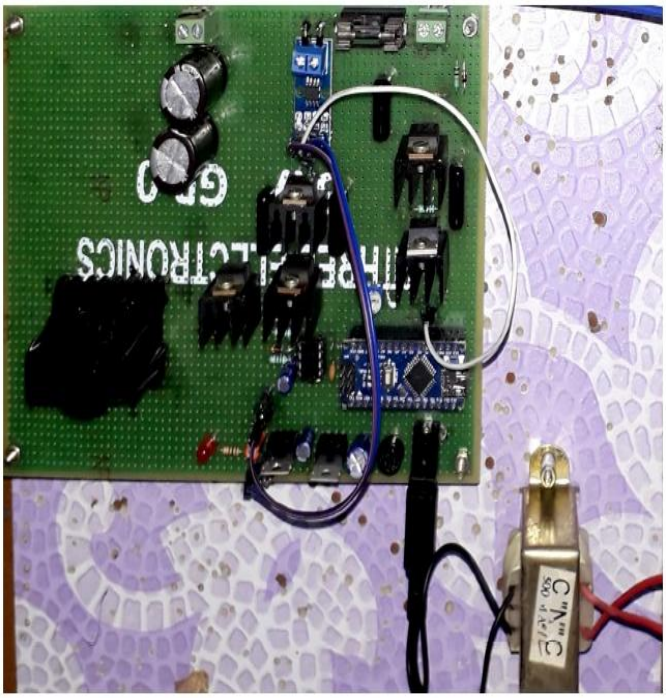

Fig 6.6: Hardware Model

The input to the converter is given from solar panel. In the proposed converter the input voltage is boosted using Coupled inductor. The use of coupled inductor gives a high gain for efficient system. The feedback voltage from

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the input and current drawn is feedback to the microcontroller. The microcontroller implements MPPT algorithm to drive the MOSFET gate voltage. The MOSFET gate is operating at a switching frequency of 40kHz.The duty cycle of the PWM is varied based on the irradiance on the solar panel. The hardware implementation of the proposed converter is shown in figure 6.6.

6.5 Hardware Results

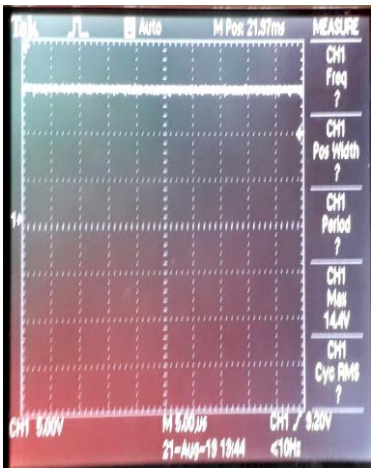

Fig 6.7: Input from PV Panel

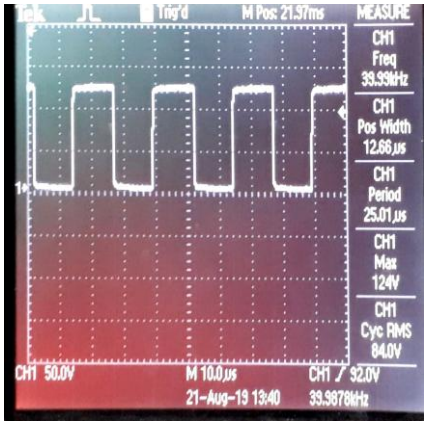

Fig 6.8: Switching Pulse

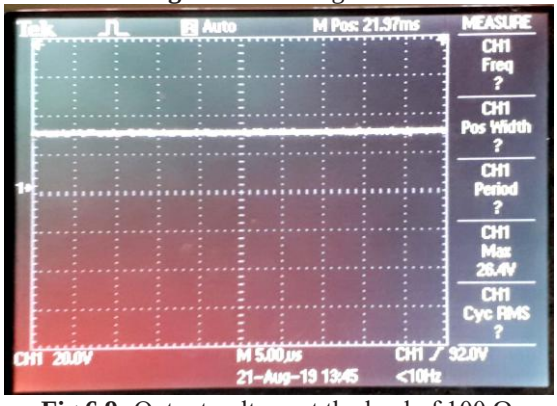

Fig 6.9: Output voltage at the load of 100 Ω

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VII. CONCLUSION

An isolated high step-up dc-dc converter with low voltage stress is presented. The proposed converter achieves extremely large voltage conversion ratio with appropriate duty cycle and reduction of voltage stress on the power devices. The topology utilizes coupled inductor. The leakage inductance energy can efficiently be discharged. Since the device stresses are low in this topology, low voltage MOSFETs with small R_{DS}(on) values can be selected to reduce the conduction loss. These features improve the converter efficiency. When compared to other topologies the proposed converter contain only one switch which simplify the circuit configuration and improve the system reliability. All these factors improve the circuit performance in the high step-up applications.

Isolated DC-DC boost converter sourced by a PV panel was simulated by MPPT algorithm. The P&O algorithm implemented was found successful in tracking the maximum power from the PV panel. The switching losses will be less when compared to conventional topologies since less number of power electronic switches are used. Due to coupled inductor isolation is present between input and output. The overall efficiency of the proposed chopper circuit is higher than that of the existing topologies.

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