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Design of 8X1 Low Power Multiplexer by using Transmission Gates

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ABSTRACT: Low power and very high speed digital circuits are basic the needs for any of digital circuit, Multiplexer is a basic circuit for any digital circuit. In this paper, different techniques of multiplexer designs like low risk Conventional technique, complementary CMOS, Transmission gate(TG) and Gate Diffusion Input(GDI) has been introduced and their comparison on the basis of power, delay and Area (number of transistor) is done. A low power Multiplexer has been introduced which consumes less power as compare to the above mentioned logic but have more delay as compare to the other ,On the basis of these analyses it is concluded that proposed multiplexer is better technique for designing an low power low area Multiplexer design but it has high delay as compare to the other Multiplexer.

KEYWORDS: CMOS, PT,TG,GDI

I.INTRODUCTION

The increasing demand for low-power very large scale integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing Combinational circuits. This is because all the important parameters governing power dissipation, switching capacitance, transition activity, and short-circuit currents are strongly influenced by the chosen logic style. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important, disallowing the formulation of universal rules for optimal logic styles .

This paper analyzes 8-to-1 multiplexer using complementary CMOS, Transmission gate and Gate Diffusion Input. These implementations are compared based on the basis of transistor count, power dissipation, and delay. A multiplexer is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of inputs has n selected lines, which are used to select which input line to send to the output that is why it is also called a data selector. Multiplexer can also be used to implement any combinational circuit. So by simplifying design of multiplexer, design of many combinational circuits can be simplified. Fig.1 and Table1 show the block diagram and truth table for 8 to1 multiplexer given below.

II. LITERATURE REVIEW

Complementary Metal Oxide Semiconductor, abbreviated as **CMOS** is a technology for constructing integrated circuits. CMOS is also sometimes referred to as **complementary-symmetry metal–oxide–semiconductor** (or COS- MOS). The words "complementary-symmetry" refer to the fact that the typical design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.Two important characteristics of CMOS devices are high noise immunity and low static power consumption.

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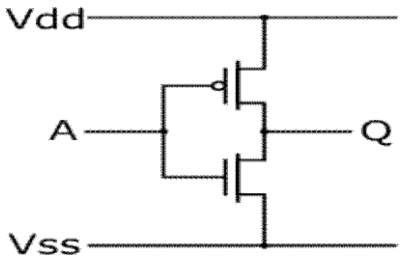

Figure 2.1 Basic CMOS cell

In electronics, **pass transistor logic** (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage.

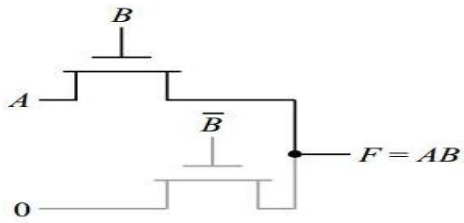

Figure 2.2 example of pass transistor logic

III.POWER TECHNIQUES

A. Gate Diffusion Input (GDI):

Apart from Conventional CMOS design, another alternative low power and area efficient technique is GDI technique.A basic GDI cell consists of four terminals- D (common diffusion of both transistors), N (outer diffusion node of nMOS transistor), P (outer diffusion node of pMOS), G (common gate input to both pMOS and nMOS transistors). Depending on the circuit structure and its mode of operation P, D and N can be used as either inputs or outputs.

IV. DESIGNING OF 8X1 MUX BY USING LOW POWER TECHNIQES

In this paper different Low power techniques are design and these techniques are compared with complementary CMOS with respect to total number of transistors and area and delay and power consumption. These multiplexers were designed on S-edit of Tanner tool on 45nm technology and simulated on T-edit with 1v power supply. Figures shows schematics of multiplexers designed using two logic styles.

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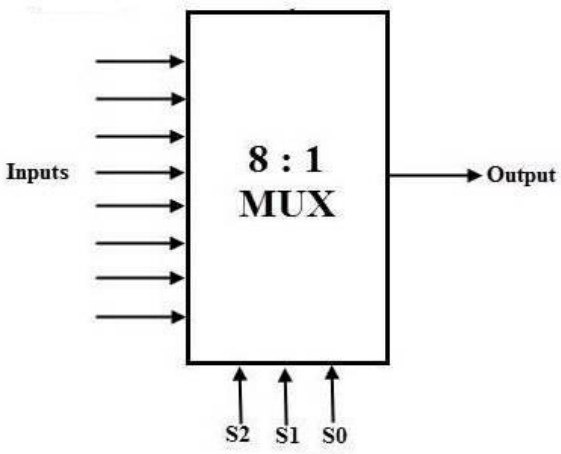

Fig 4.1: 8X1 multiplexer

TABLE 1: Truth Table Of 8X1 Mux

SELECTION LINES			INPUTS							O/P	
S2	S1	S0	A	B	C	D	E	F	G	H	Y
0	0	0	1	0	0	0	0	0	0	0	A
0	0	1	0	1	0	0	0	0	0	0	B
0	1	0	0	0	1	0	0	0	0	0	C
0	1	1	0	0	0	1	0	0	0	0	D
1	0	0	0	0	0	0	1	0	0	0	E
1	0	1	0	0	0	0	0	1	0	0	F
1	1	0	0	0	0	0	0	0	1	0	G
1	1	1	0	0	0	0	0	0	0	1	H

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Conventional CMOS

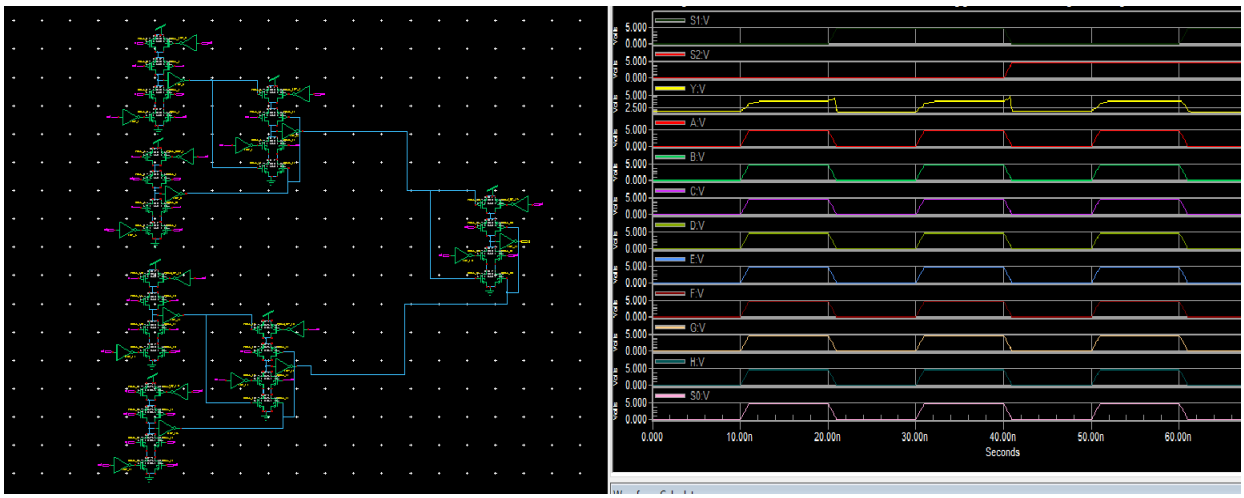

Fig 4.2: CMOS 8X1 mux Schematic design and output wave form

From fig4.2 we can say that the CMOS technique utilizes more as large number of transistors are used resulting in large power dissipation.

A. Gate Diffusion Input (GDI):

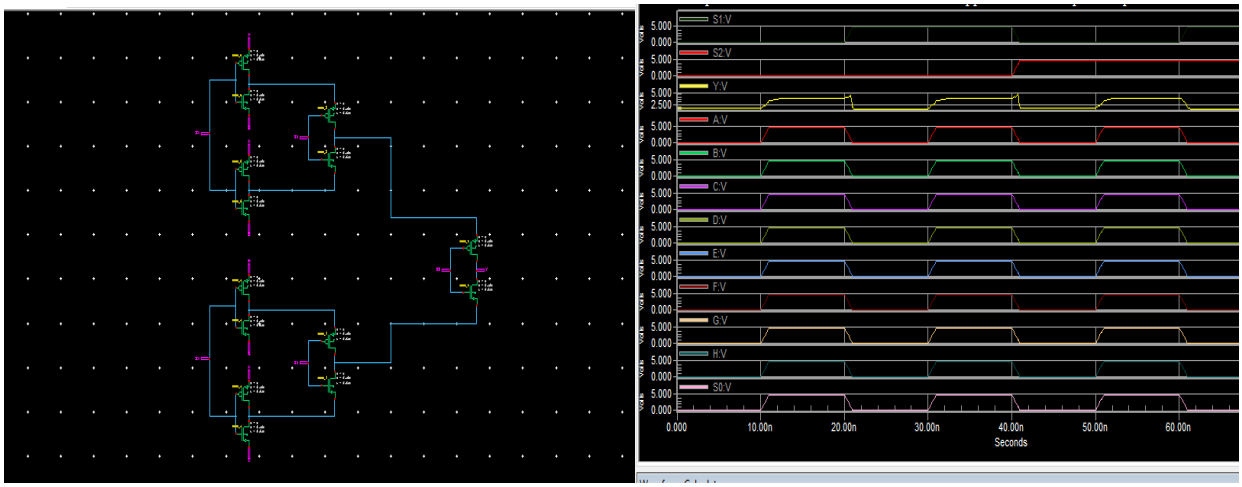

Fig 4.3: GDI 8X1 mux Schematic design and output wave form

From fig 4.3 we conclude that GDI technique uses less number of transistors resulting in less power dissipation as compared to cmos.

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B. Transmission gate(TG) logic:

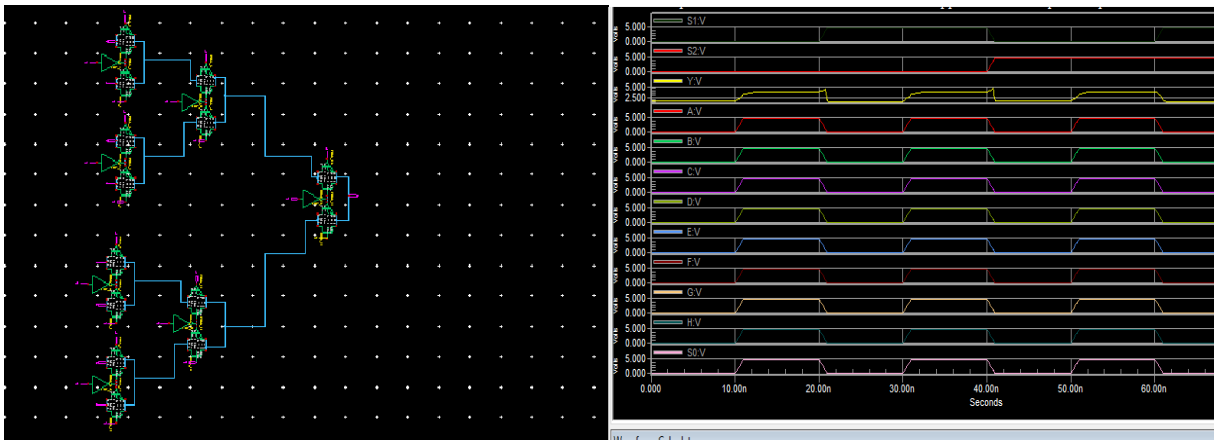

Fig 4.4: TG 8X1 mux using Schematic design and output wave form

From fig4.4 we get high speed and low power dissipation compared to other techniques it is seen that from this technique

V. RESULT

TABLE 2:COMPARISION 0F VARIOUS DESIGN TECHNIQUES ON THE BASIS OF DESIGNMETRICES

Sr.no	Technique	Transistor count	Speed	Power Dissipation	used Area
1	CMOS	56	HIGH	$15.511x10^{-8}$	MORE
2	GDI	14	LOW	$7.457\ x10^{-8}$	LOW
3	TG	30	HIGH	$8.933\ x10^{-8}$	MORE

VI.CONCLUSION

In this paper, the digital circuit 8X1 mux was implemented by different low power techniques namely CMOS, GDI and Transmission Gate. The results were simulated using tanner EDA and comparison has been done for different parameters like power dissipation, speed, area and transistor count.

The results concluded that as compared to other proposed techniques, CMOS has more power dissipation and transistor count. These advantages of proposed techniques over CMOS make them more efficient and convenient to be used in digital circuits

REFERENCES

1. “Design and Operation of 4*1 Low Power Multiplexer Using Different Logics”International Journal of Emerging Science and Engineering (IJESE) ISSN: 2319–6378, Volume-4 Issue-8, February 2017
2. "Design And Simulation Of 4*1 Mux Based On Low Power Design Techniques"- volume 2 Issue 2 March-April2015
3. "Design of Low power multiplexers using different Logics"- Vol.- 4, Issue – 2 pp 2229 – 6646
4. "low power cmos logic circuits" volume 2 Issue 2 481-520
5. "Top-down pass transistor logic design" *IEEE J. Solid-State Circuits*, vol. 31, pp 792–803, June1996.
6. "Low power CMOS digital design," *IEEE J. Solid- State Circuits*, vol 27, pp.473– 484, Apr. 1992.
7. "Low-power logic styles: CMOS versus pass- transistor logic" IEEE J. Solid-State Circuits, vol. 32, no. 7, pp. 1079{1090, Jul. 1997.
8. "Design of Energy Efficient Arithmetic Circuits Using Charge Recovery Adiabatic Logic" in IJETT, 2013.
9. "Gate-diffusion input (GDI) – A technique for low power design of digital circuits: Analysis and characterization,” in *ISCAS*, May 2002

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BIOGRAPHY

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