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Study on Different Works Done for Error Correction of Encoded Data Using Different Algorithms

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ABSTRACT:Nowadays, in the advanced world of electronics, computing system plays a major role. Many a times, in this computation process the transmitted and received data mismatches generating error. Hence, various data comparison algorithms are taken into account to compare the piece of information from sender to receiver's end. Often, this results in circuitry complexity. Here in this paper, we will discuss about different works done for designing an area efficient, low complexity and minimized delay system with error correction.

KEYWORDS: Data comparison, Error Correcting Codes(ECC), Systematic Codes, Hamming Distance, Saturate Adder(SA), Butterfly Weight Accumulator(BWA).

I.INTRODUCTION

When we discuss about high speed access or about any computation systems, CDs or computer memories the major issue which commonly arise is data mismatching when data is brought together from different sources and compared. To overcome this, many researchers have used different proprietary matching algorithms in their own unique way to effectively match the overall result. An ideal VLSI designed systems aims at high speed, area effective and low power dissipating systems. In this survey, it is found that the designers have efficiently worked out for designing area effective, low complexity and low latency. For this, the architecture using BWA with Error Correcting Codes is mainly used by the researchers. So, in this paper let us discuss about the researches done by the different authors in that thesis.

II. LITERATURE SURVEY

Till date various types of works have been done and still going on to overcome this problem of data mismatching and complexity during data mismatching and calculating hamming distance. Few of them have been studied and listed below:

Wei et al (2011)reported that mostly the information should be compared and matched in a computing system. If the stored data is protected with ECC, the previous solution is to accesses the stored information, decode and correct before comparison with the incoming data. Hence, the author proposed a technique to reduce the complexity latency for ECC encoded data. Using cache tag array look-up the result is reported with 30% area reduction and 12% delay reduction.

Kong et al (2013)proposed a new architecture with error–correcting code to minimize delay and complexity for matching the protected data that parallelizes the comparison of the data and that ofthe parity information.Moreover,the delay and complexity is reduced using BWA to efficiently calculate the Hamming distance.

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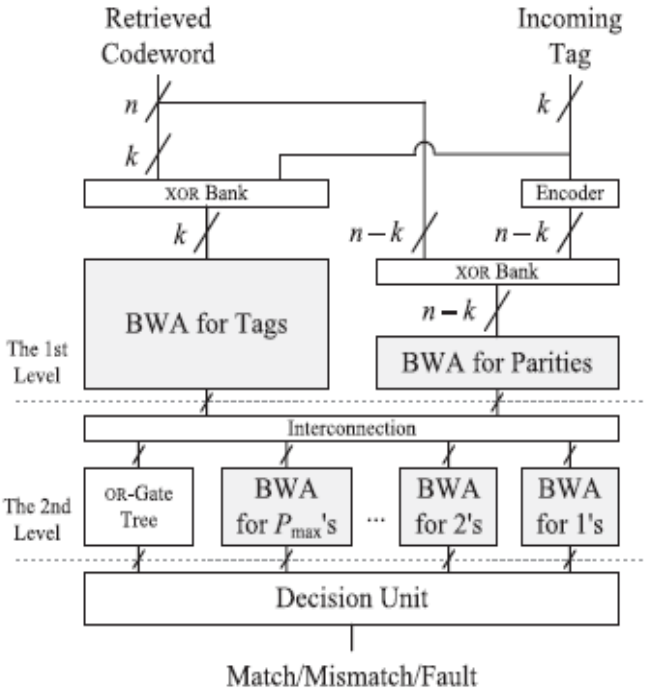

Fig 1 Proposed architecture for Systematic code words [2]

Also, the proposed architecture compares the incoming data and the stored data if a certain number of erroneous bits are corrected. Five half adders are replaced by a simple OR gate to reduce complexity. It is reported that, for a (40, 33) code, this architecture reduces the delay and the hardware complexity by ~32% and 9%, respectively.

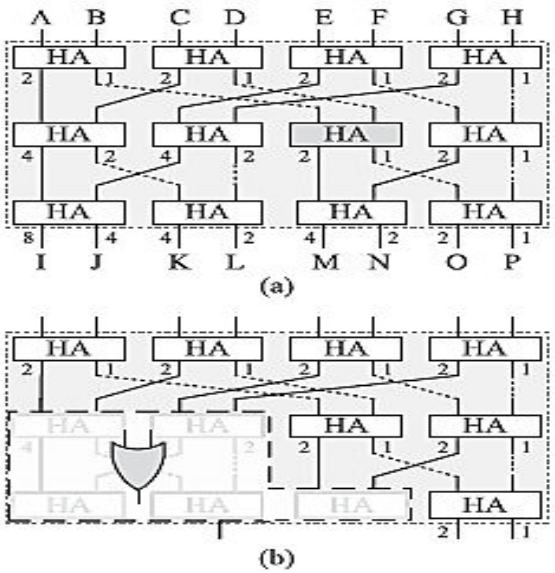

Fig 2 (a) Existing and (b) Proposed BWA architecture for matching of data [2]

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Nath et al (2015)reported that incoming data is to be compared with the stored one for matching entry location. Pre comparison, decoding and correction should be done if the stored data is ECC protected. Generally BWA is used for calculating hamming distance. Here, BWA circuitry is replaced using modified half adder (HAM) and modified XOR gate (XORM).

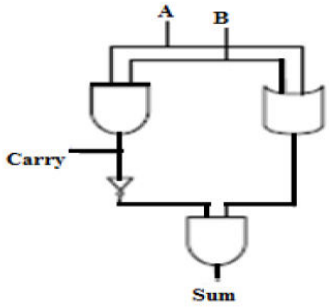

Fig.3. Modified Half Adder (HAM) [3]

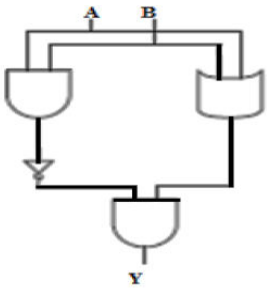

Fig.4. Modified XOR gate (XORM) [3]

It is found that XORM has 1 gate less than the conventional XOR gate of 5 gates (AND-OR-NOT implementation). HAM is reduced by two gates, resulting in area reduction by 20.44% and delay is reduced by 10.70%. The proposed work was done in Xilinx 13.2.

Chaithanya et al (2016)proposed an area efficient, low complexity, low latency architecture for matching data, protected with linear block codes that can correct single, double-adjacent, triple-adjacent and double-almost-adjacent errors [4]. The data is encoded and compared using different architectures. Additionally, hamming distance is efficiently computed by using a new Butterfly Weighted Accumulator. The proposed work encodes and compares the data using BWA based, BWA modified and BWA-Hamming modified architecture. Gate level modification is also proposed which resulted in reduced area. BWA based architecture resulted in 36.25% area reduction and 89.15% of delay reduction. BWA modified architecture resulted in 42.53% area reduction and 89.15% delay reduction. BWA-Hamming modified architecture is found to be anefficient architecture with50.36% area reduction and 89.15% delay reduction. The performance of the same is evaluated using Xilinx Synthesis Tools.

Mary et al (2016)proposed an architecture where ECC delay is moved to the noncritical path of the process by directly comparing the retrieved tag with the incoming new information which is encoded as well, thus reducing circuit complexity [5]. Furthermore, BWA architecture is introduced for calculation of hamming distance. The proposed

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encode and compare BWA based modified architecture resulted in 25.18% area reduction and 16.88% delay reduction. The proposed architecture is coded in Verilog and simulated using Xilinx ISE design suite 14.7.

Kalyani et al (2015)proposed an architecture which matches data using error correcting codes. The proposed architecture parallelizes the data bits and parity bits. A new BWA is introduced to compute hamming distance which counts the number of 1s among its input bits. The proposed work improved latency by 69.74% and power consumption is reduced by 48%.

Anju et al (2015) reported that most of the times the information needs to be compared with the stored data to locate the matching entry, for instance, cache tag array look up and translational look-aside buffer [7]. The proposed architecture parallelizes the comparison of data and parity bit. Furthermore, `latency and complexity is reduced using BWA computing the hamming distance. The proposed work of modified BWA architecture resulted in 24.71% of area reduction and 17.21% of delay reduction. The power consumption is found to be reduced by 43.59%.

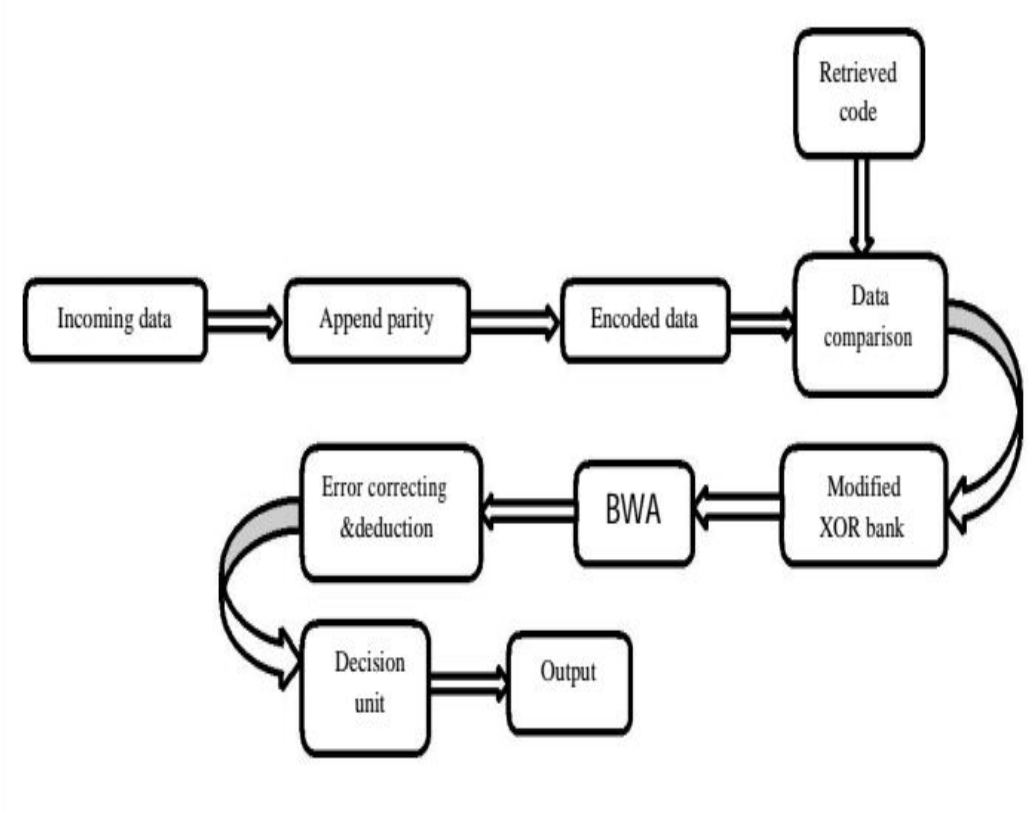

Fig 5 Modified BWA block diagram representation [7]

Srinivas et al (2016)reported that data comparison is done to find the matching data already stored resulting in error signal if mismatched the incoming and stored data. Error correcting codes are used to detect and correct the error so generated. A conventional method is compared with a new technique i.e. butterfly-formed weight accumulator to find hamming distance, reducing the complexity and latency. Here the BWA works to count 1s in the input and each bit are weighted in the half adder stages. Half adders are connected so as to accumulate the sum and carry bit separately in the butterfly form. The proposed architecture resulted in 14.28% latency minimization and hardware complexity is reduced by 9.48%.

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III.RESULT AND CONCLUSION

Below is the table listing complexity, latency and power reduction while surveying on different works done for Error Correction of encoded data using different algorithms:

Architecture	Reduction Percentage (%)		
	Area/Complexity	Delay/Latency	Power
Direct Compare Design	30	12	-
BWA for Systematic codewords	9	32	-
HAM and XORM	20.44	10.70	-
a) BWA Based Architecure b) BWAM Based Architecture c) BWA HM Based Architecture	36.25 42.53 50.36	89.15 89.15 89.15	-
Encode and Compare BWA Based Modified Architecture	25.15	16.88	-
BWA Architecture	-	69.74	48
BWAM	21.71	17.21	43.59
BWA Using ECC	9.48	14.28	-

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