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BCD Adder design using Approximate Adder in Quantum-dot Cellular Automata

K.Vinitha, B.Dhanam, Dr.K.Ramasamy

Department of Electronics and Communication Engineering, P.S.R. Rengasamy College of Engineering for Women, Sivakasi, Tamil Nadu, India

***ABSTRACT*:** The advancement of the CMOS digital design lies in reducing the process technology, projected to end in the next few years due to CMOS fundamental physical limits. Among the emerging technologies recently proposed as alternatives to the classic CMOS, Quantum-dot cellular automata (QCA) is one of the most promising solutions to design ultra-low-power and very high speed digital circuits. Efficient QCA-based implementations have been demonstrated for several binary and decimal arithmetic circuits, but significant improvements are still possible if the logic gates inherently available within the QCA technology are smartly exploited. Conventional precise adders need long delay and high power consumption to obtain accurate results. Error tolerance of some applications such as multimedia processing, signal processing and machine learning have encouraged the development of approximate adders that generates inaccurate results occasionally to reduce delay and power consumption by using approximate architecture in the design of QCA that leads to reduction of QCA cell count and area consumption. This paper demonstrates the functionality, test and validates the design of BCD adder using approximate adder using QCA Designer simulator tool.

KEYWORDS: QCA, QCA cell, five-input majority gate, BCD adder, approximate adder.

I. INTRODUCTION

In last decade various Nano electronics devices have been of attention to the research community which contains silicon nanowires, resonant tunneling diodes, carbon nanotubes, and others. These devices have emerged as alternatives to the VLSI technology. Conventional VLSI technology is purely based on CMOS. Conventional device physics is based on a flow of free electron model. Nowadays Nano electronics provides a noble introduction to the quantum mechanics of electrons based quantum-dot cellular automata (QCA) devices. QCA is a substitute to the customary CMOS-based technology [10]. Because the present silicon transistor technology faces challenging complications, such as large power consumption and difficulties in feature size reduction, and their physical limits such as power dissipation, current leakage. A Quantum-dot Cellular Automaton (QCA) was first introduced in 1993 which became as a one of the promising future solutions. In QCA, the device which is used for logic is also used as device for interconnect. The basic logic gates in the QCA is the majority gate (MG) and the inverter. Majority gate is also referred to as the majority voter [5]. Adder forms vital circuits for most digital systems and numerous adder designs in QCA have been proposed [6]. Enhanced adder performance depends on reducing the carry propagation delay. Orthodox adder circuits commonly require lots of wires which are comparatively challenging to realize and slow in QCA technology. Most prior adder designs are limited in speed due to these wire delays. This paper presents a new adder design [11], based BCD adder that is optimized for implementation with QCA. The BCD adder design is compared with prior QCA adder designs [1].

II. BACKGROUND OF QCA

QCA is a new technology in nanometer scale. It is an advanced access towards the modern era. In CMOS systems some circuits used for computation such as logic gates and some other circuits used for signal or data transfer such as wires. In contrast computation and communication occurs simultaneously in QCA. QCA is a transistor less computation approach which encodes binary information via flow of charges as quantum dots. QCA technology operates at THz frequencies and has density of 10^{12} devices/cm^2.

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QCA takes great advantage of a physical effect of the cell, the Coulomb force that interacts between electrons. Though it is still difficult to yield and activate with these devices below typical temperature settings, simulations forecast promising numbers, like theoretical clock rates of several THz. QCA does not operate by the transport of electrons, but their operation is based on the fine-tuning of electrons in a small limited space of only a few square nanometers. Power consumption of QCA is extremely lower than CMOS because there is no any current in the circuit and output capacity. QCA is implemented by quadratic cells named as QCA cells. QCA cells are in squares shape has just four potential wells are located in each corner of the QCA cell (see figure 1). In the QCA cells, exactly two electrons are locked in potential well that is only two wells able to be fill with electron and remaining two potential well remains empty. The potential wells are connected with electron tunnel junctions act as tunneling capacitor. By using a clock signal they can be unlocked for the electrons to travel through them under a particular condition. Due to the Coulomb force that interacts between the two electrons and without any interaction from outside will try to separate the electrons from each other as far as possible. The diagonal is the largest possible distance for them to reside so the electrons diagonally reside into potential well (see figure 2).

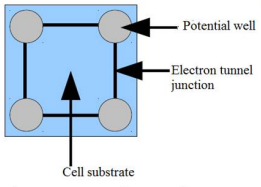

Figure 1. Anatomy of a QCA cell

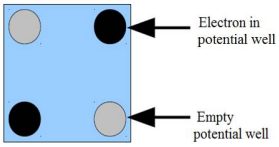

Figure 2. Electrons in potential well

A. DESIGN RULES

Cells are expected to have a breadth and altitude of 18 nm and quantum dots which is placed inside the cells are of 5 nm diameter. The cells are placed on a grid with a cell center-to-center distance of 20 nm. Thus, the cell size can be defined as 20 nm. Present-day works demonstrate that the possible QCA implementations have cell sizes of 3 nm, 2.8 nm, and 1.32 nm. There are propagation delays between cell to-cell reactions and there should be a boundary on the maximum cell count in a clock zone. This protects the appropriate propagation delay and reliable signal transmission. In physical design viewpoints, that there are several circuit operation issues like long span wires are additional vulnerable to noise and perhaps encourage the signal back propagation. Thus, the maximum cell count can be set as a design parameter, such as 15 cells for each clock zone is set as maximum cell count. The clock is incremented synchronously at the input sides of a gate. For the circuit layout and operation check, a simulation tool named QCADesigner, is used for QCA circuits. This tool permits operators to do a custom layout and then verify QCA circuit operation by simulations. Bistable approximation and a coherence vector are two different simulation engines used for simulation.

B. EDITING FEATURES

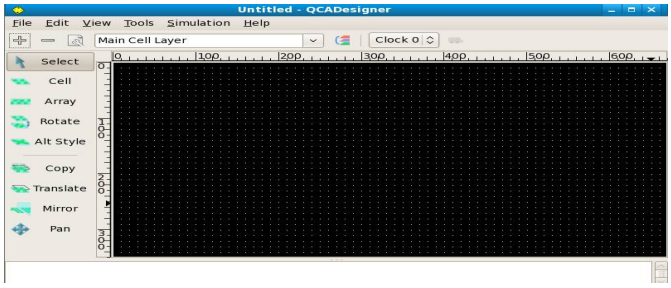

Fig 3. QCADesigner 2.3 layout editor window

QCA cells are able to draw individually or in arrays, cells are ranged to a grid with a default spacing of 20 nm which is equal to the default cell size of 18 nm plus the default inter cell spacing of 2 nm. Providing clock signal for each QCA cell is essential to have synchronous circuits functioning accurately. For Multi-layer QCA layout design multilayer signal crossing is required. Representation of QCA cells with 90 degrees rotation is essential to have in plane signal crossing. Graphical marking of special cells on via and crossover layers is possible. The simulation can be achieved by an

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exhaustive set of input vectors, or otherwise with a user-defined set of input vectors. QCA Designer simulation inputs window has the option to specify a set of user defined input vectors, or otherwise choose an exhaustive simulation.

C. DESIGN PROCEDURE

The following are the steps followed to design a circuit in QCA.

1) Open the QCADesigner tool and save the filename
2) Press cell in editors window to insert cell.
3) To insert array of cells click array and trap the cells up to required cell count
4) To give clock signal first click select option and then select the cell to give clock signal choose one of four clock signal zones.
5) Rotate is used to rotate the cell orientation.
6) Pan is used to detect the design. W and Q keys are used for zoom in and zoom out options.
7) To provide input click on simulation in that click simulation type setup, vector table will be display. Inputs are given in this vector table.
8) Simulation engine must be as bistable approximation.
9) Bistable option is used for setting parameters such as clock high, clock low, number of samples etc.
10) Animation is possible to see the flow of electrons for this purpose animate option want to be selected.
11) Start the simulation. Result window is opened. It gives the output waveform

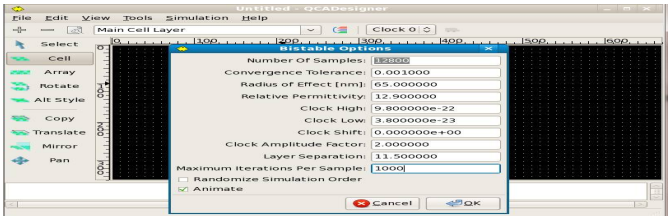

Fig 4. Bistable engine setup

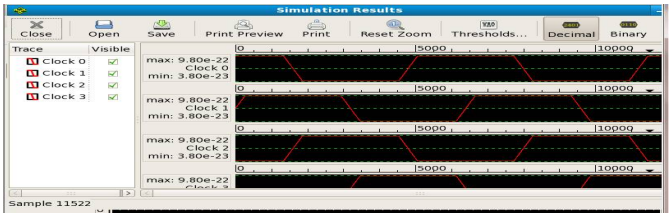

Fig 5. Simulation window

III. BASIC QCA DESIGN

A. FULL ADDER

The supreme uncomplicated arithmetic task is the addition of two binary digits. A full adder is a combinational circuit that executes the arithmetic sum of three bits: a, b and a carry in, Cin, from a preceding addition and it gives the corresponding sum, S, and a carry out Co as output. A full adder may be designed by using two half adders in series or by using Boolean expression.

QCA Addition Algorithm

There are two approaches in the QCA research area. One is a physical design and the other is an algorithmic design. From top to bottom level designs in addition to physical design QCA concentrates on the logical and algorithmic design. The algorithmic approach is also a significant part in high level systems because the QCA circuit designs need to manage physical interactions which are probably undesirable and disruptive. Basic adder design based on majority gate is given in Figure 6.

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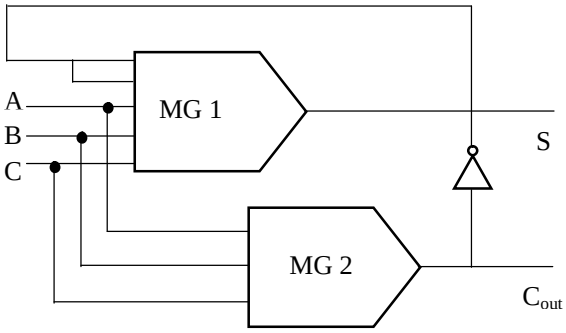

Fig 6. Circuit diagram of full adder using QCA gates

TABLE I. FULL ADDER TRUTH TABLE

A	B	C	$\hat{C}_{out}$	$\hat{C}_{out}$	Sum	C_{out}
0	0	0	1	1	0	0
0	0	1	1	1	1	0
0	1	0	1	1	1	0
0	1	1	0	0	0	1
1	0	0	1	1	1	0
1	0	1	0	0	0	1
1	1	0	0	0	0	1
1	1	1	0	0	1	1

Majority Logic of Carry:
Cout = AB+BC+AC
= M (M (B,M(A,C,1),0),M(A,C,0),1)
= M (A, B, C)
Majority Logic of Sum:
Sum = ABC+A'B'C+A'BC'+AB'C'
Figure 7 shows the implementation of full adder in QCA

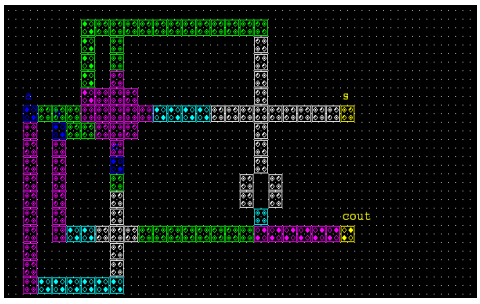

Fig 7. Full adder design in QCA

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Each color in the diagram indicates the clock pulses of various clock zone. QCA has four clock pulses as clock 0, clock 1, clock 2, and clock 3. The design should be in order. The flow of signal is from clock 0 to clock 1 and clock 1 to clock 2 and clock 2 to 3 and clock 3 to clock 0. Like this the signal flows into the circuit.

B. BCD ADDER

A BCD adder is a circuit that adds two BCD numbers and produces a sum also in BCD form. Design of a BCD adder need three major parts such as Binary adder, above nine value detection unit and correction unit. In these the Binary adder executes the addition process on two BCD numbers and one-bit carry input. Over 9 detection unit identifies if the outcome of first part is more than 9 or not. If the outcome is more than 9 it produces 1 otherwise 0. The key drawback of the conventional decimal adder is its low speed as all the first level 4-bit adders must wait for a number of 4-bit additions to get the right carry input.

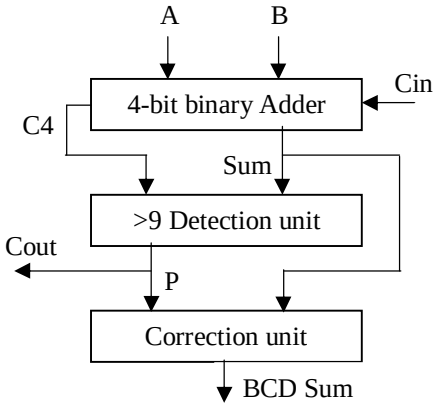

Fig 8. BCD adder block diagram

If the outcome result is one then the six is added with the sum otherwise sum would be added with zero. Correction unit performs this process.

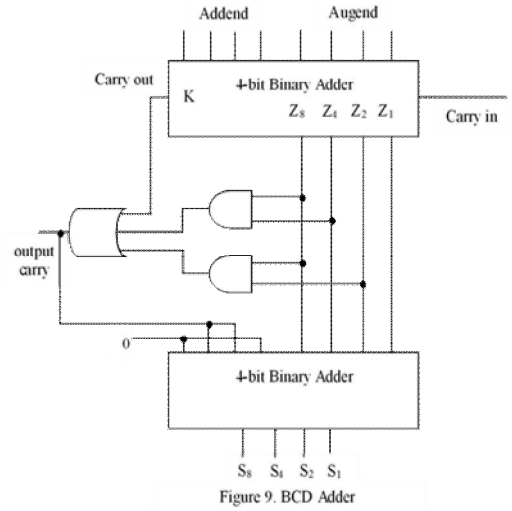

Figure 9. BCD Adder

A conventional BCD adder has the major portion as 4-bit binary adder is cascade with other 4-bit binary adder. The next portion detection unit is built by using two AND gates and one OR gate. The last portion correction unit adds 0 to the binary number if the binary result is less than 9 and adds 6 to the binary result if it is more than 9.Binary full adder is an elementary circuit for designing binary arithmetic units such as n-bit binary adder, subtractor and multiplier. Like this a BCD adder/subtractor forms as a basic circuit for designing BCD arithmetic units such as BCD n-bit adder/subtractor.

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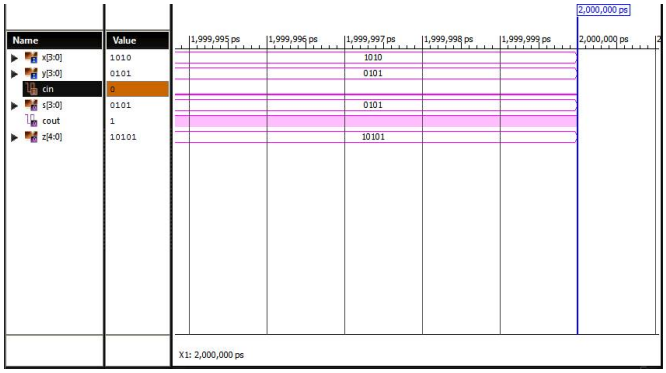

Fig 10. Simulation result of conventional BCD adder

C. EXISTING SYSTEM

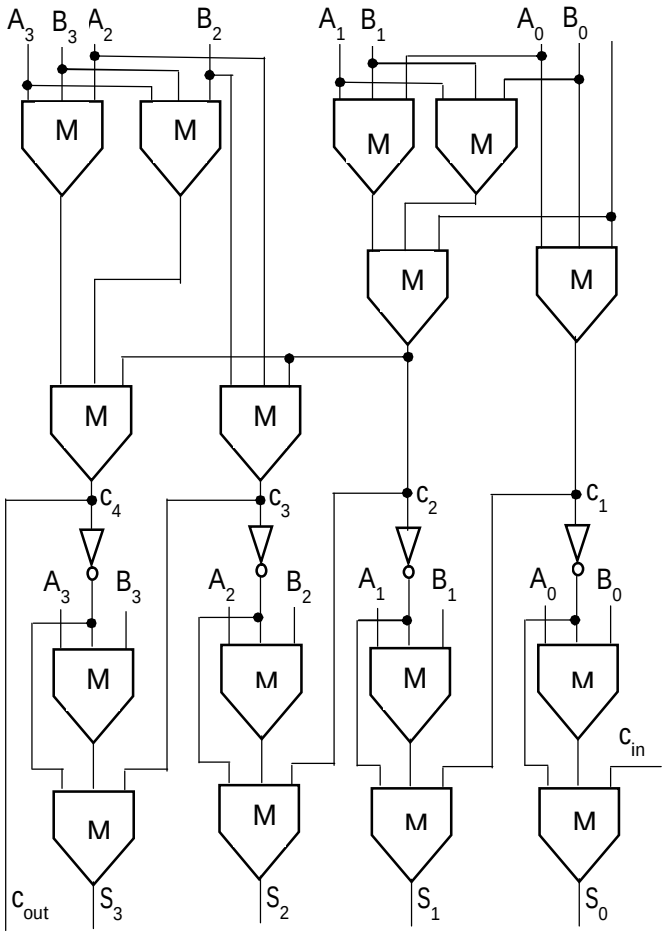

Fig 11. Existing system BCD adder schematic diagram

Efficient QCA-based applications have been verified for numerous binary and decimal arithmetic circuits, but major enhancements are still promising if the logic gates inherently obtainable within the QCA technology are rapidly exploited. This offers a new method to design QCA-based BCD adders. The QCA circuit purposed a design for the adder module which forms the basic unit for the BCD adder. The new circuit shows a critical computational path of 5 MGs and

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1 inverter, which is 1 MG smaller than the orthodox Ripple Carry Adder. The new adder module uses only 16 MGs and 4 inverters; this made this design to overcome the drawback of orthodox 4-bit Carry Look ahead Adder, which is designed using 43MGs and 4 inverters. This design method has been offered and proven to achieve efficient QCA based implementations of decimal adders. This existing structure is based on a new algorithm that requires only three majority gates and two inverters for the QCA addition. It is noted that the bit serial QCA adder uses a variant of the one-bit QCA adder. By connecting n one-bit QCA adders, n obtain an efficient n-bit QCA adder with CLA.

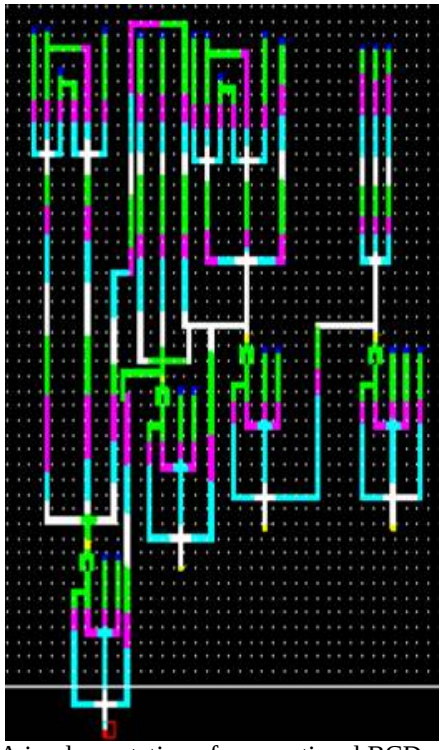

Fig 12. QCA implementation of conventional BCD adder design

IV. PROPOSED SYSTEM

A. APPROXIMATE ADDER

An approximate adder is executed with quantum dot cellular automata (QCA). In numerous fields the adder plays a vital role but in maximum of the field the accuracy is not in worry. So a different adder is projected called approximate adder in quantum dot cellular automata (QCA). This suggested adder is used to decrease the circuit complexity and time delay with low error rate. The circuit complexity reduction is attained by dropping the majority gate in the adder circuit. The process of QCA circuits is simulated and proved using QCADesigner bistable vector simulation. In approximate adder design, the carry output is attained by the one majority gate through an input of A, B and C. The sum is gained from the inverted output of carry. The number of majority gate used for this design is 1. The function of the sum and the carry of an approximate adder are specified by,

Cout = m (a, b, c);

Sum = $\hat{C}$out

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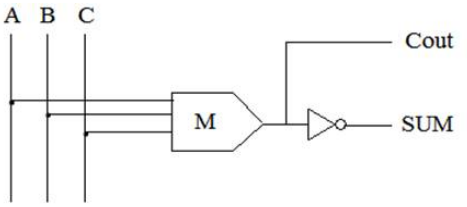

Fig 13. Approximate adder schematic diagram

TABLE II. TRUTH TABLE OF APPROXIMATE ADDER

Input			Original full adder output		Approximate adder output	
a	B	c_{in}	sum	c_{out}	Sum	c_{out}
0	0	0	0	0	1×	0
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	1	0	1
1	1	0	0	1	0	1
1	1	1	1	1	0×	1

For this approximate design, a technic would be used to evaluate the approximation with regard to the exact result; the supposed error distance has been suggested as form of value for inaccurate calculation. This design is implemented in QCA its layout is shown in figure 14.

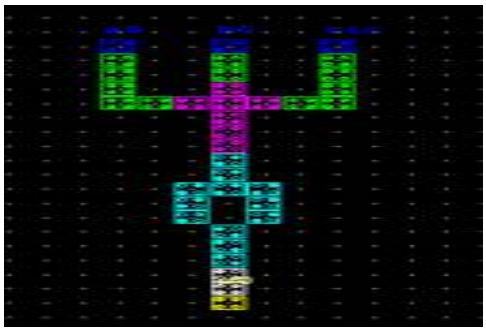

Fig 14. QCA implementation of approximate adder

In this layout indigo color QCA cells indicate the inputs to the circuit and the yellow color indicates the output from the circuit. Other different colors are used to indicate the different clock zones as green color for clock zone 0, rose color for clock zone 1, light turquoise color for clock zone 2, white color for clock zone 3.

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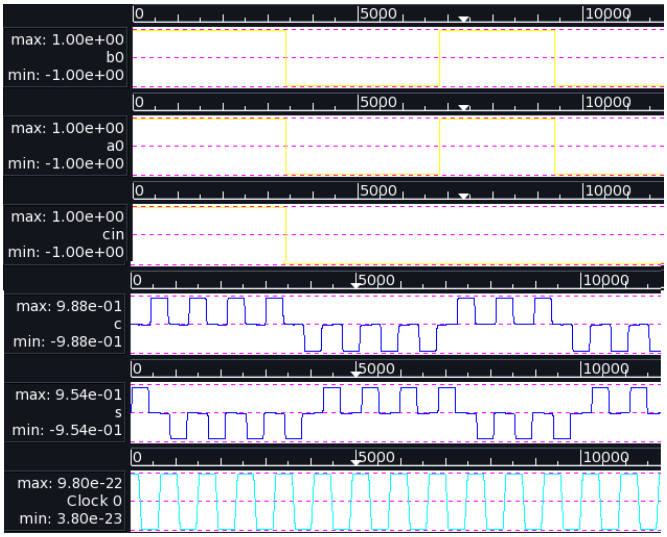

Fig 15. Simulation result of approximate adder

B. DECIMAL ADDER USING APPROXIMATE ADDER

New decimal adder is designed on the basics of approximate adder.

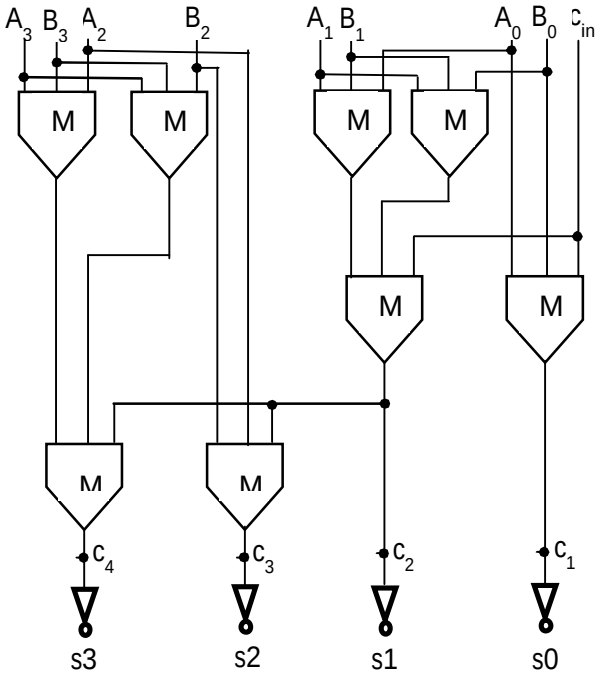

Fig 16. Schematic diagram of proposed system

Single bit approximate adder is cascaded to form four bit adder which function is equal to a decimal adder. By using majority gate reduction theorem number of majority gate is reduced. For conventional decimal adder it need up to 1512 cells were used but for the proposed decimal adder 994 cells only used. The number of majority gate count also reduced by replacing normal conventional adder by approximate adder.

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Sixteen majority gate and four invertors were used in existing system. It was reduced to half the number of majority gate in the proposed design. Eight majority gate and four invertors were used in the proposed system.

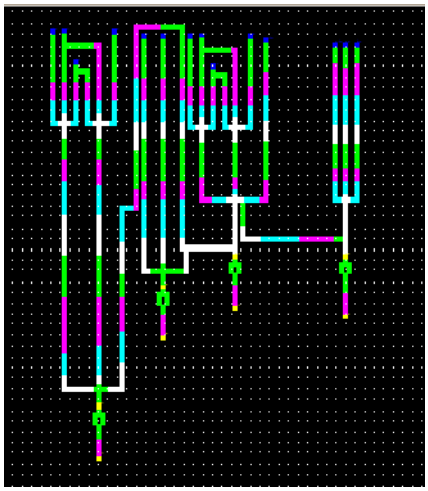

Fig 17. QCA implementation of proposed system

V. PERFORMANCE ANALYSIS

Table III discusses about the performance analysis of existing and proposed systems.

TABLE III. PERFORMANCE ANALYSIS

S.no	Parameter	Existing	Proposed
1	Majority gate count	16	8
2	Cells count	1512	994
3	Area	4.44μm^2	3.38μm^2

VI. CONCLUSION

In this proposed, Approximate Adder has been design and simulated using the QCA Designer tool for the four-bit adder has been presented that reduces the number of majority gates compared to the conventional full adder. The proposed Approximate Adder produces the accurate output rather than the exact output with low error rate. When the errors introduced by these approximations were reflected at a high level like signal processing algorithms, the impact on output quality was very little. A decrease in the number of majority cells helped in reducing overall area when number of bits increases.

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