ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 5, May 2017

Simulation of 11-level Inverter with Reduced Number of Power Switches for R and RL load

Vasudevamurthy.S[1], Somashekara. G[2]

Associate professor, Dept. of E&EE, Dr. AIT, Bengaluru, Karnataka, India[1]

PG student [EPE], Dept. of E&EE, Dr. AIT, Bengaluru, Karnataka, India[2]

ABSTRACT: This paper proposes simulation of a11-level inverter using reduced number of power switches. It can feed maximum power of input PV array to the connected load with high quality output current with THD of only 0.45%. The level shifted modulation technique is used for the proposed 11-level inverter to generate switching pulses. The conventional multilevel inverter(MLI) has very complicated inverter control and more expensive. Absolute aim of this project is to reduce the number of switches required. The topology consists of five input capacitors and only one DC source. The less number of power components decreases the size of the inverter, weight, circuit complexity and also reduces the cost. Another advantage of this topology is that it increases the efficiency of the system and decreases the switching losses. The simulation is done in MATLAB/SIMULINK R2011b for 1000W system for R and RL load and THD is also obtained.

KEYWORDS: Multilevel inverter(MLI), Multilevel converter(MLC), Neutral point clamped(NPC), Flying capacitor(FC), Maximum Power Point Tracker(MPPT), Total Harmonic Distortion(THD).

I.INTRODUCTION

The multi-level inverter was first introduced in 1975. The three level converters was the first multi-level inverter introduced. A multi-level inverter is a static power electronics circuit that synthesizes stepped form of output voltage from several levels of input DC voltages. With an increasing number of levels in output voltage of an inverter, output waveform approaches to sinusoidal waveform. Renewable energy sources (RES) gain an importance in recent decades because they are pollution free, easily erectable, and limitless. Among RES, Photovoltaic systems are mostly used as they are light, clean and easily installable. To meet high voltage and power requirements, engineer's started developing the multilevel inverter concept and now it has been one of the extensively used inverter in the area of power research.

Multilevel converters (MLCs) were invented with the specific aim of overcoming the voltage limit capability of semiconductor devices. These converters offer numerous advantages compared with the two-level (2L) converter counterpart. The features include good power quality, low switching losses, high voltage capability, and low *dV/dt.*These properties and the advancement in semiconductortechnology make MLCs attractive for high-powerapplications[1]. A very popular method in industrial applications is the classic carrier-based sinusoidal PWM (SPWM) that uses the phase-shifting technique to reduce the harmonics in the load voltage[2,3]. In order to bring the switching component stresses back to acceptable values, new topologies of multilevel converters have been emerging, including five-level topologies[4].

The classic multilevel topologies include the neutral point clamped (NPC), flying capacitor (FC), and the cascaded H-bridge (CHB). Diode clamped MLI require large number of clamping diodes as the level increases .In FC MLI, Switching utilization and efficiency are poor and also it requires large number of capacitors as the level increases and cost is also high. Cascaded H-bridge are mostly preferred for high power applications as the regulation of the DC bus is simple. But it requires separate dc sources and also the complexity of the structure increases as the level predominantly increase. In all

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these cases the basic target was to generate high quality power output with minimum number of power devices and easier control. The drawback of the 5-level Active Neutral Point Clamped(5L-ANPC) is that the switch voltage ratings are different in different converter branches[5].

The disadvantages of FC-ANPC are high number of switches, series connection of high voltage switches, and poor loss distribution[6]. A new coupled inductor based 9-level inverter has only 10 power switches, 4 power diodes and one high frequency coupled inductor to generate nine voltage levels. It improves system efficiency and reduces the size of the system[7]. The use of a coupled split-wound inductor has been described to allow interleaved PWM switching of the upper and lower switches in an inverter leg. The switch control dead times can be eliminated, helping to improve the quality of the PWM voltage generation and increasing the maximum potential output voltage and switching frequency[8].The transformer-less topologies reduce power losses and cost, the principal problem of such topologies is caused by the parasitic capacitance between ground and PV cell [9]. A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10kW [10]. The Renewable sources include solar, wind, biomass, hydro,etc . One of the sources are interfaced into the power production which produces increased reliability, security, flexibility, low power losses and increased power quality.
This paper deals with how higher level of output voltage is achieved for a new 11-level inverter topology using level shifted modulation technique. This topology has the advantages of its reduced number of switching devices,five input dc capacitors and only one dc source compared to the conventional inverter topology for the same levels. The modes of operations are outlined for 11-levelinverter. Simulation of proposed inverter topology is carried out in MATLAB/SIMULINK software.

II.BASIC SYSTEM MODEL

The basic system model consists of four blocks namely, PV array block, DC-DC converter block, Multi-level inverter block and lastly load section. This topologyuses a two stage power conversion process as shown in Fig. 1. DC-DC converter is used to boost the low voltage input PV source and as well as MPPT of PV source. Then with the use of MLI nice quality of power can fed in to the load or grid.

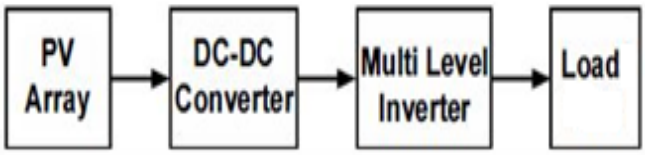

Fig. 1 System block diagram

III.PROPOSED 11-LEVEL INVERTER TOPOLOGY

The proposed topology has 9 power switches as shown in Fig.2. There is only one dc source which is split into five with the help of five dc link capacitors (C_1-C_5). 11 different voltage levels which can be produced by the inverter are $\pm V_{dc}$, $\pm 4V_{dc}/5$, $\pm 3V_{dc}/5$, $\pm 2V_{dc}/5$, $\pm V_{dc}/5$ and zero as shown in Fig. 3.

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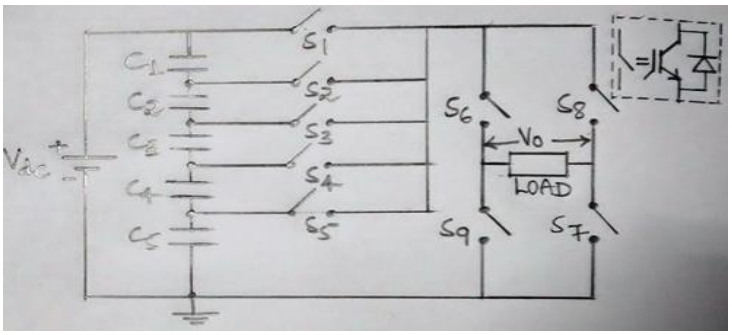

Fig. 2 Proposed 11-level inverter topology

A. STATES OF OPERATIONS

There are 11 different switching states, which can be used to generate eleven output voltage levels as shown in Table 1.The circuit operates in accordance with switching pattern given in Table 1.

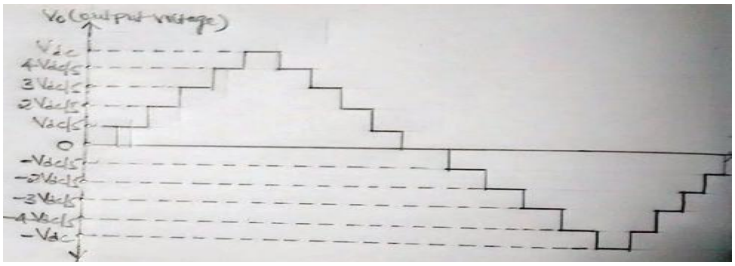

Fig. 3 Proposed topology output voltage waveform

Table 1 Switching pattern for 11-levelinverter

States	Switching State									V
	S1	S2	S3	S4	S5	S6	S7	S8	S9	
1	1	0	0	0	0	1	1	0	0	V_{dc}
2	0	1	0	0	0	1	1	0	0	$4V_{dc}/5$
3	0	0	1	0	0	1	1	0	0	$3V_{dc}/5$
4	0	0	0	1	0	1	1	0	0	$2V_{dc}/5$
5	0	0	0	0	1	1	1	0	0	$V_{dc}/5$
6	0	0	0	0	0	0	0	0	0	0
7	0	0	0	0	1	0	0	1	1	$-V_{dc}/5$
8	0	0	0	1	0	0	0	1	1	$-2V_{dc}/5$

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9	0	0	1	0	0	0	0	1	1	$-3V_{dc}/5$
10	0	1	0	0	0	0	0	1	1	$-4V_{dc}/5$
11	1	0	0	0	0	0	0	1	1	$-V_{dc}$

1) *MODE-1*:In this modepower switches S1, S6 and S7 are turned on simultaneously and the remaining switches are kept in OFF condition. The output voltage across Load is $V_o = V_{dc}$.

2) *MODE-2:*In this mode power switches S2, S6 and S7 are turned on simultaneously and the remaining switches are kept in OFF condition. The output voltage across Load is $V_o = 4V_{dc}/5$.

3) *MODE-3:*In this mode power switches S3, S6 and S7 are turned on simultaneously and the remaining switches are kept in OFF condition. The output voltage across Load is $V_o = 3V_{dc}/5$.

4) *MODE-4:*In this mode power switches S4, S6 and S7 are turned on simultaneously and the remaining switches are kept in OFF condition. The output voltage across Load is $V_o = 2V_{dc}/5$.

5) *MODE-5:*In this mode power switches S5, S6 and S7 are turned on simultaneously and the remaining switches are kept in OFF condition. The output voltage across Load is $V_o = V_{dc}/5$.

*6) MODE-6:*This mode generates an output voltage of zero in both positive and negative half cycle.

7) *MODE-7:*In this mode power switches S5, S8 and S9 are turned on at a time and the remaining switches are kept in OFF condition. The output voltage across Load is $V_o = -V_{dc}/5$.

8) *MODE-8:*In this mode power switches S4, S8 and S9 are turned on at a time and the remaining switches are kept in OFF condition. The output voltage across Load is $V_o = -2V_{dc}/5$.

9) *MODE-9:* In this mode power switches S3, S8 and S9are turned on at a time and the remaining switches are kept in OFF condition. The output voltage across Load is $V_o = -3V_{dc}/5$.

10) *MODE-10:* In this mode power switches S2, S8 and S9 are turned on at a time and the remaining switches are kept in OFF condition. The output voltage across Load is $V_o = -4V_{dc}/5$.

11) *MODE-1*: In this mode power switches S1, S8 and S9 are turned on at a time and the remaining switches are kept in OFF condition. The output voltage across Load is $V_o = -V_{dc}$.

The switching pattern as discussed in Mode 1 to Mode 6can be used to generatepositive output voltage levels. Similarly Mode 7 to Mode 11 can be used to generate negative output voltage levels.

III.CONTROL STRATEGY

The level shifted modulation technique is used for the proposed 11-level inverter to produce switching pulses. Single modulating wave V_m is used to compare with different carrier waves to generate switching pulses in the positive half cycle.

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Similarly same modulating wave V_m is used to compare with different carrier waves to generate switching pulses in negative half cycle. The main focus of the implemented control strategy is to extract maximum power from the PV source and fed it to the connected load. The control strategy for the proposed inverter is shown in Fig. 4.

The control strategy operates in three different steps:

- The MPP voltage and currents computation.
- Deciding the modulating signal phase and amplitude
- Switching pulses generation.

PI controller is a combination of Proportional and Integral controllers. The forced oscillation and steady state error will be eliminated by this and they are most commonly used in industries.Tuning of the PI controller is a very important task.Fine tuning is necessary to obtain appropriate output.The overall simplicity and efficiency of the PV system depends on the MPPT technique employed.

PV voltage and current are sensed and the MPP voltage(V_{mpp}) and currents(I_{mpp}) are calculated through a Purturb& Observe algorithm in order to extract maximum power from the solar PV module. The reference voltage V_{mpp} is compared with the actual voltage of PV module V_{PV} to generate error signal(e_m). This error $e_m$is fed to the PI controller, then required peak of the load current (i_L^*) is obtained. The obtained i_L^* is used to calculate the reference current for the second step(for generating modulating signal). In the second step, the PLL output is multiplied with peak of the loadcurrent(i_L^*) in order to calculate reference current(i_r^*). By comparing the reference current (i_r^*) and the load current (i_r) the error signal (e_c) is generated. This error signal is passed through the PR controller to generate the modulating signal (m_a). At last, the desired switching pulses is generated by using the resulting modulating signal.

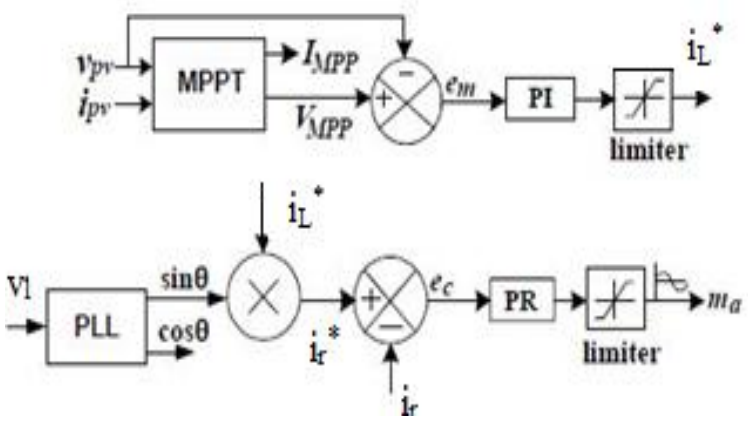

Fig. 4 Control strategy for the proposed 11-level inverter.

The values of PI controller are K_P=0.1 and K_i=10. The Load or output Current is controlled by using PR controller. The obtained PR controller is given by $s^2+314.1s+98596/s^2+157s+98596$.

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V.SIMULATION RESULTS

The analysis of proposed 11-level inverter is carried out in MATLAB/SIMULINK software. Here MOSFETs are used to work as switches in place of S1 to S9. Scopes are used to measure output voltage, output current and voltage across input capacitors. Fig.1 shows the basic system model. Fig. 2 shows the proposed 11-level inverter topology. Fig. 3 shows the output voltage waveform of proposed topology. Fig.4shows the control strategy for the proposed inverter. Table 1 shows the switching pattern for the proposed inverter. Table 2shows model specifications of the proposed 11-level inverter. Fig. 5 and Fig. 6 shows the Simulink model of 11-level inverter with R and RL load respectively. The switching pulses and output voltage and output current waveforms for R load asshown in Fig. 7 and Fig. 8 respectively. Output voltage and current waveforms with RL load as shown in fig.9. Fig. 10 shows input capacitor(C_1-C_5) voltage waveforms. The THD also obtained by simulating main circuit in MATLAB. Fig.11 represents the %THD present in the output current waveform of the proposed inverter.

Table 2 Model specifications

1	PV source voltage: V_{PV}	400V
2	Power rating of the system	1000W
3	%THD	0.45
4	Input capacitor: $C_1 - C_5$	330mF
5	Carrier wave frequency	3kHz
6	Inductance L_1	1mH
7	Output voltage: V_{DC}	380V

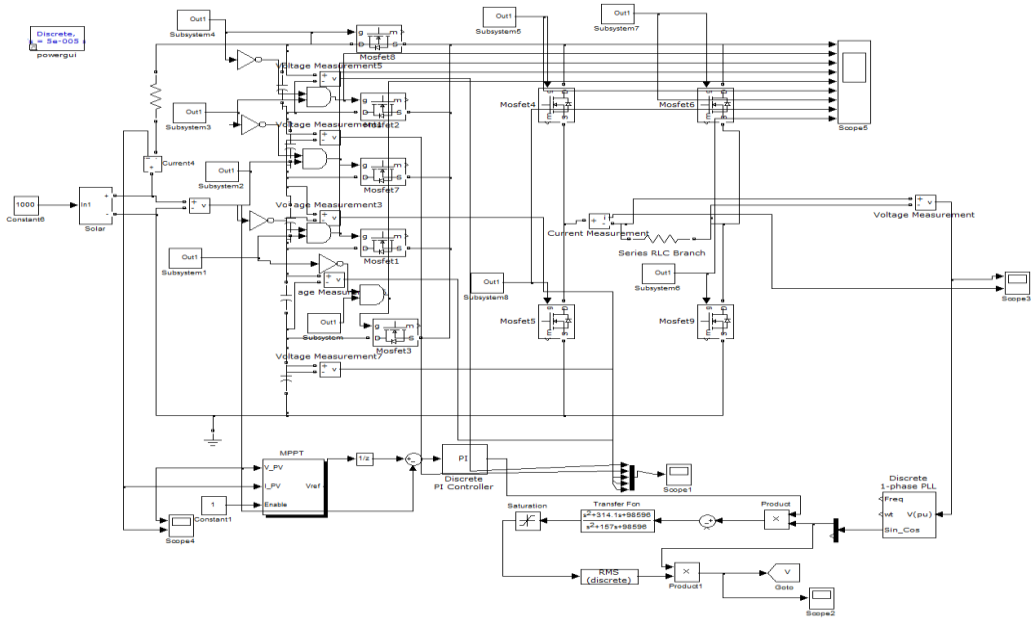

Fig. 5 Simulink model of 11-level inverter with R load

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Fig. 5 shows Simulink model of 11-level multi-level inverter with R load.

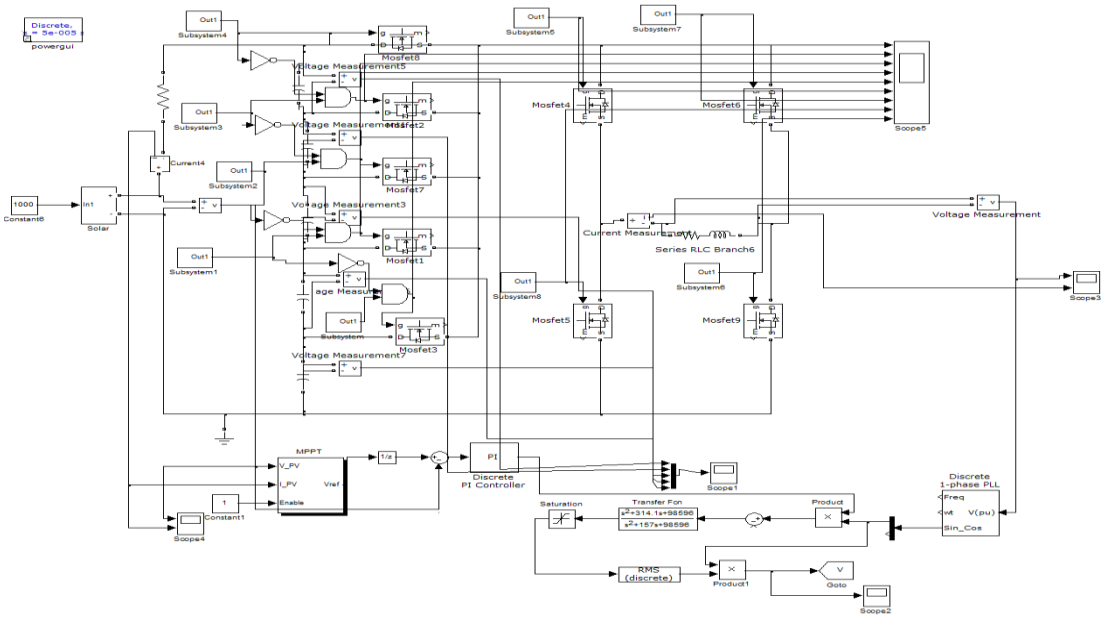

Fig. 6 Simulink model of 11-level inverter with RL load

Fig. 6 shows Simulink model of 11-level multi-level inverter with RL load.

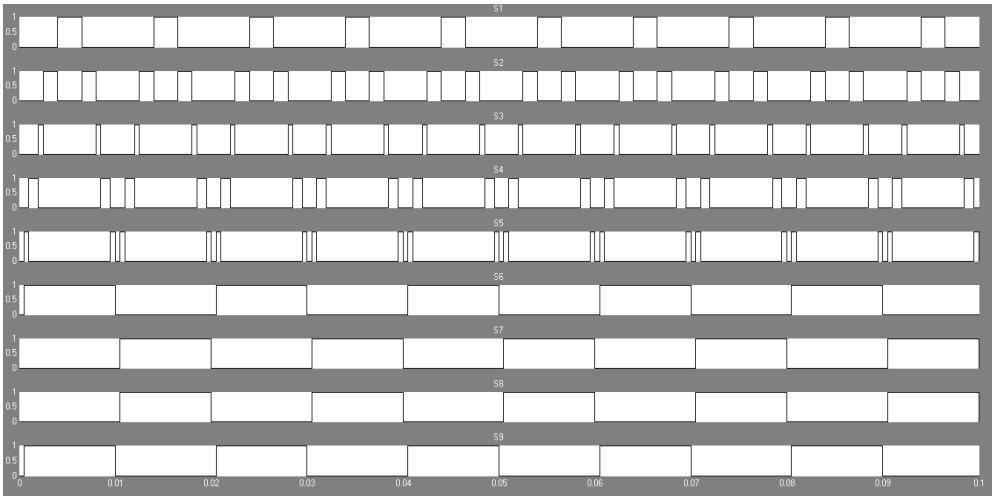

Fig. 7 Switching pattern of switches S1 to S10

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Fig. 7 shows switching pulses of power switches S1 to S10.

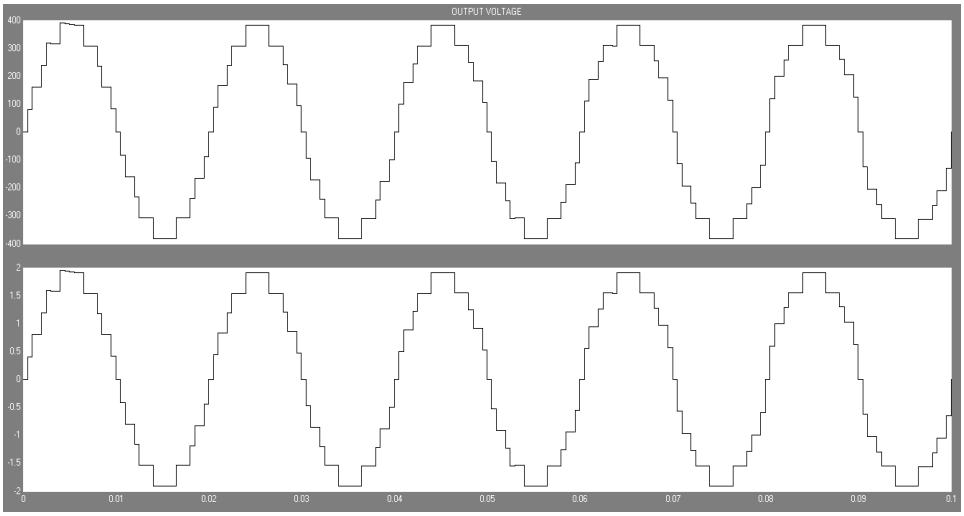

Fig. 8 Output voltage and Current waveforms of 11-level inverter with R load

In the fig. 8, it shows the graph of Time(s) VsOutput voltage(V)and Current(A) waveforms of 11-level inverter with R load.

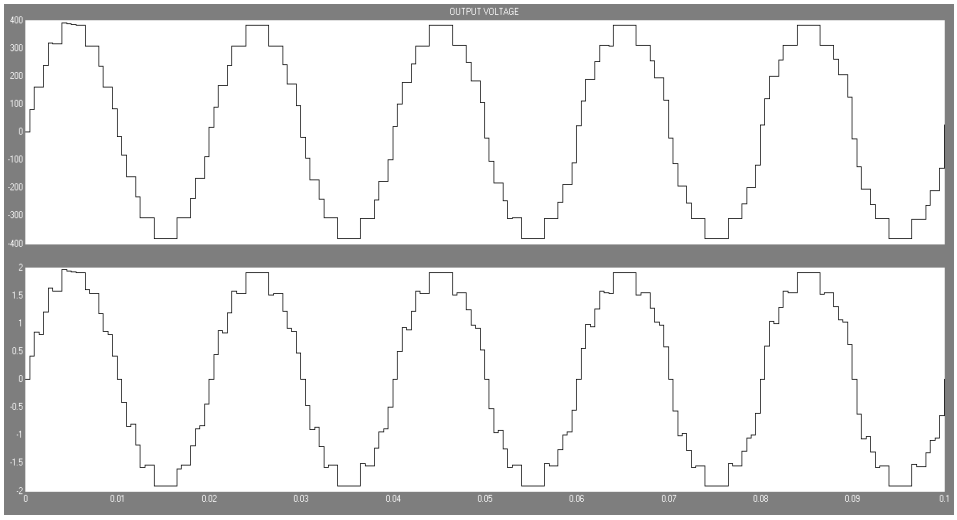

Fig. 9 Outputvoltage and current waveforms of 11-level inverter with RL load

In the fig. 9, it shows the graph of Time(s) VsOutput voltage(V)and Current(A) waveforms of 11-level inverter with RL load.

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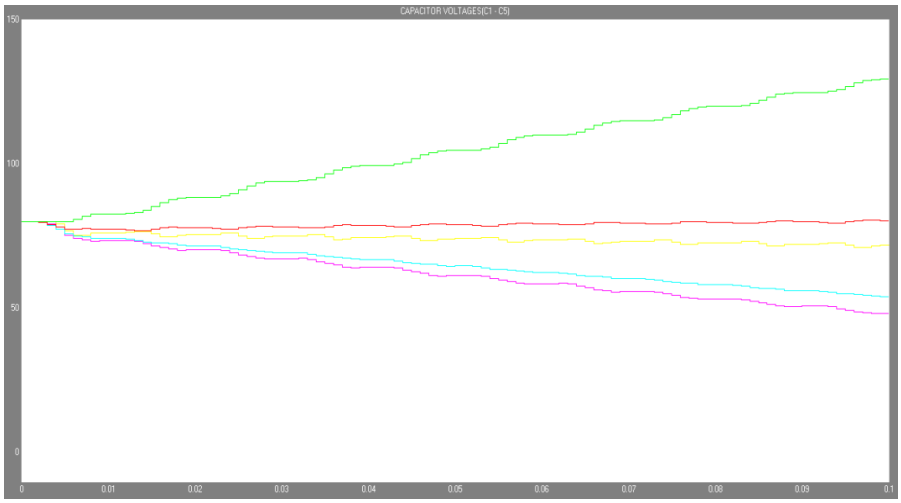

Fig. 10 Input capacitors(C1-C5) voltage waveforms

In the fig. 10, it shows the graph of Time(s) Vscapacitor voltage waveforms of 11-level inverter.

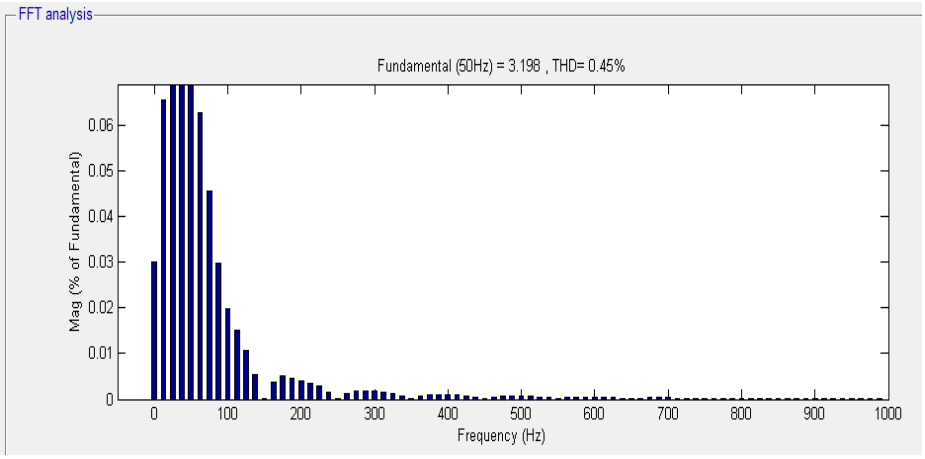

Fig. 11 THD analysis of output current

In the fig. 11, it shows the graph of Frequency(Hz) VsMagnitude waveforms of 11-level inverter. The THD obtained with quality obtained current is only 0.45%.

VI.CONCLUSION

Simulation of 11-level inverter with R and RL loadis carried out in MATLAB Simulink R2011b. The number of switching devices required is very less compared to the other 11-level multi-level inverters.It can feed maximum power of input PV array to the connected load with high quality output current with THD of only 0.45%. As the number of switches is reduced, the overall cost, size, driver circuits required are reduced. So this topology is cost-effective. The less number of

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power components also results in reduced switching losses, increased reliability and higher efficiency.This topology also produces Easier inverter control with lower harmonics.

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