ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 5, May 2017

Coupled-Inductor and Cascaded H-bridge Based Reduced Switch Multilevel Inverter

Rashmy Deepak [1], Sushmitha.B [2]

Assistant Professor, Dept. of EEE, RNSIT, Bangalore, Karnataka, India[1]

PG Student [Power Electronics], Dept. of EEE, RNSIT, Bangalore, Karnataka, India[2]

ABSTRACT: This paper proposes a new hybrid coupled-inductor and cascaded H-bridge (CHB) multilevel inverter. In the proposed topology, one 5-level coupled inductor inverter is cascaded with several H-bridges so that a hybrid multilevel inverter is obtained. The main aim is to use the advantages of both topologies (coupled-inductor and CHB) in one structure. In the 5-level coupled-inductor inverter, the current of switches is reduced to half of the output current making it possible to use low -current switches in this part. In the CHB part, the voltage of the inverter is divided on several bridges so that low-voltage switches can be used. Also, the proposed topology gives higher number of voltage levels with lower number of switches. For example, the proposed 9-level inverter uses only 10 switches while the CHB multilevel inverter uses 16 switches for the same number of voltage levels. A suitable control method is also presented for the proposed topology. Using this control method, only the low-current switches operate with high frequency and the other switches operate with fundamental frequency. This results in reduced stresses on the switches. The simulation results of the proposed 9-level inverter are presented to verify the proposed topology and control method.

KEYWORDS: Coupled-inductor; cascaded multilevel inverter; Hybrid multilevel inverter.

I.INTRODUCTION

The general function of a multilevel inverter is to synthesize a desired output voltage from several levels of dc voltages as inputs. Multilevel inverters receive more and more attention from both academy and industry. This is because of some inherent advantageous features such as ability to operate in higher voltage/power condition and improved quality of the output waveform and better electromagnetic compatibility. The concept of multilevel inverter is to produce a staircase output voltage using the available dc voltage sources. The higher the number of voltage level the better the output voltage quality. Three main topologies of multilevel inverters include cascaded H-bridge (CHB) multilevel inverter, the flying capacitor (FC) multilevel inverter and the neutral point clamped (NPC) multilevel inverter.

Cascaded multilevel inverters are based on a series connection of several single-phase inverters. This structure is capable of reaching medium output voltage levels using only standard low-voltage mature technology components. Therefore, the cascaded multilevel inverters are popular and easy to extend to desired number of voltage levels and operating voltage. The simple structure and operating principle has results in introducing many different topologies for cascaded multilevel inverters. The cascaded multilevel inverters provide an interesting solution to overcome limitation in operating voltage of the inverters. However, in these kind of multilevel inverters current of all of switches are equal to the output current. Therefore, application of these inverters for higher current loads may be challenging. The parallel inverters have been presented as a solution for high-current applications. The parallel inverters are based on inter-phase transformers or current-sharing inductors. These inverters can also produce multilevel pulse width modulated (PWM) output voltages. However, the main problem is that the operation of the parallel inverters depends on the device parameter variations.

A small variations in the switch turn-off times and on -state voltage drops can create dc current drifts and circulating currents. A balanced symmetrical operation of parallel connected inverters can be obtained by using interleaved PWM controls. In both parallel inverter and coupled-inductor inverter the output voltage is not increased. Beside the parallel inverters, the split-wound coupled-inductor based inverters have been presented in the literature. These topologies use

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 5, May 2017

lower number of components and have better performance. In the 3-level three-phase six-switch coupled-inductor inverter has been presented and its application as a motor drive. The significant advantage of this topology is that the requirement for dead-time to avoid shoot-through current is eliminated since the split-wound coupled inductor is in series with the upper and lower switches. Thus, traditional adverse effects of dead-time are avoided. In addition, by using a proper PWM switching scheme, the effective switching frequency of the PWM output voltages can be doubled. The coupled-inductor H-bridge inverter generated 5-level output voltage. In comparison with the conventional multilevel inverters (such as CHB multilevel inverters) the coupled- inductor based topologies have attracted less attention and the presented works in this relation have focused on special cases (very well-known topologies and limited number of voltage levels). Therefore, it seems that this field can be investigated further by introducing new topologies and control methods. In this paper, a new hybrid coupled-inductor and cascaded multilevel inverter is proposed.

In the proposed topology, unlike other coupled-inductor based multilevel topologies, the output voltage can be also increased. In fact, the proposed topology uses the advantages of both the cascaded and the coupled-inductor inverters. In section II, the proposed 9-leve inverter is presented along with its switching table and modulation method. The proposed modulation method is in a way that only the low-current switches operate with high frequency and the higher-current switches operate with fundamental frequency. Therefore, the stresses of the switches are reduced. At the end of this section, extension of the proposed topology to higher number of voltage levels is discussed. Section III presents the simulation results of the proposed 9-level inverter obtained from the PSCAD/EMTDC software to verify its performance and control.

II. THE PROPOSED HYBRID MULTILEVEL INVERTER TOPOLOGY

Fig. 1 shows the proposed 9- level hybrid cascaded coupled-inductor inverter. It consists of two parts. The first part is a 5-level coupled-inductor inverter. This part has six power electronic switches ($S_{1,1}$, $S_{6,1}$), a coupled-inductor. This 5-level inverter is cascaded with an H-bridge. Due to usage of coupled-inductor, the current through the switches $S_{1,1}$, $S_{4,1}$ is half of the output current. However, the switches $S_{5,1}$, $S_{6,1}$ and $S_{1,2}$, $S_{4,2}$ operate with the current rating equal to the output current.

For the 9-level topology shown in Fig. 1, the following equations can be written:

$$i_o = i_1 + i_2 \qquad (1)$$

Using proper switching method, the current through the branches of the coupled-inductor are the same. Therefore, using (1) the following relations can be written:

$$i_o = i_1 = i_2/2 \qquad (2)$$

Equation (2) demonstrates that the current through the switches $S_{1,1}$, $S_{4,1}$ is half of the output current.

In order to explain the operation principle of the proposed topology, its switching states are shown in Table I in positive half-cycle. For the negative half-cycle, the switching states can be obtained by simply replacing each switch with its complementary operated switch. However, they are not shown in the table to avoid the table to be too long. Considering the contents of the table, it is obvious that in all of the positive voltage levels the switch $S_{6,1}$ is turned on. In the zero voltage level, both the switches $S_{5,1}$ and $S_{6,1}$ can be turned on. However, in order to make the control easy it is better to turn on the switch $S_{6,1}$ during the positive half-cycle. The switch $S_{5,1}$ is also turned on during the negative half-cycle. In other words, these switches operate in fundamental frequency even the PWM method is used to control the inverter.

Considering that the switches $S_{5,1}$ and $S_{6,1}$ operate with full output current, their switching with fundamental frequency help to reduce switching stresses. In order to generate the desired output voltage, different modulation method can be used. It is important to note that the coupled-inductor inverter should use high-frequency PWM method. Otherwise, if the fundamental frequency modulation is used the current through the coupled-inductor branches will grow up in unstable form. Moreover, the switches in the coupled-inductor inverter operate with lower current and therefore this part can be modulated with high frequency. On the other hand, the switches of the H-bridge inverter ($S_{1,2}$, $S_{4,2}$)

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 5, May 2017

operate with full output current and therefore, it is better to use fundamental frequency modulation for these switches. In this way, their stresses can be reduced. In the proposed method for modulation of the 9-level inverter, the switches $S_{1,1}$, $S_{4,1}$ are controlled by the carrier based method. The modulation method of the coupled-inductor part of the proposed 9-level inverter is shown in Fig. 2.

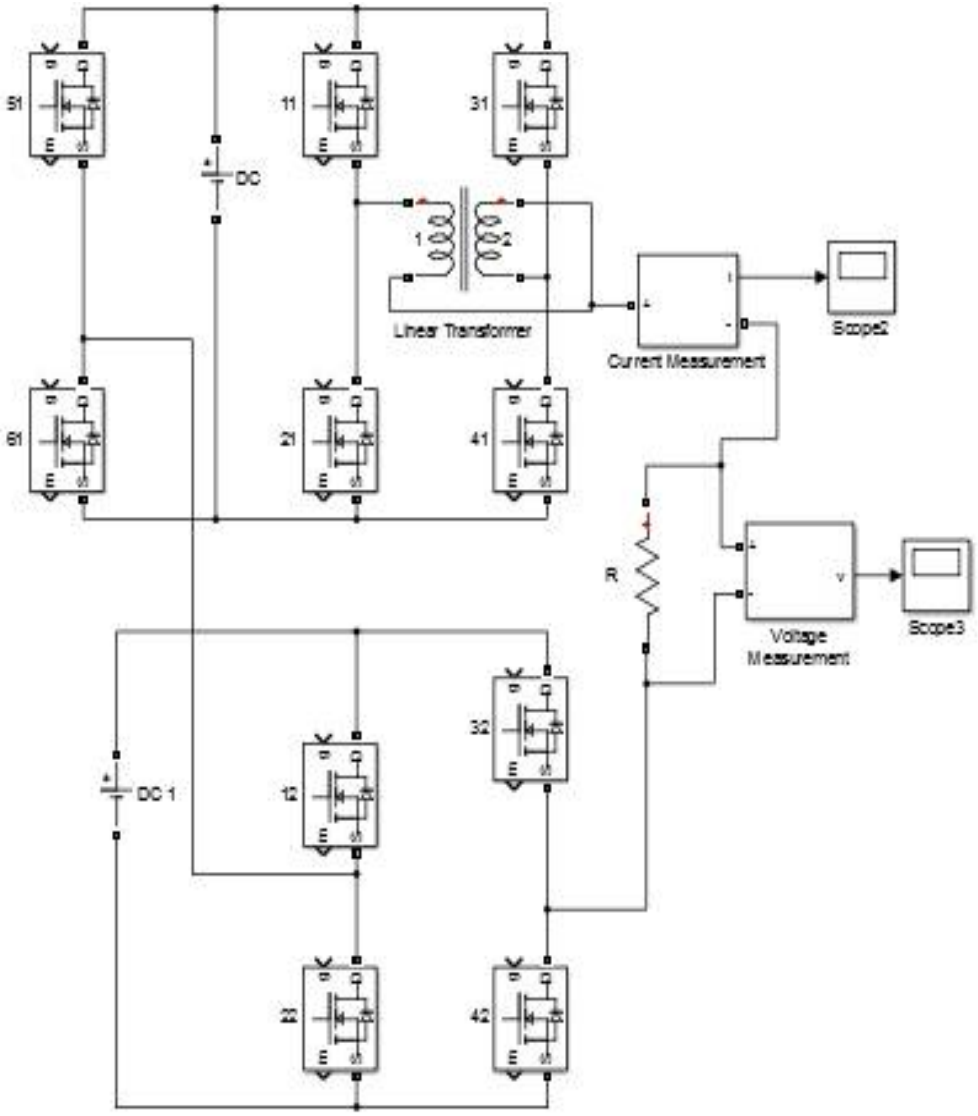

Fig. 1: The proposed 9-level hybrid cascaded coupled-inductor inverter

As the figure shows, the modified reference waveform is compared with two high-frequency triangular carrier waveforms to produce the switching pulses for the switches $S_{1,1}$, $S_{4,1}$. As motioned before, the switch 6,1 *S* is turned on during the positive half-cycle and the switch $S_{5,1}$ is turned on during the negative half-cycle. Supposing that the reference output voltage is $v_{o\ ,ref}$, the following equation can be written:

$$v_{o\ ,\ ref} = v_{o\ ,1,\ ref} + v_{o\ ,2,ref}$$

where, $v_{o\ ,1,ref}$ and $v_{o\ ,2,ref}$ are the reference output voltage of the coupled-inductor and H-bridge inverter, respectively.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 5, May 2017

TABLE I. SWITCHING STATES OF THE PROPOSED 9-LEVEL INVERTER IN POSITIVE HALF-CYCLE

LVL	V_O	$S_{1,1}$	$S_{2,1}$	$S_{3,1}$	$S_{4,1}$	$S_{5,1}$	$S_{6,1}$	$S_{1,2}$	$S_{2,2}$	$S_{3,2}$	$S_{4,2}$
0	0	0	1	0	1	0	1	1	0	1	0
1	V/2	1	0	0	1	0	1	1	0	1	0
2	V	1	0	1	0	0	1	1	0	1	0
3	3V/2	1	0	0	1	0	1	1	0	0	1
4	2V	1	0	1	0	0	1	1	0	0	1
5	3V/2	1	0	0	1	0	1	1	0	0	1
6	V	1	0	1	0	0	1	1	0	1	0
7	V2	1	0	0	1	0	1	1	0	1	0
8	0	1	0	1	0	1	0	0	1	0	1
9	-V/2	0	1	1	0	1	0	0	1	0	1
10	-V	0	1	0	1	1	0	0	1	0	1
11	-3V/2	0	1	1	0	1	0	0	1	1	0
12	-2V	0	1	0	1	1	0	0	1	1	0
13	-3V/2	0	1	1	0	1	0	0	1	1	0
14	-V	0	1	0	1	1	0	0	1	0	1
15	-V2	0	1	1	0	1	0	0	1	0	1
0	0	0	1	0	1	0	1	1	0	1	0

Fig. 2: Modulation method of the coupled-inductor part in the proposed 9-level inverter

Fig. 3 shows the typical waveforms of $v_{o,ref}$, $v_{o,2,ref}$, $v_{o,1,ref}$ and $v'_{o,1,ref}$. In comparison with the conventional CHB multilevel inverter, the proposed topology uses lower number of components. For the 9-level inverter, the proposed topology uses only 10 switches while the CHB multilevel inverter uses 16 switches for the same number of voltage levels. The proposed topology shows some advantages in comparison with the 5-level coupled-inductor inverter presented in [19]. the topology presented in [19] uses 8 switches for generating 5-level voltage while the proposed topology uses 10 switches (only two more switches) for generating 9-level voltage. Also, in the topology of [19] the maximum output voltage is limited to half of the value of the dc voltage source, but, in the proposed topology the maximum value of the output voltage is equal to sum of the dc voltage sources.

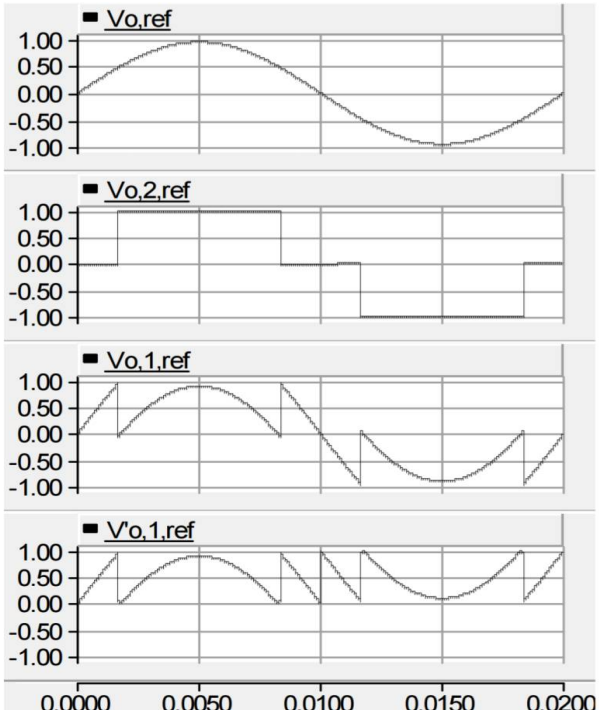

Fig. 3. Top to bottom: typical waveforms of *vo,ref* , *vo*,2,*ref* , *vo*,1,*ref* and *vo*′ ,1,*ref*

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 5, May 2017

However, both topologies are the same from the view point of current rating of the switches. In both of the topologies, four switches operate with half of the output current. The proposed topology can be extended to higher number of voltage levels by cascading more number of H-bridge inverter. Fig. 4 shows the extended topology. In this way, more number of output voltage levels is obtained leading to high-quality output waveform. Also, the operating voltage of the inverter can be increased by cascading several low-voltage bridges. For the proposed extended topology, the number of power-electronic switches (N_{switch}) and number of output voltage levels (N_{step}) can be written as follows, respectively:

$$N_{IGBT}=4m+2 \quad (8)$$
$$N_{STEP}=4m+1 \quad (9)$$

III.SIMULATION RESULTS

In order to verify the proposed topology and control method, the 9-level inverter based on the proposed topology has been simulated using PSCAD/EMTDC software and the results are presented and discussed. The inverter is designed to give output voltage of 110V RMS. Therefore, the value of each dc voltage source should be about 78V. The load is considered to be an inductive load with the resistance and inductance equal to 30Ω and 15mH, respectively. The frequency of carrier waveforms is considered to be 5kHz and the fundamental frequency of the output voltage is 50Hz. The self and mutual inductance of the coupled-inductor is 2mH and 1.9mH, respectively. Fig. 5 shows the output voltage of the* coupled- inductor part, output voltage of the H-bridge inverter and the total output voltage, from top to bottom, respectively. As the figure shows, the output voltage of the coupled-inductor part is a 5-level PWM voltage. Also, the output voltage of the H-bridge inverter is a 3-level stepped voltage with fundamental frequency. This shows that the switches of the H-bridge inverter operate in fundamental frequency. The total output voltage is in fact sum of the two mentioned voltages. As expected, the output voltage is a 9-level voltage without any overlap of voltage levels. Considering Fig. 5, the maximum value of the output voltage is equal to sum of values of the dc voltage sources. This shows full utilization of the dc voltage sources by the proposed topology. The perfect 9-level output voltage also shows successful operation of the proposed control method for the proposed topology.

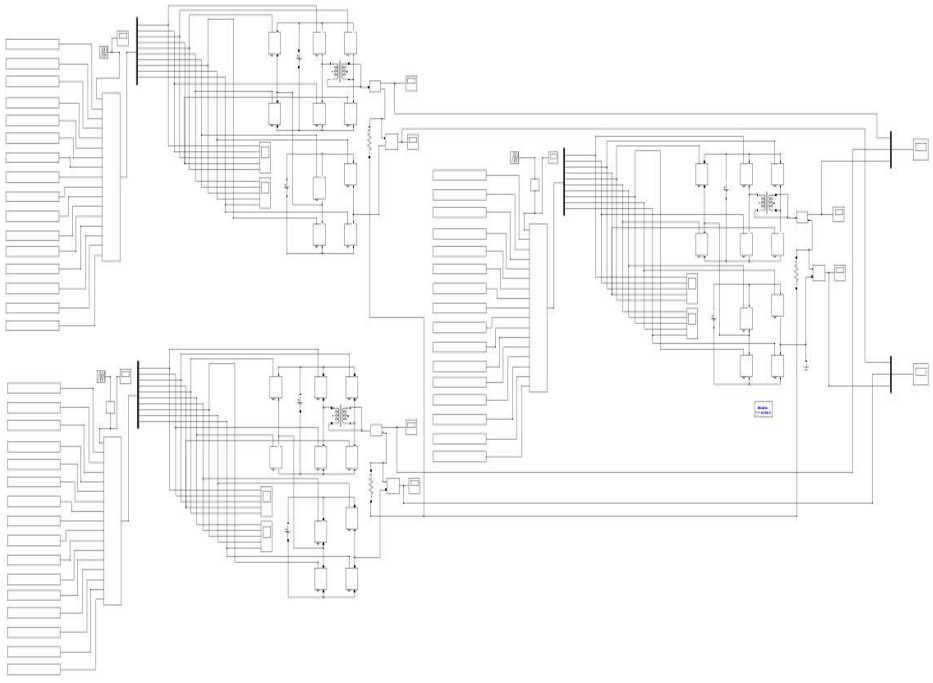

Fig. 4: Proposed extended topology of the hybrid cascaded coupled-inductor multilevel inverter

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 5, May 2017

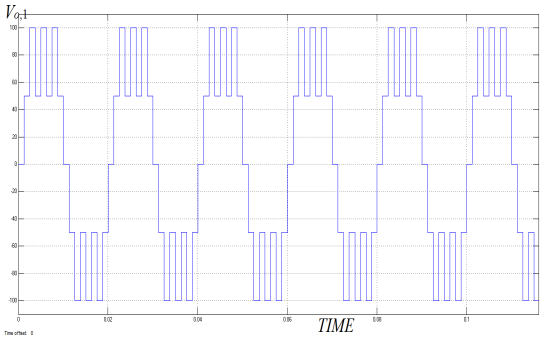

Fig: output voltage of the coupled-inductor part

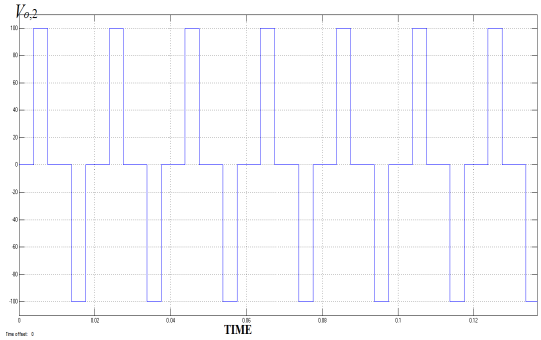

Fig: output voltage of the H-bridge part

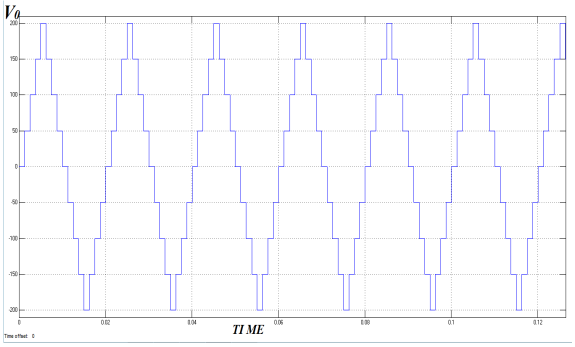

Fig: the total output voltage

Fig. 5: From top to bottom: output voltage of the coupled-inductor part, output voltage of the H-bridge part and the total output voltage

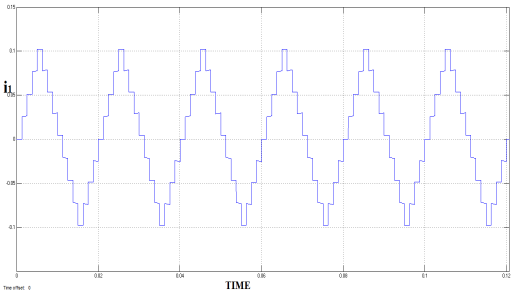

Fig: current of the right branch of the coupled inductor

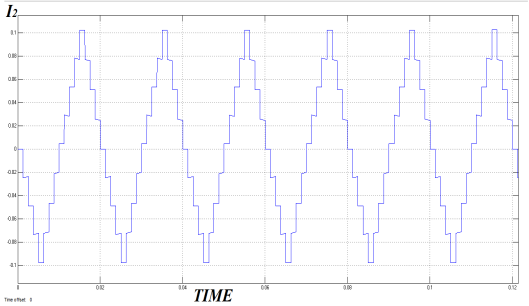

Fig: current of the left branch of the coupled-inductor

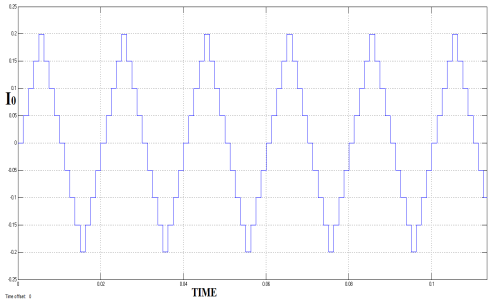

Fig: the total output current

Fig. 6: From top to bottom: output current of the right branch of the coupled inductor, output current of the left branch of the coupled-inductor and the total output current

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 5, May 2017

Top to bottom traces of Fig. 6 shows the current through the branches of the coupled-inductor and also the total output current, respectively. As the figure indicates, the current of the branches of the coupled-inductor are the same showing the proper switching method. Also, the current of the coupled-inductor is half of the output current demonstrating that the switches of the coupled-inductor part work with half of the output current. Moreover, the ripples on te output current are less than that of the coupled-inductor currents.

IV.CONCLUSION

This paper studied a new hybrid coupled-inductor cascaded multilevel inverter. In the proposed topology, a 5-level coupled-inductor inverter is cascaded with several H-bridges to form a hybrid multilevel inverter. The proposed topology owns the advantages of both coupled-inductor and cascaded multilevel inverters. In other words, it reduces the current ratings of some of the switches and also reduces the voltage rating of all of the switches (the general advantage of cascaded multilevel inverters) in comparison with the rated output voltage. For the proposed topology a suitable control method has been presented. The interesting point about the proposed topology in conjunction with the proposed control method is that only the low-current switches operate with high *frequency and the remaining switches operate with the fundamental frequency. This leads to reduced stresses on the switches. As the simulation results of the proposed 9-level inverter showed, the proposed topology can perfectly generate the expected voltage levels. Form the view point of the components, the comparison showed that for the 9-level case, the proposed topology uses only 10 switches while the 9-level CHB topology uses 16 switches. With only two switches less than the proposed topology, the number of voltage levels in the topology presented in [19] is only five.

REFERENCES

[1] J. E. Babaei, S. Laali, and Z. Bayat, *"A single-phase cascaded multilevel inverter based on A new basic unit with reduced number of power switches," IEEE Trans. Ind. Electron., vol. 62, no. 2, pp. 922-929, Feb.* 2015

[2] J. Rodriguez, L.G. Franquelo, S. Kouro, J.I. Leon, R.C. Portillo, M.A.M. Prats, and M.A. Perez, "Multilevel converters: An enabling technology for high power applications," *Proceedings of the IEEE*, vol. 97, no. 11, pp. 1786-1817, Nov. 2009.

[3] Bolla Madhusudana Reddy, Dr.Y. V. Siva Reddy, Dr. M. Vijaya Kumar, *"Design Of Novel Cascaded Multilevel Inverter By Series Of Sub Multilevel Inverters", IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) e-ISSN: 2278-1676,p-ISSN: 2320-3331, Volume 10, Issue 4 Ver. II (July – Aug. 2015), PP 25-30.* D

[4] C.R.Balamurugan , S.P.Natarajan and T.S.Anandhi, *"Single phase symmetrical multilevel inverter design for various loads"*, Electrical and Electronics Engineering: An International Journal (ELELIJ) Vol 5, No 2, May 2016.

[5] Chippy Venugopal, Shinosh Mathew, *"A single source five level inverter with reduced number of switches"*, IJAREEIE *(An ISO 3297: 2007 Certified Organization)* Vol. 4, Issue 5, May 2015.

[6] José Rodríguez, *IEEE, Jih-Sheng Lai, IEEE, and* Fang Zheng Peng, *"Multilevel inverters: A survey of topologies, controls, and applications"*, IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, VOL. 49, NO. 4, AUGUST 2002

[7] L.G. Franquelo, J. Rodriguez, J.I. Leon, S. Kouro, R.C. Portillo, and M.A.M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Magazine*, vol. 2, no. 2, pp. 28-39, Jun. 2008.

[8] E. Babaei, "A cascade multilevel converter topology with reduced number of switches," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2657-2664, Nov. 2008.

[9] J. Rodriguez, J.S. Lai, and F.Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[10] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197-2206, Jul. 2010.

[11] Y. Hinago and H. Koizumi, "A single phase multilevel inverter using switched series/parallel dc voltage sources," *IEEE Trans. Ind. Electron.*, vol. 58, no. 8, pp. 2643-2650, Aug. 2010.

[12] E. Babaei, S. Laali, and Z. Bayat, "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 922-929, Feb. 2015.

[13] E. Babaei, S. Sheermohammadzadeh, M. Sabahi, "A new cascaded multilevel inverter with series and parallel connection ability of dc voltage sources," *Turkish Journal of Electrical Engineering & Computer Sciences*, vol. 23, pp. 85-102, Feb. 2015.

[14] D.. Floricau, E. Floricau, and G. Gateau, "New multilevel converters with coupled inductors: properties and control, " *IEEE Trans. Ind Electron.*, vol. 58, no. 12, pp. 5344-5351, Dec. 2011

[15] P. Lezana, J. Rodriguez, and D.A. Oyarzun, "Cascade multilevel inverter with regeneration capability and reduced number of switches," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1059-1066, Mar. 2008.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 5, May 2017

[16] E. Babaei and S. Laali, "Optimum structures of proposed new cascaded multilevel inverter with reduced number of components," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6887-6895, Nov. 2015.

[17] J. Ebrahimi, E. Babaei, and G.B. Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 655-667, Feb. 2012.

[18] E. Babaei, M. Farhadi Kangarlu, M. Sabahi, and M.R.A. Pahlavani, "Cascaded multilevel inverter using sub-multilevel cells," *Electr. Power Syst. Res.*, vol. 96, pp. 101-110, 2013.

[19] M. Farhadi Kangarlu, E. Babaei, "A generalized cascaded multilevel inverter using series connection of sub-multilevel inverters," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 625-636, Feb. 2013.