ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: www.ijareeie.com

Vol. 6, Issue 5, May 2017

Design a Low Power 4:2 Compressor using Adders

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ABSTRACT: The conventional digital computation arithmetic circuit with different architecture are designed to produce the effectual results. The 4:2 Compressor is the mostly utilized for multipliers actualisation based on the less number of Transistors in place of conventional design. In the Arithmetic function most of design using Adders in an essential portions. The design has to complete with the CMOS technology .The main purpose of this paper to reduce power consumption and delay in the 4:2 Compressor circuits using Adders. This paper represent the review of proposed work of Compressor, using different number of transistors and compared with the static designs. The more number of transistors in an IC has increased power dissipation. That's why, low-power circuits have become a main precedence in modern VLSI design with using less number of transistors.

KEYWORDS: Adders, 8T, 6T, CMOS Technique, Tanner EDA V16.0.

I.INTRODUCTION

In field of VLSI Designing the compactness of the chip is necessary to reduce the power consumption, area for improve performance of the multimedia devices.Now a day's, battery life is most concern field in digital life environment, portability of devices which make our work easier save time and money. In such case it is the major task for the designer to give the expected out come to the user and make the device user friendly. In field of arithmetic circuit the multiplexer and adders are the mostly used component in chip designing. Multiplier has mainly used to reduce the complexity of the arithmetic circuits which has mainly three works: partial product generation, partial product reduction and addition.For the organization of the power and voltage source is an important area to concern due to the increased implementing of multimedia devices. In the field of chip designing Multipliers and Adders are the mostly used sources of power consumption. The lower order compressors are used to improve the performance of the complex part of the circuits like 3-2, 4-2 and 5-2 compressors, and are used as the conventional components in many DSP applications. In this paper, 4:2 compressors has been designed using different logic styles with the existing CMOS logic. In this proposed 4:2 compressor architecture we can designed by using less number of transistor for implementation. We perform the compressor design by using conventional logic styles, are discussed with using these low power Adders architectures.We can reduce the power dissipation by reducing the supply voltage. In this technique, we use the less number of transistors by reducing the number of transistor we can also reduce and simplify the complexity of the circuits in the arithmetic and digital systems. Compressor is one of the device which is used to overcome the complex calculation in multipliers circuits, it reduce the power consumption and delay of the circuit. To the lower response time of the partial product accumulation stage, 4-2and5-2compressorshavebeenwidely utilized nowa days for high speed and performance of multipliers. The 4-2compressoris nonesuch forthe structure of regularly construction of, Wallace tree with less complexity various 4-2 compressor circuits have been proposed for less power and efficient area. Some of these are capable to functioned to low supply voltages, but require enormous number of transistors due to their CMOS structures, others uses of less numberoftransistorsbut flunk tofunctionat ultralow voltages, or fail the driving capability to drive the next level of the systems.

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II.ARCHITECTURES

In this section various types of designs are discussed as the basics of the designs to structured 4:2 compressor. Various type of adders are used in privies designs some are discussed below:-

Basic Adder block: A full Adder circuit add three number as input (A, B, C) and it gives the response as the addition of bit values represent as Sum and carry. It perform the addition of the given input function and give the output as Sum and Carry, digital logic gates are used to design the Adder.

Sum = (A XOR B) XOR Cin
Cout = A AND B + Cin (A AND B)

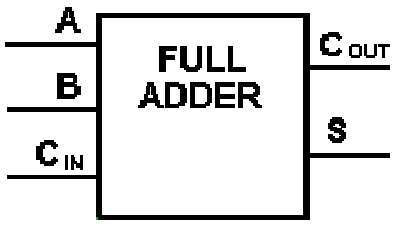

Fig.1: Block diagram of 1-bit Full Adder circuit.

The basic circuit include the Gates for designing the Full Adder, it consist of the two XOR Gate three AND Gate and one OR Gate.

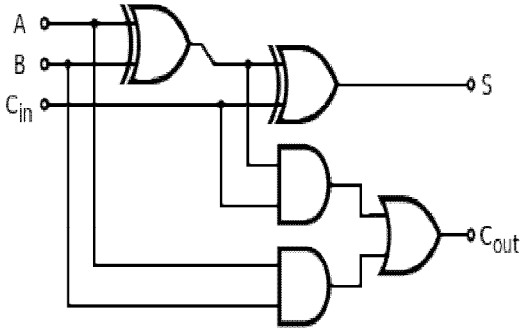

Fig.2: Static Design of Full Adder circuit using Gates.

Full Adder using 28T: It also consist the three input and two output, full adder also design using connecting two HA. In this paper we use CMOS Technology to design the full adder circuit .It require the 28 number of Transistors with three input (A,B,C) to give two number of output Sum and Carry respectively as the response of the Full Adder circuit. The Fig.3 shows that the function of the Full Adder cell using 28T.

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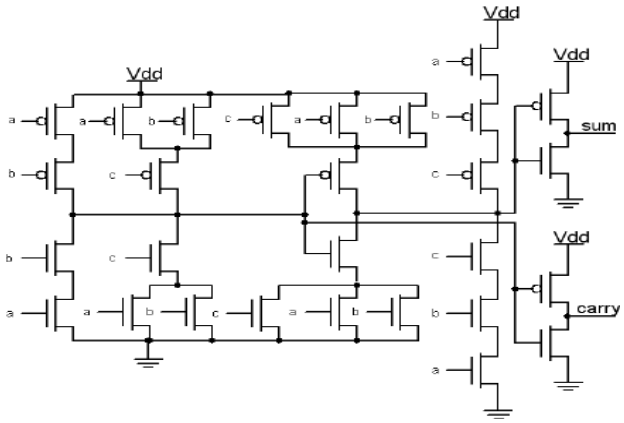

Fig.3: Full Adder using Static design 28T.

So many logic styles have been designed using CMOS logic technique. The basic in between them is the Static logic which consist of the combination of both NMOS and PMOS. Fig.3, shows the Static CMOS logic style of representing pulling up and pulling down NMOS transistors. The fig.3, shows that the above logic style uses 28 transistors which is lead to high area expense and high power dissipation.

Full Adder using 8T:Fig.4 shows the circuit of 8T1-bit Full Adder cell. The Sum output is basically organized by a cascaded exclusive ORof the three inputs. Cout is implemented using 2-transistormultiplexer.

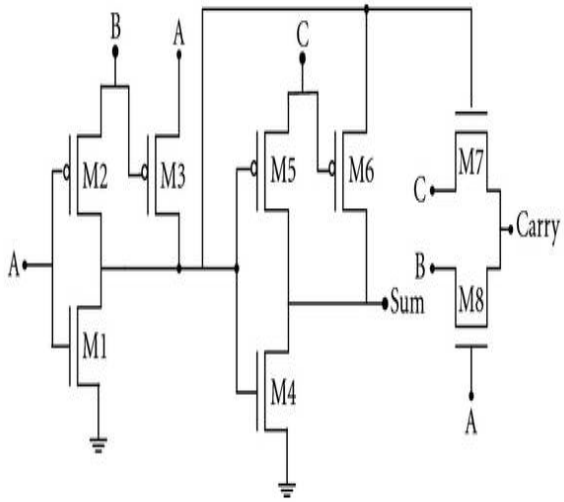

Fig.4: Full Adder using 8T

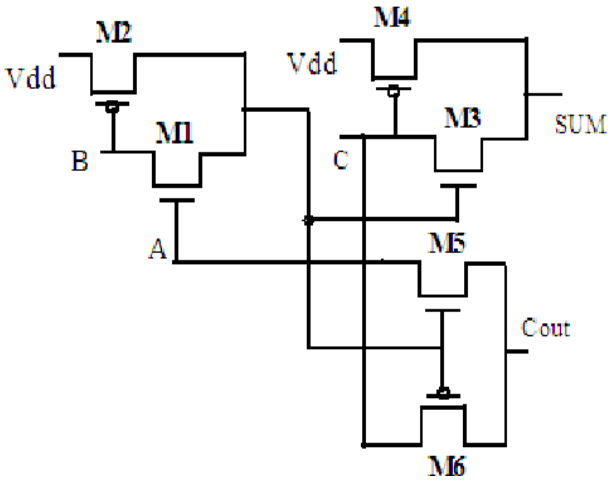

Fig .5: Full Adder using 6T.

As shown in Fig.4 the full adder further researches have done by reducing the number of transistors used in the previous operation of calculating sum and carry. Which was proposed in the existing system of designing compressor circuits. Proposed a full adder design by using transistors level logic style. Further reductions in the number of Transistors using various logics were proposed and new designs were developed. The above Fig.5 consist the 6T out of this 3 are N-channel and three P-channel.

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III.LITERATURE REVIEW

A Brief Review of the Work already done in the Field: We take review from number of research paper and various journal and conference papers. We are studied the work and the development of the structure in different technique. In digital system processing the speed of the system is necessary to enhance the performance and get the desire outcome. As we know different type of adder and multiplier are used to construct the 4:2 compressor. In previous many papers use the MUX and the XOR gate for the construction of the Adder circuit to develop the Compressor.

Veeramachaneni et. Al The lower order compressors are used as the main cell in different arithmetic applications, and mostly in particular partial product summation in multipliers. In this paper novel .Designs of high speed, low power (3-2, 4-2, and 5-2) compressors having the abilityto performat low voltages are correspond at design. The main concern fields are discussed which are power consumption, overall delay and efficient area and also compare the compressor with the existing one. By using multiplexer in proposed work gives the better efficient design also in all previous design implementations are compared like design using XOR and multiplexer. Both output and its opposite are present but resent designs of compressors do not use these outputs expeditiously. In the paper architecture, the outputs are expeditiously organized to heighten the performance of compressors. The low power, less number of transistor and efficient delay represent the new compressors an executable option for effective design.

Agarwal et. Alhybrid-CMOS logic style use thefull Adder by separated it into three modules so it can design usingmost effective of various levels. In this design first module is an XOR-XNOR circuit, which are capable to generate full swing XOR and XNOR outputs at the same time and have a better driving potentiality. It also consumes minimum power and provides better delay performance. Further in the design second module is a Sum circuit which is also a XOR circuit and uses Carry input and the output of the first module as input to give the Sum output. Third module is a carry circuit which uses the output of the first stage and other inputs to generate carry output. In the proposed full adder design we have design new full adder circuit which overcome the power consumption, over all delay between Carry out to carry in and Power Delay Product.

Tonfat et. Al: In this paper we use the compressor circuit designed using arithmetic cell like full adder. In the most VLSI circuit compressors are designed using adder to implement arithmetic circuits, most of the arithmetic circuits use multiplier and adders. (ARSTRAN) is the basic tool with the help of this we generate the electrical and physical performance of the proposed architecture .In this paper we use the multiplexer cell in place of the gates like XOR and XNOR, And the automated physical layout generated by using the proposed tool. This tool has overcome the area power consumption in circuit and the overall delay.

Menon et. Al Many arithmetic circuits like adders, mux are main elements of high performance are employed in the DSP systems. In the highly recommended of these applications, multipliers have been a complex and mostly used component in the overall circuit performance. When is strained by power consumption and speed. Compressors are a vital component of the multiplier circuit in many applications, which greatly regulate the overall multiplier speed. The authors propose two novel high performance low logic compressor architectures to give the better performance. The main objective of their designs is to restrict the carry propagation to a single stage, thereby overcome the overall propagation delay. The designs are compared with the best one in the literature in terms of delay and are found to have lower values.

Radhakrishnan et. Al In this proposed work paper a 4:2 compressor circuit is designed by using pass transistor logic for the better result in performance of the system. In this the design use the XOR-XNOR gates and avoid the use of inverter cell. The complete circuit is designed using 28T .Tish work represent many low power and high performance cells, to overcome the use of the complex circuit architectures. The total voltage it reduced by minimise the output voltage swings at the nodes in the overall circuits. The performance of the most of DSP applications are

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Vol. 6, Issue 5, May 2017

depend at the selection of the cells. This paper reduce the most important field in the VLSI system and give the expected results.

IV. PROPOSED METHEDOLOGY

Compressor: In above previous work the design of compressor is employed for the efficiency and power consumptions of the system. In the proposed work we compare the power consumption of the compressor and the overall delay of the circuit by using Various Adder designed with CMOS technology and reduce the number of transistor for the improvement of the performance of the design. Compressors are the most usable component in the DSP applications now a days .Compressors are constructed using different technique like Adiabatic logic ,Pass transistor logic ,Wallace tree multipliers , Adders using CMOS technology etc. Here the 4:2 Compressor using blocks are shown in Fig.7 & fig.8:-

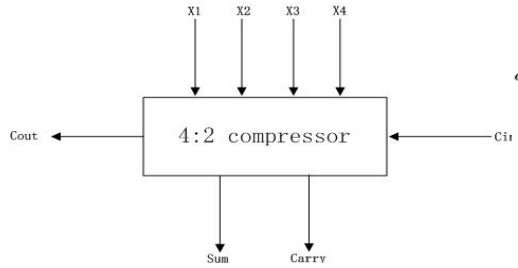

Fig.7: Block diagram of 4:2 compressor circuit.

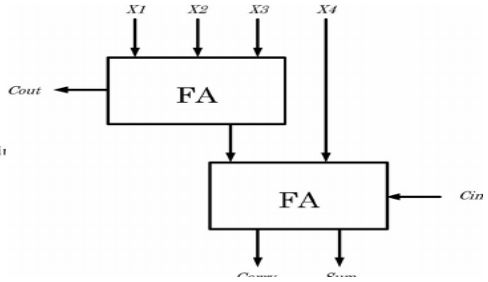

Fig.8: 4:2 Compressor using Two Full Adder.

Using Full Adder compressors have been implement arithmetic and digital signal processing (DSP) circuits for low power applications. Compressors are mainly used component in multiplier architectures. Multipliers are designed into three part: partial-product generation, partial-product accumulation and final addition. In the first part, the multiplication function is performed bit by bit to give the partial products as the output. The second part is the most significant part of multipliers and enhance the performance of the system. In this proposed work the methodology is used to design 4:2 compressor is transistor level different CMOS logic technique basically we develop the 4:2 compressor using different Full Adder. As shown in Fig.8, the compressor is the combination of the two Full adder circuit.

$$Sum = x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin$$

$$Cout = x1 \oplus x2\ x3 + x1x2$$

$$Carry = (x1 \oplus x2 \oplus x3 \oplus x4)\ Cin + (x1 \oplus x2 \oplus x3)\ x4$$

Inputs				Cin 0		Cin 1		Cout
A	B	C	D	Carry	Sum	Carry	Sum	
0	0	0	0	0	0	0	1	0
0	0	0	1					
0	0	1	0	0	1	1	0	0
0	1	0	0					
1	0	0	0					
0	0	1	1	0	0	0	1	1
0	1	1	0					
1	1	0	0					
0	1	0	1					
0	1	1	1	0	1	1	0	1
1	1	1	0					
1	1	0	1					
1	1	1	0					
1	1	1	1	1	0	1	1	1

Fig.9: Truth Table of 4:2 Compressor circuit.

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By using different type of Adder in construction with the different technology and the voltage source. By using less number of the transistors we can simplify the complexity of circuit and performance of the system.

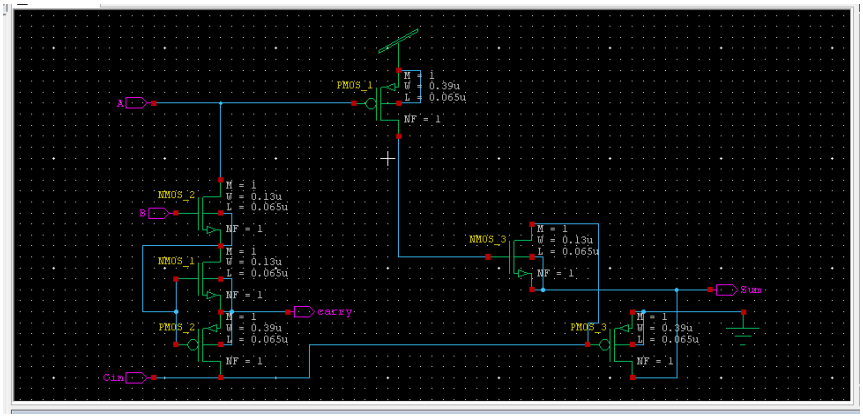
V. RESULT AND DISCUSSION

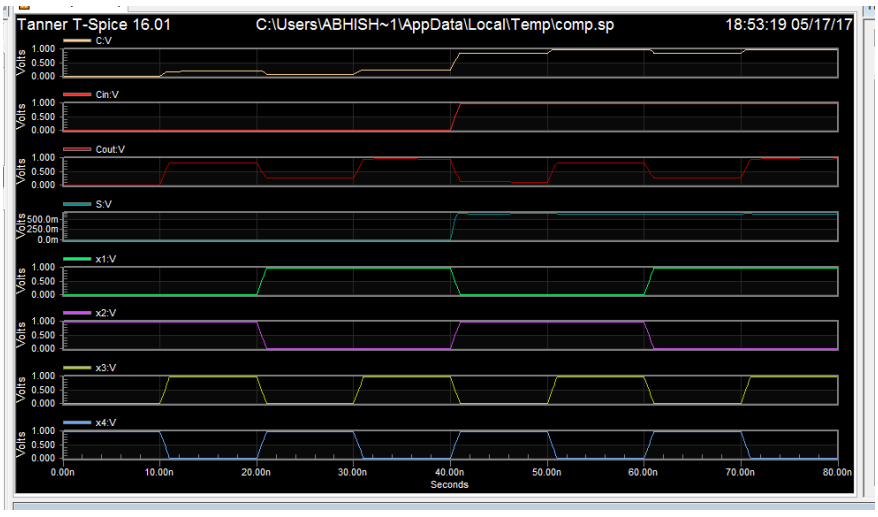
In this paper various types of adders are used to design compressor some low power adder are shown below:

Compression Table of Adders in previous work

TYPE OG LOGIC	NO. OF TRANSISTORS	POWER CONSUMPTION(nW)	DELAY(ns)
STATIC	28	62.35	420.3
8T	8	12.56	302.5
6T	6	5.69	186.6

The above table show the different between the logics as the table show by reducing number of transistor following results are shown. Using this we design the 4:2 compressor circuit and see the result in terms of Power and overall delay. Below fig. shows the CMOS design of 6Tadder and the Wave form of the 4:2 Compressor respectively.





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V.CONCLUSION

By using the different voltage and the technology we get the better result, by designing the various low power Full Adder for construction of 4:2 compressor has the les number of transistor which reduces the power consumption in design by using less voltage source .The power consumption will less and also reduce the overall Delay in the circuit. Adders are mostly used in arithmetic circuit because of their reliability and durable for the DSP systems. By reducing the number of transistor in circuit reduce the overall delay and also consume less power.

REFERENCES

1 Ajit Pal, "Low Power VLSI Circuits and systems" Springer India 2015.
2 Sreehari Veeramachaneni, Kirthi Krishna M, Lingamneni Avinash, Sreekanth Reddy Puppala , M.B. Srinivas Centre for VLSI and Embedded System Technologies. International Institute of Information Technology Gachibowli, hyderabad-500032, India."Novel Architectures for High-Speed and Low-Power 3-2, 4-2 and 5-2 Compressors"20th International Conference on VLSI Design 0-7695-2762-0/07 $20.00 © 2007.
3 Mayur Agarwal, Neha Agrawal, Md. Anis Alam "A New Design of Low Power High Speed Hybrid CMOS Full Adder" 2014 International Conference on Signal Processing and Integrated Networks (SPIN).Jorge Tonfat, Ricardo Reis, "Low Power 3-2 and 4-2 Adder Compressors Implemented Using ASTRAN" XXVII SIM - South Symposium on Microelectronics 2014.
4 R. Menon and D. Radhakrishnan, "High performance 5: 2 compressor architectures"IEE Proc.-Circuits Devices Syst., Vol. 153, No. 5, October 2006.
5 D. Radhakrishnan Department of Electrical and Computer Engineering State University of New York, A.P. Preethy, School of Computer Engineering, Nanyang Technological University, "Low Power CMOS Pass Logic 4-2 Compressor for High-Speed Multiplication" Proc. 43rd IEEE Midwest Symp. On Circuits and Systems, Lansing MI, Aug 8-11, 2000 0-7803-6475-9/00/$10.00 ©IEEE 2000.
6 *Jiangmin Gu and Chip-Hong Chang* School *of* Electrical and Electronic Engineering, Nanyang Technological University, "low voltage, low power (52) compressor cell for fast arithmetic circuits" ICASSP 2003, ***Proc.** IEEE **In: CO$ on Application-Specific Systems, Architectures, and Processors, 2000.*** pp. 235 -243, 2000.
7 *Karuna Prasad Keshab K. Parhi* Morphics Technology Inc. Campbell, California, USA Department of Electrical and Computer Engineering University of Minnesota, Minneapolis, USA, "Low-Power 4-2 and 5-2 Compressors".
8 Richa Singh, Anjali Sharma, Rohit Singh," Power Efficient Design of Multiplexer based Compressor using Adiabatic Logic", International Journal of Computer Applications, November 2013, pp. 45-50
9 Momeni, J. Han, Member, P.Montuschi, Senior Member and F. Lombardi," Design and Analysis of Approximate Compressors for Multiplication", Transactions on Computers, pp.1-13
10 Jorge Tonfat, Ricardo Reis, "Low Power 3-2 and 4-2 Adder Compressors Implemented Using ASTRAN", South Symposium on Microelectronics, pp.1-6.