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# Super-fast Hierarchical Topology for Network on Chip for mega CMP core Architecture

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**ABSTRACT**: Today, advanced fabrication technologies promise us mega integration of processor cores on single chip. It is an era of multiprocessor engines and parallel computing on chip. However, just integration of multiple PEs is not sufficient for these calculating monsters. Internally, they must be fortified with proper network. The NOC with appropriate topology is the only way to weave communication fabric for efficient integration of PEs. The key challenge is reducing the number of hops required for data packets to reach from one end to other end processor core. Regular topology fall less for mega core integration. Problems like slower network, traffic congestion and non tolerable latency crop up. For efficient communication between PEs the hierarchical network typology clubbed along with parallel network provides a solution. The proposed topology reduces the number of hops taken by packets from source to destination nodes and latency too is reduced with hybrid topology. The proposed network solution combines hierarchical, spidergon and star topology. A little attention is also given to the interconnecting router architecture for hierarchy planes.

**KEYWORDS:** Network-on-chip (NoC), System on chip (SoC), processor element (PE), Chip Multi-Processor (CMP)

## I.INTRODUCTION

Progress in parallel computing and SOCs has fueled integration of more number of processor cores, memory controllers and other specific accelerators. Final achievement is high performance processing power. For less number of cores bus-based architecture works well. It is still well proven and robust. However, the bus based architecture becomes bottleneck as the number of cores on chip cross 16. It is not suitable for multiple masters communicating simultaneously. Also it is less efficient in case of power consumption and area consumed. In that case, NoC is the solution. For moderate integration of PEs (up to 100) NOC with regular topology works well. In this research article, I want to consider integration of PEs more than 100. When question comes of mega integration (thousands of PEs), one need to choose topology very carefully . I propose a hybrid topology (star plus spidergon plus hierarchical) as a solution for it.

Granular analysis of process allotment, traffic phases and software threads leads to efficient SOCs. It saves design time, silicon area, power, extra networking etc. Here I am considering a general CMP architecture where network traffic pattern is unknown. Good process allotment policies may give better results with keeping minimum exchange of information between PE clusters. However, still some peculiar computations may need frequent exchange of information between clusters leading to complex network traffic. For that, I suggest parallel network and additional routers to avoid traffic congestion. In this article moderate traffic between clusters is considered. Subsequent sections are as given below:-

- Section II-quick overview of other topology performance
- Section III- finding topology for mega integration
- Section IV- proposed topology
- Section V- router architecture
- Section VI- proposed hybrid topology Vs other regular topology
- Section VII-modular additions to topology

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- Section VIII- from 2D topology to 3D topology
- Section IX- conclusion

The tile required for building base level in the hierarchy is explained and the topology for interconnecting 64, 512 and 4096 nodes is explained in proposed topology section.

## II. QUICK OVERVIEW OF OTHER TOPOLOGY PERFORMANCES

A 2D Mesh topology is mostly used due to its proven simplicity and suitability. Pyramesh is another good solution for moderate integration (i.e. maximum 64 number of PEs)[2]. However for mega integration of PEs, more hops per packet delivery becomes bottleneck[2]. "The square octagon interconnect" topology [4] is better in terms of number of hops but still not suitable for 250 and above PEs. "The clustering in mesh"[6] caters for heterogeneous core integration. Direct Network [7] is useful for large data transfers. Switch based design is used in scalable interconnection of direct network. Indirect Network is packet based and topology is selected as per the application requirement. The hierarchical topology is solution to reduce the number of hops and faster network. It needs lesser number of routers as compare to flat 2D mesh topology. Fat tree or spin network topology are suitable for integration of PEs less than 250. But still, this topology is not suitable for CMP architectures having large number of cores, as congestion occurs in case frequent inter cluster communication.

## III. FINDING TOPOLOGY FOR MEGA INTEGRATION

As we are considering generic solution for mega integration of PEs (500 to 1000 and above), I look for hybrid topology implementation. A spidergon combined with star topology at multiple level of hierarchy is proposed in this research article. A hybrid approach is proposed for reducing hops efficiently. Of course, the router complexity is more for interconnecting nodes, but requirement of mega integration and faster network win over it. Spidergon and star topology combined here are having PEs at every node, but at the hub, PE may not be there in traditional star topology. As per the requirement of application, we can add summing PE at every hub of the star. This resembles to the neural network. See figure 1,2,3 and 4. Billions of neurons work seamlessly in human brain. I have taken inspiration from the basic model of neurons in this topology[8]. Spidergon network is added on top of that, as we want faster and efficient network.

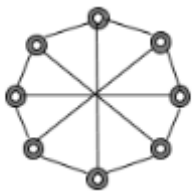

**Figure 1: Spidergon Topology**

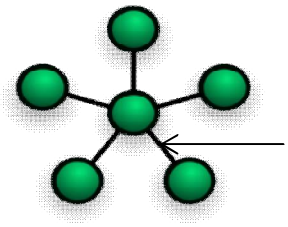

**Figure 2 : Star topology**

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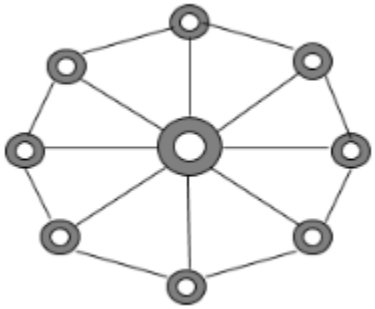

**Figure 3: Spidergon topology with hub at the center for hierarchical network integration, fusion with star topology.**

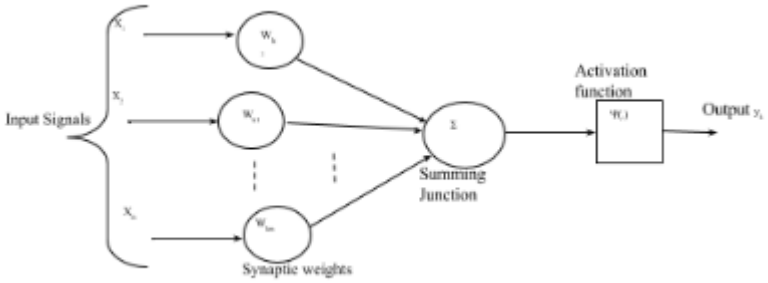


**Figure 4: Basic nonlinear model of Neuron**

As shown in the basic model, synaptic weights can become nodes in CMP architecture, summing junction can become hub and activation function can become I/O peripheral of the CMP. Inputs can come from another sensor network. Output can become understanding of our total system like human brain.

## IV. PROPOSED TOPOLOGY

The spidergon-star topology of eight nodes is shown in figure5. Tiles of 10 and 12 nodes can be formed in similar way. With every node leaf level router will be attached.

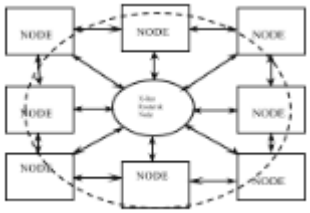

**Figure 5: 8 nodes spidergon-star Topology**

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In the following diagram I have given topology for the four levels of hierarchy. It is integrating 4096 PEs. At every level, eight routers are integrated except at the leaf level. (At leaf level, only four routers are connected including one upper level router, two neighboring router and one diagonally opposite ). At every level, spidergon-star hybrid topology is followed. For the sake of understanding and to avoid complexity, at higher levels of hierarchy, complete network is not shown in the diagram. The topology is modular and number of levels of hierarchy can be reduced for the integration of less number of PEs.

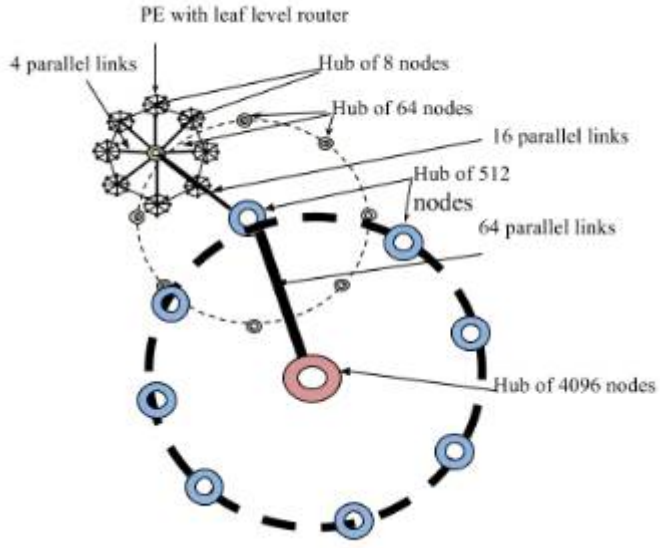


Fig. 6 Spidergon-star hybrid topology with hierarchical & parallel network

## V. ROUTER ARCHITECTURE

Depending on the topology selected, router will have number of I/P and O/P ports. For example, if at the lowest hierarchy, eight PEs exist, at first level (one level upper) of hierarchy, router will have eight input ports and eight output ports. In addition, it will have (1) one pair of input and output port for the upper echelons of network called port H (hierarchy) (2) Two pairs for neighboring routers at the same level called port L (left) and Port R (right) (3) one pair for diagonally opposite router at the same level called Port D (diagonal). In total 12 pair of ports. Thus spidergon-star hybrid topology is followed at the first level of hierarchy. If Similar structure is followed in every hierarchy, same router design will do the job. Router clubbed along with PE, i.e. router at the leaf level will have similar design with fixed four pair of input and output ports. Two ports for adjacent PEs i.e. port L and port R, one port for diagonally opposite PE i.e. port D and one port for router at the first level (one level upper) of hierarchy i.e port H.

**Parallel Network:-** At first level each port width is one link. Same way at second level it is 4 times of first, at third level 16 times and fourth level 64 times. Port going to next level of hierarchy, will have parallel links equal to that upper hierarchy. For example, at first level port H will have four parallel links.
Here I am elaborating the design for router at the first level of hierarchy.

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Considering virtual cut through (VCT) routing[9], one FLIT size buffer is attached with every input port. Routing control unit will divert data traffic to output ports as per requirement. In case multiple requests for a single output port, round robin priority will be followed by the router.

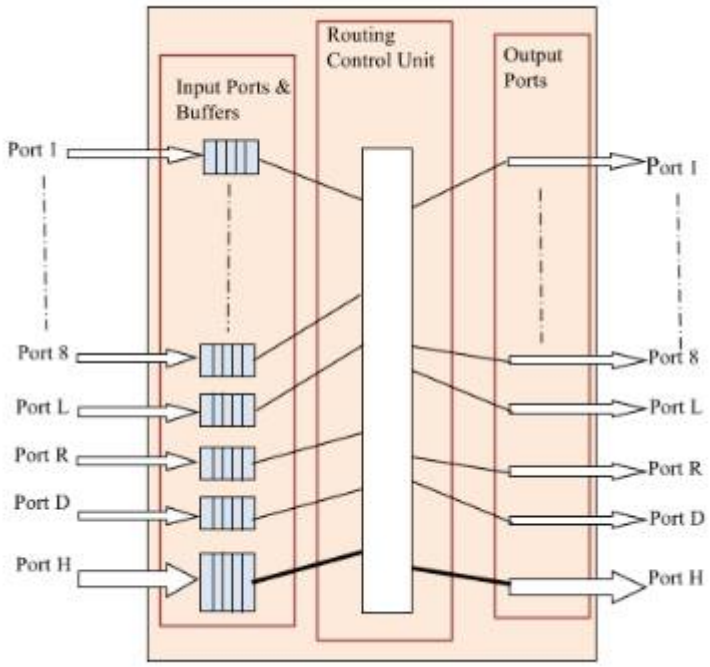


**Fig. 7 Router internal architecture**

In routing control unit, output router selection logic block will store packet headers for every packet, which it has to network. It will in turn divert network traffic by generating appropriate selection signals for multiplexers. Neighboring router will be selected as per the destination PE specified in packet header and the network which follows minimum hop distance for it. FLIT transmission will not occur if the neighboring router has already asserted busy signal.

**Algorithm for output router selection block:-**

- ✓ Poll for packet header for all input ports.
- ✓ Once header is received find destination node number in packet.
- ✓ Check whether destination node is in same cluster.
- ✓ If yes, route through adjacent/opposite router in the same level.
- ✓ If not, route the packet to upper hierarchy.
- ✓ Again check, whether destination lies within same cluster in current hierarchy.
- ✓ If yes, route through adjacent/opposite router in the same level.
- ✓ If not, route the packet to next upper hierarchy.
- ✓ Repeat it till it completes all the hierarchies.
- ✓ No destination found, drop the packet.
- ✓ If found, search nearest router for the packet for shortest path to the destination
- ✓ Check whether nearest router is busy.
- ✓ If busy, look for second shortest path.
- ✓ Repeat till path is found.

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- ✓ If all possible paths are busy, halt the packet till it finds empty route.
- ✓ Once route is found, generate mux selection signals
- ✓ Connect input port to appropriate output port
- ✓ Allow trailing FLITS through the same path.
- ✓ Repeat the algorithm for every input port.
- ✓ In case, multiple input port found same shortest path and same nearest router as next hop, follow priority on round robin basis.

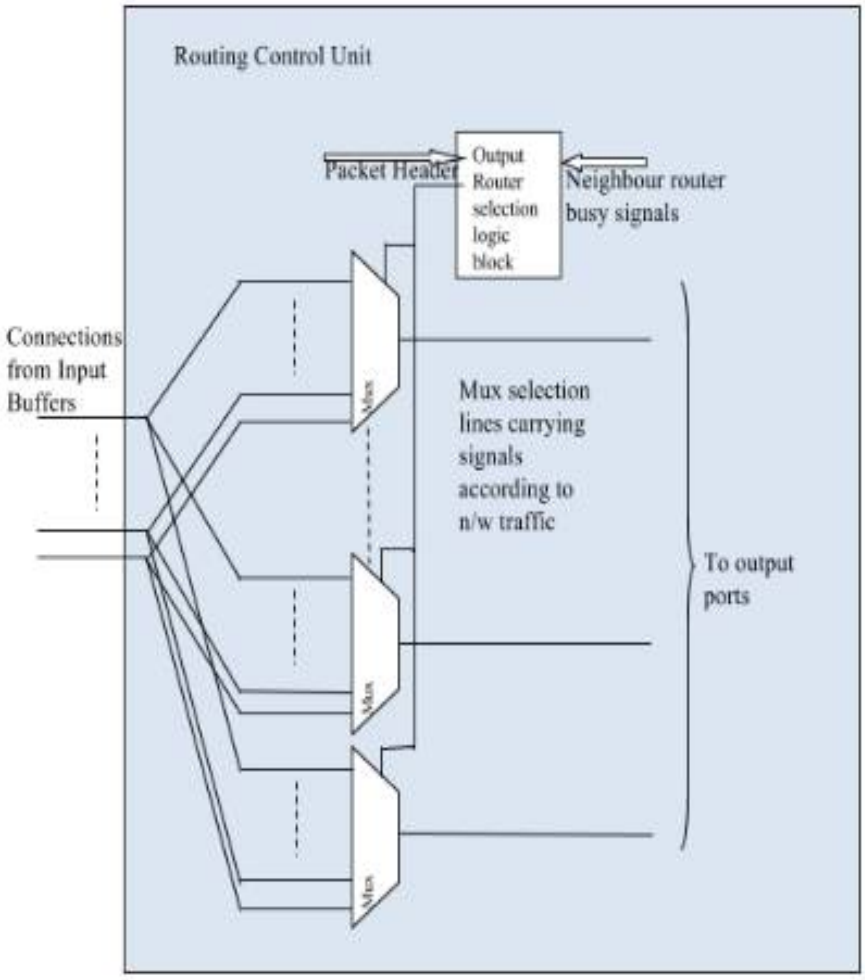


Fig. 8 Router control Unit

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Following table shows routers required for number of PEs' integration with proposed hybrid and hierarchical topology

| No of PEs | Leaf Router | Hierarchy Level1 Router | Hierarchy Level2 Routers | Hierarchy Level3 Routers | Hierarchy Level4 Routers | Total routers |
|---|---|---|---|---|---|---|
| **64** | 64 | 8 (Hub of 8 leaf router) | 1(Hub of 8 Level1 router) | -- | -- | 73 |
| **256** | 256 | 32 (Hub of 8 leaf router) | 4 (Hub of 8 Level1 router) | 1 (Hub of 8 Level2 router) | -- | 293 |
| **512** | 512 | 64 (Hub of 8 leaf router) | 8 (Hub of 8 Level1 router) | 1 (Hub of 8 Level2 router) | -- | 585 |
| **4096** | 4096 | 512(Hub of 8 Leaf router) | 64(Hub of 8 Level1 router) | 8 (Hub of 8 Level2 router) | 1(Hub of 8 Level3 router) | 4681 |
| **1000** | 1000 | 100 (Hub of 10 leaf router) | 10(Hub of 10 Level1 router) | 1 (Hub of 10 Level2 router) | -- | 1111 |
| **1728** | 1728 | 144 (Hub of 12 leaf router) | 12(Hub of 12 Level1 router) | 1 (Hub of 12 Level2 router) | -- | 1885 |

**Table 1.0**

## VI. PROPOSED HYBRID TOPOLOGY VS OTHER REGULAR TOPOLOGY

Now, Let us consider longest hop length in various topology for 'N' number of nodes/PEs. Longest hop length is given by formulas : -

**Maximum No of hops taken by flits for 'N' number of PEs**.

1. For 2D Mesh :- [2SQRT(N) -1]
2. For RING :- [(N)/2] - 1
3. Torus 2 D :- SQRT[N] + 1
4. Binary Tree :- 2 * $LOG_2$ (N) -1
5. Tree with k leafs: - 2*$LOG_k$ (N)-1
6. Proposed Hybrid Topology:- 2(HL)+3, HL is hierarchy level starting from 0,1,2…

For the proposed topology, for N nodes, we need approximately 14% extra routers for base 8 hubs, 12% for base 10 hubs and 10% extra for base 12 hub in comparison with 2D mesh topology. However we get very good reduction in longest hop length. See table 2.0

Another important aspect is path length which is directly proportional to the hop length of the network. Thus Hybrid topology gives better result in case of hop length and path length. See Table 3.0

| Topology | Longest Hop Length | | | |
|---|---|---|---|---|
| | 8 PEs | 64 PEs | 512 PEs | 4096 PEs |
| **2D Mesh** | 5 | 15 | 45 | 127 |
| **Ring** | 3 | 31 | 505 | 2047 |
| **Torus** | 4 | 9 | 24 | 65 |
| **Binary Tree** | 5 | 11 | 17 | 23 |
| **Fat Tree with four leafs in every branch** | 2 | 5 | 8 | 11 |
| **Proposed Hierarchical Hybrid topology** | 2 | 5 | 7 | 9 |

**Table 2.0**

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The comparison between proposed hybrid topology and regular 2D mesh topology for 'N' number of PEs is given below:

| **Criteria** | **2-D Mesh** | **Ring** | **Torus** | **Binary Tree** | **Fat Tree (base 4)** | **Proposed Hybrid** |
|---|---|---|---|---|---|---|
| **Average Hop Length** | SQRT(N) | N/4 | SQRT(N)-1 | $2\log_2 N-1$ | $2\log_4 N-1$ | $2\log_8 N-1$ |
| **Longest path length X=9.76*10-4mm2 at 14nm technology** | [2SQRT(N)]*SQRT(2X) | [(N/2)-1]*SQRT(2X) | [2SQRT(N)]*SQRT(2X) | 4096SQRT(X) | 486SQRT(2X) for 4096 PEs | 621SQRT(2X) for 4096 PEs |
| **No. Of Routers** | **N** | **N** | **N** | **N-1** | $\sum_{i=0}^{m} 4^i$ **where m=log4N-1** | $N+\sum 8^i$ **Where M=log8N-1** |

**Table 3.0**

Fat tree topology is having the least worst case latency among all regular topology. The proposed hybrid topology has one third worst case latency than the fat tree due to addition of spidergon network at every hierarchy. Thus even though, proposed topology requires more number of routers than the fat tree, it is better in comparison with worst case latency considering uniform traffic.

## VII. THE MODULAR ADDITIONS TO PROPOSED TOPOLOGY

Depending on the end user requirement, SoC designer has to choose NOC carefully. He has to keep balance between development/ production cost and used technology. Also, one need to opt reasonable capabilities of network. Unnecessary heavy capabilities of network will result in wastage of silicon area and power required to maintain it. Under capable network will result in less efficient and slow SoCs.
Redundancy in routers will add speed, reliability and lifespan of NOC. However choosing appropriate number of routers will save power and silicon.

Binary tree topology adds router for every two PEs. This may lead to silicon overhead but speed is achieved. However, for the ASICs where network traffic is fully predictable and slower network is affordable, we can increase number of PEs from two to 8,10 or 12 as per requirement.
Every PE may have its own local memory as distributed memory for computations such as digital image processing, advanced digital signal processing etc. CMP architecture becomes ace performer only after every PE getting clubbed with local memory. Also, router at the upper levels of hierarchy can be clubbed with summing PEs with more capability and more memory.

Dedicated DMA channels can be added, for heavy network traffic to improve performance further. Full duplex DMA channels can swap large memory contents very fast.
Fusion of bus architecture and routers also can exist where routers will go silent and they will behave just like repeaters. For very high priority operations, to reduce latency, these type of options in networking may be useful.

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Data compression techniques can be used for efficient networking. Instead of communicating complete information, pre - coded messages can be passed.

For massive integration, wireless technology wins definitely. Carbon nano - tube antennas are already at the place. But wireless NOC is still in incubation. My work may be useful for the applications where wireless communication is not preferred.
Or same topology can be modified by making few hubs wireless, especially, for the networking of one end cluster to other end cluster. As FDMA based wireless RF transmission for a channel having 16 nodes is already achieved in WiNOC with 18 nano meter fabrication technology[10].
The bandwidth of router at higher level of hierarchy can be kept more by providing higher link widths as compared to link width given in proposed design. Or end to end parallel wires can also be added directly for application specific requirements.

## VIII. FROM 2-D TOPOLOGY TO 3-D TOPOLOGY

In above discussion, we have considered only 2-D fabrication. If we go for 3D fabrication technology, present topology can be converted into 3D hybrid topology as shown in figure 9. Worst case hop length will remain same for 2D and 3D. But worst case path length can improved up to 33%. However, 3D fabrication technology is dearer compared to 2D fabrication. Designer need to achieve optimum balance between cost and performance. Obviously, 3D topology is better where cost is no bar.

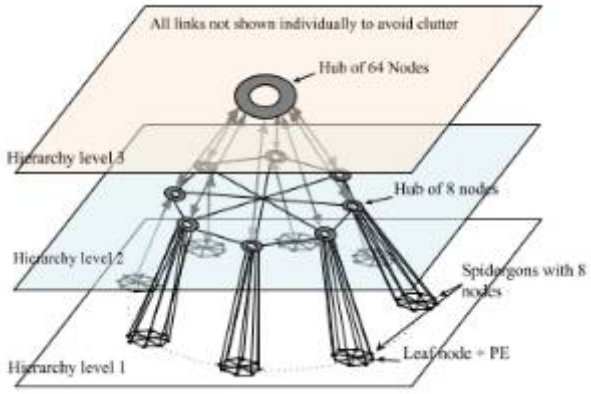


**Fig. 9 3D hybrid (hierarchical+spidergon) topology**

## IX. CONCLUSION

In this work, a hybrid topology is proposed for mega core integration of CMP architecture. The aim is to propose a topology for reducing hop distance compared to other regular topology. The analysis of router design required is done at abstract level. It is modular and can be extended in future for higher level of integration of PEs. Design performance is gauged in comparison with other regular topology. Various modular additions are suggested for customized NOC. Conversion of 2D topology to 3D topology is also included in modular changes for better performance.

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