



Low Power Multiplier Architectures Design Using Vedic Mathematics in 22nm Technology

Sushma S. Gadekar¹, Mahesh S. Badmera²

PG Student, Department of E&TC, Deogiri Institute of Engineering & Management Studies, Aurangabad (MS), India¹

Assistant Professor, Department of E&TC, Deogiri Institute of Engineering & Management Studies,
Aurangabad (MS), India²

ABSTRACT: This paper presents unsigned 8 x 8 high speed multiplier power and area efficient multipliers can be used in digital signal processor based applications. The high speed multipliers can be implemented by using Vedic mathematics mainly the “Urdhav Tiryakbhyam [3]” “Multiplication requires more hardware and processing time than addition and subtraction. Vedic algorithm (sutras) reduces the number of computational steps as compared with any conventional method. In the proposed system, the schematic is designed using TANNER TOOL. The design is verified in T-SPICE using 22nm CMOS technology library file. The performance evaluation that the transistor requirement is reduced hence the area, also the power consumption and propagation delay is reduced.

KEYWORDS: Multipliers, Vedic Mathematics, Urdhav Tirakbhyam Sutra.

I. INTRODUCTION

While designing any processor, the multiplier is basic building block. Multiplication process is used in many applications like communication, image processing, video processing, etc. To multiply two binary numbers a binary multiplier is used. Most multiplication techniques involve the process of adding a number of partial products. Many algorithms differ in the partial product generation and partial product addition to produce the final results (compare). The proposed system uses a multiplier based on the Vedic mathematics [3]. (The Vedic mathematics was rediscovered from 1911 to 1980 by Shri Bhatri Krishna Tirthaji Maharaj). Vedic mathematics contains 16 sutras.

This paper process the architecture which is based on Urdhva Tiryakbhyam. In this sutra the multiplication is based on vertically and cross wise operation.

This paper is organized in five sections. Section I gives a brief introduction, Section II technique of Vedic multiplication by using Urdhva Tiryakbhyam sutra. Section III Illustrates different multiplier design. Section IV presents experimental results of the proposed system and performance evaluation with previous systems. Section V concludes the paper.

II. VEDIC MATHEMATICS

Vedic Mathematics comprises four Vedas. Vedic mathematics explains various mathematical terms which includes arithmetic, geometry, trigonometry, factorization and quadratic equations. The Vedic mathematics was rediscovered by Shri Bhatri Krishna Tirthaji Maharaj (1884 – 1960). Swamiji has given 16 sutras and its explanation with it application. These Sutras along with their meanings are enlisted below alphabetically.

- 1) Shunyamanyat – If one is in ratio, the other is zero.
- 2) Chalana-Kalanabyham – Differences and Similarities.
- 3) Ekadhikina Purvena – By one more than the previous One.
- 4) Ekanyunena Purvena – By one less than the previous one.
- 5) Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
- 6) Gunitasamuchyah – The product of the sum is equal to the sum of the product.
- 7) Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
- 8) Paraavartya Yojayet – Transpose and adjust.
- 9) Puranapuranabyham – By the completion or noncompletion.

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- 10) Sankalana- Vyavakalanabhyam – By addition and by subtraction.
- 11) ShesanyankenaCharamena – The remainders by the last digit.
- 12) ShunyamSaamyasamuccaye – When the sum is the same that sum is zero.
- 13) Sopaantyadvayamantyam – The ultimate and twice the penultimate.
- 14) Urdhva-Tiryakbhyam – Vertically and crosswise.
- 15) Vyashtisamanstih – Part and Whole.
- 16) Yaavadunam – Whatever the extent of its deficiency.

This paper is discussed by using Urdhva Tiryakbhyam (UT) Sutra. It is seen that by using this sutra, the designing of faster and lower power multiplier circuits can be implemented. Urdhva Tiryakbhyam Sutra is a Sanskrit word which means vertically and crosswise explanation for 2-bit multiplication is as follows

$$\begin{array}{r} a1 \quad a0 \\ \times b1 \quad b0 \\ \hline a1 \times b1 : a1 \times b0 + a0 \times b1 : a0 \times b0 \end{array}$$

Similar type of 2-bit multiplication can be carried out for any digital numbers by using Urdhva Tiryakbhyam algorithm.

III. DESIGN OF MULTIPLIER ARCHITECTURE

A) Design 2-Bit Multiplier

The fundamental block for all types of multiplier design is a 2-bit multiplier. The proposed 2-bit multiplier comprises four AND gates and two 1-bit half adder blocks. The modified AND gate consists of five transistors which is having one less transistors as compared with the conventional multiplier [4]. The half adder used is designed with 9 transistors. Figure 1 shows the 2-bit multiplier.

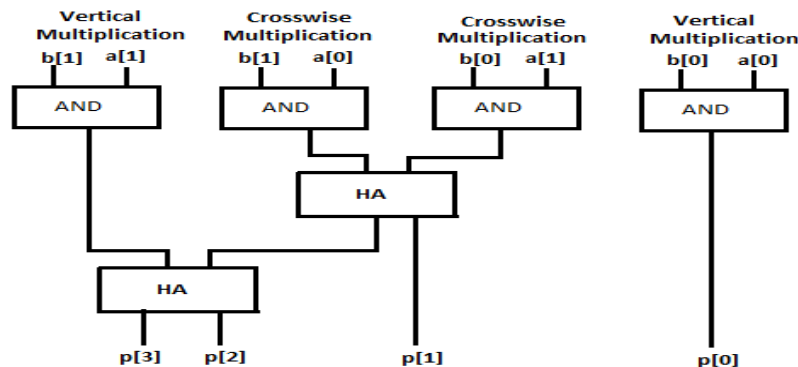


Figure 1 Design of 2-bit Multiplier

B) Design of 4-bit multiplier

The 4-bit multiplier is designed by using four 2-bit multiplier and three 4-bit adders. The different blocks of a 4-bit multiplier are as shown in figure 2. Each adder consists of four full adders. The full adder is used in this design is having 14 transistors [4] [5]. With use of this new full adder it is observed that the speed of multiplication is improved with low power consumption. The conventional multipliers units comprise long adder chains which gives rise to more propagation delay. The 4-bit multiplier is used to have reduced propagation delay. As per the UT sutra the 4-bit input is applied to four 2-bit multiplier and the output is of 8-bit.

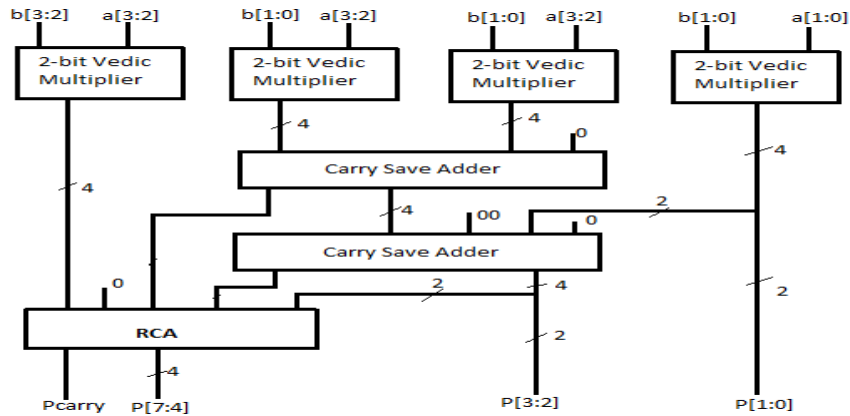


Figure 2 Design of 4-bit Multiplier.

C] Design of 8-bit multiplier

The proposed 8-bit multiplier is designed by using four 4-bit multiplier blocks and three 8-bit adders. The input to the 8-bit multiplier is 8-bit (Multiplicand) and the output obtained is of 16-bit wide. The output is applied to the four 4-bit multipliers. The output of 4-bit multipliers is given to the 8-bit adder.

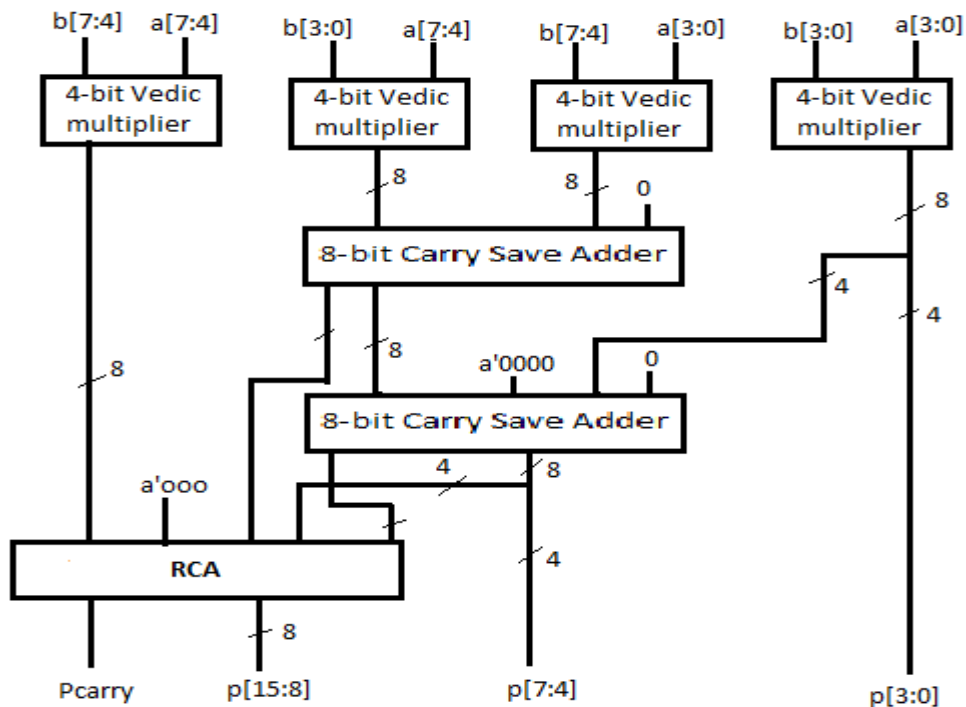


Figure 3 Design of 8-bit Multiplier.

IV. PERFORMANCE ANALYSIS

Performance analysis of the multiplier topologies presented in this paper is realized using the Tanner EDA tool, in 22nm CMOS process technology [1]. The schematics views of the topologies are obtained at power supply of 400mV, to analyze the power consumption and propagation delay. The results obtained are compared with different architectures to approximate the effectiveness of the proposed architectures [4] [6] [12]. The results are given in TABLE I-III. TABLE I gives the transistor count related with the topologies. The modified designs used for the AND



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gate ,the half adder and the full adder units provides the overall reduction in area of the multiplier architectures as these topologies utilize less number of transistors as opposed to the conventional designs.. TABLE II lists the propagation delays and power consumptions associated with the proposed designs, both for the schematic.

TABLE I. Transistor Count and Layout Area

Name of the topology	Transistor count
4-bit Multiplier of proposed Multiplier	320
8-bit Multiplier of proposed Multiplier	1616

A comparative analysis of propagation delays and power dissipation of different existing 8-bit multiplier architectures reported in the literature with the proposed architecture is presented in TABLE III. The comparison indicates that with respect to the different existing multiplier algorithms and architectures, the proposed design offers improved speed at considerably smaller power consumption with 0.4 volt power supply.

TABLE II. Propagation Delay and Power Consumption of different multiplier topologies

Name of the topology	Propagation Delay (in ns)	Power Consumption (in μ W)
4-bit Multiplier of proposed Multiplier	0.019	0.134
8-bit Multiplier of proposed Multiplier	0.408	0.776

TABLE III. Performance Comparison

Name of the topology	Power Supply in V	Propagation Delay (in ns)	Power Consumption (in μ W)
Proposed 8-bit Multiplier	0.4	0.408	0.776
[4]	1	0.635	7.460
[6]	--	21.5	--
[7]	--	22.216	--
[12]	--	18.532	--
[13]	2.5 to 5	14.13sec	9.386e-2

VI.CONCLUSION

The proposed paper presents new topologies for 4-bit and 8-bit multipliers based on UT sutra of Vedic mathematics. The topologies are realized in 22 nm CMOS process technology in Tanner EDA tool and the performance analysis is performed using with a power supply of 400mV. The multiplier designs proposed in this paper provides improvement in propagation speed and power consumption and the improvement in performance is achieved due to the new UT based architecture with fewer number of adder units with the use of modified circuits.



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