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A Short Channel Double Gate MOSFET Model

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ABSTRACT: There are several effects when the size of the transistor decreases and it challenges the limits of Si CMOS planar process technologies. The leakage current is one of the most important side effects of reduction in the size of the transistor. The scaling of the transistor involves the reduction in the Threshold Voltage, Channel Length and Gate Oxide thickness. This requires change from planar technology to 3-D transistor structures. Some solutions to these short channel effects are the use of new materials which have high – k and the design of new transistor models like FinFET double Gate devices. This paper presents new models of Double Gate FET with different high-k materials and Gate structures are developed and analyzed. The results indicated the improvement in the transistor performance in certain parameters.

KEYWORDS: Double Gate MOSFET, high-k materials, FinFET, Al Gate, leakage current.

I. INTRODUCTION

The integrated circuits (IC's) were invented in the year 1959 which eventually led to the birth and development of modern semiconductors industry. The IC's have enabled the development of new functional devices and gadgets that improved the way the world lives. In 1965 Gordan Moore predicted that the number of transistors per chip would quadruple every three year – famously know as Moore's law. Several new models, methods and materials have been introduced to continue the transistor road map for nodes from 90 nm to 14 nm or less.

It was a straight forward and inexpensive effort to migrate from one node to another node till the 14 nm node is reached. The foundry vendors introduced FinFET transistors from this node. In order to overcome lithography and performance gain challenges, new device structure for next generation technologies is used such as Silicon on Insulator(SOI) MOSFET and double gate (DG) MOSFET(to name a few). Double gate MOSFET is a type of FinFET device and provides significant advantages over the existing transistor designs [2]. Double gate FinFET is a promising candidate because of its quasi-planar structure, excellent roll-off characteristics and drive current. Also these are close to the present technology in terms of layout and fabrication techniques used to fabricate the MOSFET's [4].

Some main advantages of FinFET are:

- Reduced channel and gate leakage currents.
- Use of high –k materials to overcome tunneling.

II. DOUBLE GATE FET

The FinFET device consists of a thin silicon body, the thickness of which is denoted by T_{Si}, wrapped by gate electrodes. The current flows parallel to the wafer plane, whereas the channel is formed perpendicular to the plane of the wafer [5]. Due to this reason, the device is termed quasi-planar. The independent control of the front and back gates of the FinFET is achieved by etching away the gate electrode at the top of the channel.

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Figure 1: Double Gate MOSFET

This is shown in Figure 1. The presence of double gate provides electrostatic control over the channel in which the drain field line cannot effect or disturb the channel and it significantly reduces the short channel effects. In this design the Leakage current is reduced as the second gate acts like the substrate [6]. The Double Gate FET's (DG-FETs) are of smaller dimension as compared to the bulk type of transistors. The body in this transistor is left un-doped because this enhances the mobility ion transfer characteristic. This design also removes the drawback present in the present conventional model.

III. DEVICE DESIGN AND SIMULATION

This paper presents a modified and effective design of 45 nm Rectangular Double Gate FET (DG FET) and Curved Double Gate FET. Here high-k materials with relative dielectric greater than 4 are used to reduce the leakage current and to increase the performance of the device. Some of the high-k materials used with Al as Gate are Al_2O_3 and HfO_2, ZrO_2, TiO_2. These material changes have been found to improve the performance after scaling.
The Table 1 shows the properties of various materials used in the design of DG FET. As seen the relative dielectric values are generally more than 4 and up to a value of 80 for TiO_2. Also the Table details the comparison of several other electrical properties like thermal conductivity, electrical conductivity, specific heat and density.

Table 1:Specifications of High-k dielectric Materials

	SiO_2	Al_2O_3	HfO_2	ZrO_2	TiO_2
Relative dielectric	*3.90*	*9*	*25*	*24*	*80*
Thermal Conductivity (W/mk)	*1.38e+00*	*2.80E+01*	*2.20E+01*	*2.00E+00*	*7.4*
Electrical Conductivity (S/m)	*1.00E-15*	*1.00E-17*	*1.00E-12*	*3.16E-11*	*1.00E-13*
Specific Heat (J/kg K)	*7.09E+02*	*7.96E+02*	*2.61E+02*	*4.50E+02*	*6.90E+02*
Density (kg/m^3)	*2.20E+03*	*3.90E+03*	*9.68E+03*	*5.68E+03*	*4.95E+03*

As shown in Figure 1 & 2 the Source and Drain made up of Silicon material and Gate is made up of Al material. The use of Al as Gate material it reduces the tunneling current through base and increases the current from Source to Drain. Since the gates are independent, it provides a better control in the variation of threshold voltage can be obtained.

Figure 2: Curved DG MOSFET

The use of High-k material provides good electrical stability, and the amount of charge trapped in the high-k materials remain at a low level even after extended operation of a transistor. The material used should be scalable as it provides

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an acceptable level of electron and hole mobility even at reduced thickness. The MOSFET's using high-k materials can be used as high performance semiconductor devices.
As the leakage current increases, the thickness of the Gate Oxide material has to be increased to reduce these currents. An alternative method to increase Gate Capacitance is replacing the relative dielectric constant of the material Silicon Dioxide with a relatively high-k dielectric material. This will allow the use of thicker dielectric Gate layer which can be used to reduce the leakage current through the structure.
In FinFETs drain-conductance, g_d, is the change in the drain current divided by the change in the Gate to Source voltage with a constant Drain to Source voltage.

$$g_d = \frac{\partial I_d}{\partial I_g} \text{.....(1)}$$

The sub-threshold swing (SS) of a device is defined as the change in gate voltage which must be applied in order to create a one decade increase in the output current.
The Table 2 shows the values of the Drain conductance and sub-threshold swingof rectangular and curved double gate MOSFET for different high-k dielectric materials.

Table 2: g_d and SS of Rectangular and Curved DG MOSFET

Type	**k**	**Rectangle Gate**		**Curved Gate**	
		g_d	SS	g_d	SS
SiO_2	3.9	0.000143	-3.2E-05	0.000222	-0.000161
Al_2O_3	9	0.000121	-2.7E-05	0.000160	-3.5409E-05
HfO_2	25	0.000155	-3.4E-05	0.000401	-0.000291
ZrO_2	24	0.000111	-2.5E-05	0.000284	-0.000206
TiO_2	80	0.000158	-3.5E-05	0.000436	-0.000316

IV. RESULTS AND DISCUSSION

The electrical characteristics of the DG MOSFETs were simulated by varying the device parameters. The device parameters used are: channel length L = 45nm, Silicon thickness t_{Si} = 30nm, equivalent Gate Oxide thickness t_{ox} = 2nm, L_{sd} = 50nm, doping concentration of the silicon channel $N_A = 10^{16}$ cm^3, doping concentration of the Source and Drain contact regions $N_D = 10^{20}$ cm^3 and mid-gap metal gate with work-function of 4.28 eV. The lateral length of the Source and Drain contacts were considered small (all most zero) to avoid the influence of the series resistance on the Current–Voltage characteristics. The impact of high-k materials on the performance of DG MOSFET on both rectangular and curved gate types is studied.
It has been observed that the curved DG MOSFET has more control over the device characteristics than the regular rectangular DG MOSFET. The Curved Gate structure of the DG MOSFET showed improvement in the Drain conductance (g_d), early voltage and higher drive current. The simulation results proved that use of high-k materials in DG MOSFETs has significantly reduced the leakage current and has given better controllability.

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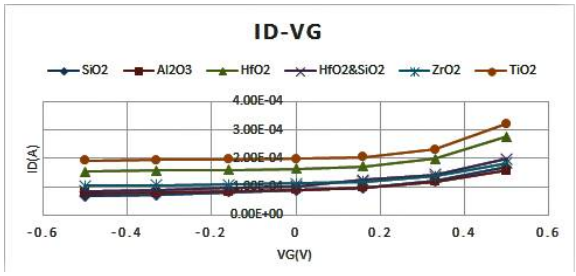

Figure 3: I_D-V_G of rectangular DG MOSFET (with Al-gate, V_{GB}=0.5V, l=45nm, t=2nm, N_D=2*$10^{20}$$cm^3$, L_{sd}=50nm, t_{ch}=30nm, at V_D=1V)

Figure 3 and Figure 4 shows I_D-V_G curves of rectangular and curved DG MOSFET for different high-k dielectric materials. From the graph we can infer that for the same gate voltage there is an increase in drain current for different high-k dielectric materials. The curved double gate FET (Figure 4) drives the drain current to a higher value compared to the rectangular double gate FET.

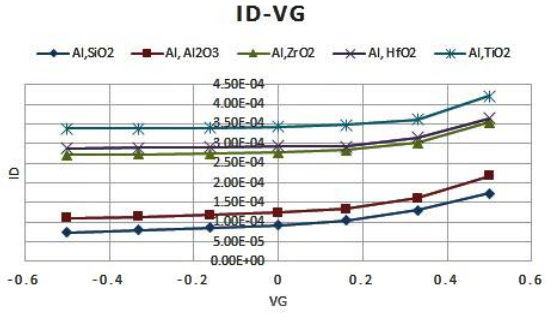

Figure 4: I_D-V_G of curved DG MOSFET (with Al-Gate, V_{GB}=0.5V, l=45nm, t=2nm, N_D=2*$10^{20}$$cm^{-3}$, L_{SD}=50nm, t_{ch}=30nm, at V_D=1V)

As the gate voltage increases, higher electron density is formed in channel due to increase in the local electric field along the position of the channel. In the DG FET movements of ions are more due to the potential applied from two gate terminals because of the lower resistance of the channel.

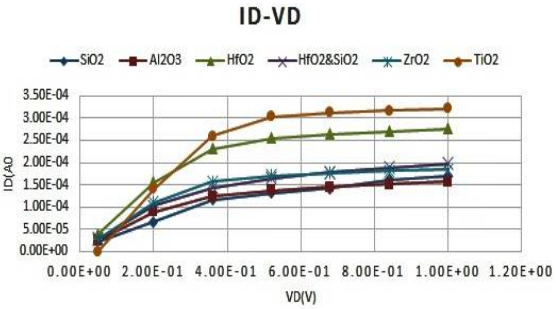

Figure 5: I_D-V_D of rectangular DG MOSFET (with Al-Gate, V_{GB}=0.5V, l=45nm, t=2nm, N_D=2*$10^{20}$$cm^{-3}$, L_{SD}=50nm, t_{ch}=30nm, at V_D=1V)

Figure 5 and Figure 6 shows I_D-V_D curves of rectangular and curved DG MOSFET for different high-k dielectric materials. The subthreshold leakage current (I_{off}) decreases and the I_{on} current increases with increase in dielectric constant.

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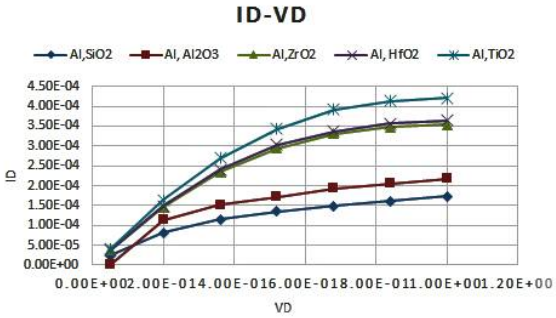

Figure 6: I_D-V_D of curved DG MOSFET (with Al-Gate, V_{GB}=0.5V, l=45nm, t=2nm, N_D=2*$10^{20}$$cm^{-3}$, L_{SD}=50nm, t_{ch}=30nm, at V_D=1V)

From the Figure 5 and Figure 6 the drain current is high for curved double gate FET compared to the rectangular double gate FET. From the graph we can infer that for the same drain voltage there is an increase in drain current for different high-k dielectric materials.

V. CONCLUSION

Curved and rectangular Double gate FinFET is designed for various gate dielectrics instead of SiO2 possible high-k materials are Al_2O_3 (k~9), HfO_2/ZrO_2 (k~25), TiO_2 (k~80) are used. The device performance is analyzed by replacing the SiO_2 with various high-k materials and the characteristics are analyzed for both rectangular and curved DG MOSFET. The curved DG MOSFET shows improved drain-conductance, early voltage and higher drive current. The simulation results prove that use of high-k materials in DG MOSFETs reduces the Off current and gives better controllability.

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