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Compression of Multilevel Inverter Based Different Higher Output Voltages Levels with Minimum Number of Switches

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ABSTRACT: this paper presents different types of multilevel inverters, known as symmetrical and asymmetrical multilevel inverter. Compared to diode clamped & flying capacitor type multilevel inverters cascaded H-bridge multilevel inverter requires least no. of components to achieve same no of voltage levels and optimized circuit layout is possible because each level have same structure and there is no extra clamping diodes or capacitors. However as the number of voltage levels m grows the number of active switches increases according to 2×(m-1) for the cascaded H-bridge multilevel inverters. Compared with the existing type of cascaded H-bridge multilevel inverter, the proposed a multilevel DC link MLDCL inverters can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases. Both types are very effective and efficient for improving the quality of the inverter output voltage. Firstly, we describe briefly the structural parts of the inverter then switching strategy and operational principles of the proposed inverter are explained and operational topologies are given. The proposed topology reduces the number of switches, losses, installation area and converter cost.Seven level, thirteen level and fifteen level proposed MLI is simulated using Matlab/Simulink environment and the corresponding results are presented in this paper.

KEYWORDS: Asymmetrical multilevel Inverter, Bidirectional switch, Total Harmonic Distortion (THD).

I.INTRODUCTION

Power electronic inverters are becoming popular for various industrial drives applications. In recent years, inverters have even become a necessity for many implementations such as motor controlling and power systems [1],[2]. The concept of utilizing multiple small voltage levels to perform power conversion was patented by an MIT researcher over twenty years ago [3]. The multi-level inverter system is very promising in AC drives, when both reduced harmonic contents and high power are required [4],[5]. Multilevel inverters have been mainly used in medium or high power system applications, such as static reactive power compensation and adjustable-speed drives [6],[7]. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter system for a high power application [8].

The concept of multilevel inverters was first introduced in 1975. The term multilevel began with the three-level inverter. Subsequently, several multilevel inverter topologies have been developed [3], [9]. Up to now, several topologies of multi-level inverter system have been introduced. The main topologies used to generate a high voltage waveform using low voltage devices are the series H-bridge design, diode clamped inverter system and flying capacitor inverter system. Each of these topologies has a different mechanism for providing the voltage level. Comparing with the other components, for instance, DC-link capacitors having the same capacity per unit, diode clamped inverter has the least number of capacitors among the multi-level inverter system topologies but it requires additional clamping diodes[4].The flying-capacitor topology followed diode-clamped after few years. Instead of series connected capacitors, this topology uses floating capacitors to clamp the voltage levels.[10] H-bridge inverters have isolation transformers to isolate the voltage source but they do not need either clamping diode or flying capacitor inverters. Also, some soft-switching methods can be implemented for different multilevel inverters to reduce the switching losses and to increase efficiency. Recently, several multilevel inverter topologies have been developed [11], [12],[13], [14].

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In this paper, authors propose a photovoltaic system based on fifteen-level PUC inverter suitable for a standalone application. Combined with the INCOND MPPT technique, the proposed system allows a good power quality in the load side with a good energetic conversion yield. Even the PUC inverter is constituted only from eight switches and two capacitors; it can nevertheless offer a fifteen-level output voltage [15].
A multiband hysteresis control technique is also performed to draw a nearly sinusoidal load current. This technique has been proven to be the most suitable solution for all the applications of current controlled voltage source inverters where performance requirements are more demanding, albeit at the expense of variable switching frequency [16].

II. MULTILEVEL INVERTER

The general structure of proposed new multilevel inverter is shown in the figure.1.

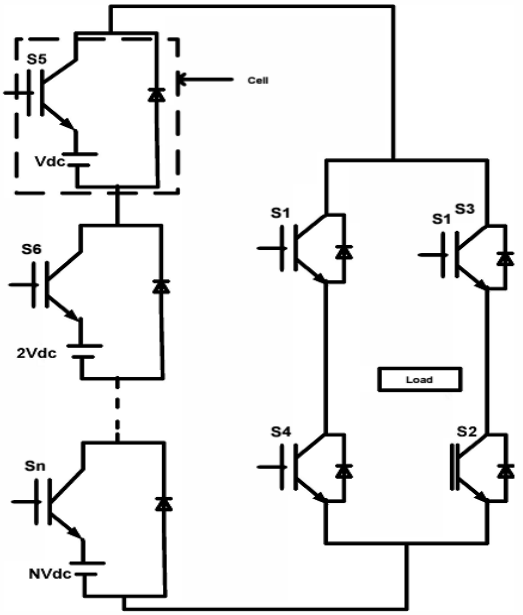

Fig.1. General Structure of proposed new multilevel inverter.

It consists of a one H-bridge inverter and 'N' number of cascaded cells, which are having a dc rating of V dc. The number of levels can be given by the formula:

Number of Levels = [n (n+1) +1]

Where n= Number of cells excluding the H-bridge. For generating + V dc we need turned on switches S I and S2, for -Vdc, switches S3 and S4 has to be turned on, and for zero voltage either switches Sl and S3 or switches S2 and S4 has to be turned on.

(a) Seven Level Proposed Multilevel Inverter: The seven level proposed inverter uses only six switches compared to cascaded H-bridge inverter which uses ten switches and three separate dc sources. But in proposed inverter, the requirement of separate dc sources is only two and the switching losses are also low. Using proper switching sequence proposed circuit generates seven levelsin output voltage [7]. Table I shows the switching sequence used for creating seven levels for the output voltage.
The output waveform has 7 levels: ± 3Vdc, ± 2Vdc, ± V_{dc} and 0. Circuit diagram of proposed seven level multilevel inverter is shown in figure.2.

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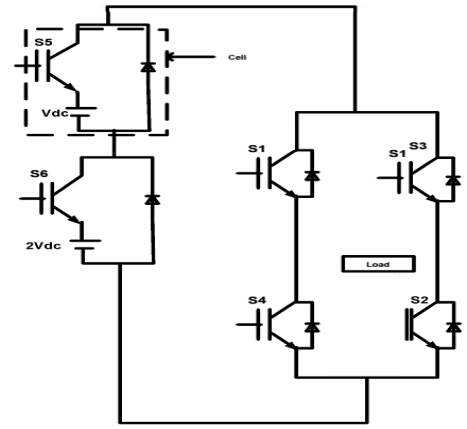

Fig.2.Circuit digram of seven level proposed inverter.

For generating seven levels, the proposed inverter uses two cells that mean it contains two switches and two diodes in addition with the one H-bridge. The output voltage waveform of the ideal seven level inverter is shown in fig .3.

Table. I Switching Sequence for Proposed Seven Levels Inverter

Sw1	Sw2	Sw3	Sw4	Sw5	Sw6	Load Voltage
On	On	off	off	On	off	V_{dc}
On	On	off	off	off	On	$2V_{dc}$
On	On	off	on	On	On	$3V_{dc}$
off	On	off	On	off	off	0
off	off	On	On	On	off	$-V_{dc}$
off	off	On	On	off	On	$-2V_{dc}$
off	off	On	On	On	On	$-3V_{dc}$

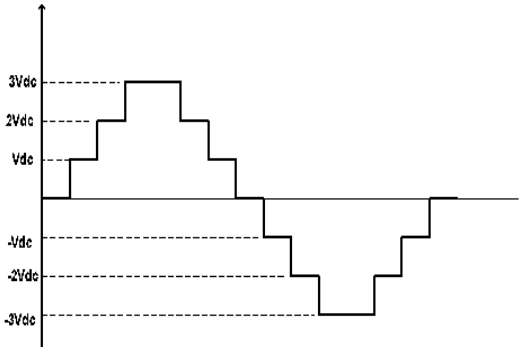

Fig.3. Ideal seven level output voltage waveform.

(b) Thirteen Level Proposed Multi level inverter: The thirteen level proposed inverter uses only seven switches compared to cascaded H-bridge inverter which uses twenty four switches and six separate dc sources. But in proposed inverter, the requirement of separate dc sources is only three and the switching losses are also low. Using proper switching sequence proposed circuit generates seven levels in output voltage. Table.II shows the switching sequence used for creating thirteen levels for the output voltage.

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Table.II.Switching Sequence for Proposed Thirteen Level Inverter

Sw1	Sw2	Sw3	Sw4	Sw5	Sw6	Sw7	V_{load}
On	On	off	off	On	On	On	$6V_{dc}$
On	On	off	off	off	On	On	$5V_{dc}$
On	On	off	on	On	off	On	$4V_{dc}$
On	On	off	off	off	off	On	$3V_{dc}$
On	On	off	off	off	On	off	$2V_{dc}$
On	On	off	off	On	off	off	V_{dc}
off	On	off	On	off	off	off	0
off	off	On	On	On	off	off	$-V_{dc}$
off	off	On	On	off	On	off	$-2V_{dc}$
off	off	On	On	off	off	On	$-3V_{dc}$
off	off	On	On	On	off	On	$-4V_{dc}$
off	off	On	On	off	On	On	$-5V_{dc}$
off	off	On	On	On	On	On	$-6V_{dc}$

Circuit diagram of proposed thirteen level multilevel inverter is shown in figure.4.

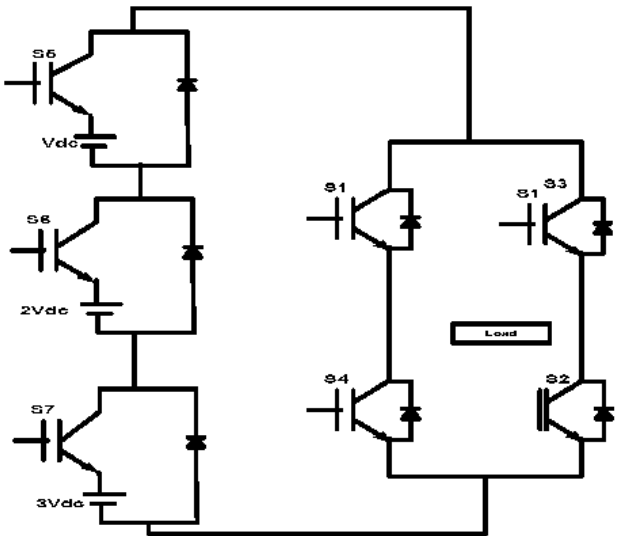

Fig.4. Circuit diagram of thirteen level proposed inverter.

The output waveform has 13 levels: ± 6Vdc, ± 5Vdc, ± 4Vdc± 3Vdc, ± 2Vdc, ± V_{dc} and 0. The output voltage waveform of the ideal thirteen level inverter is shown in fig.5.

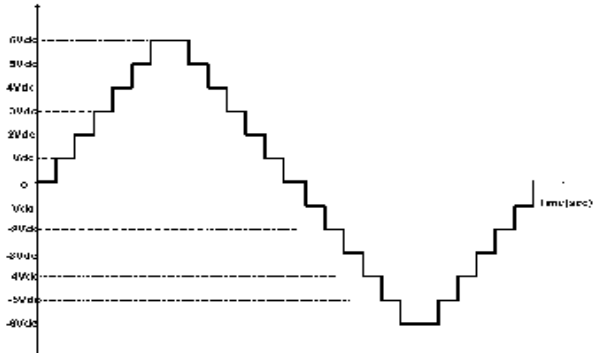

Fig.5. Ideal thirteen level output voltage waveform.

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III. PRESENTATION OF THE 15-LEVEL PROPOSED INVERTER

The Proposed inverter makes use of three DC sources as shown in Fig.6. The attainable output voltage levels depend merely on the ratios between these sources. Depicts them with their according switches pulses. Switches Ti and Ti operate complimentarily, thus, only Ti switches are considered in this table III.
As an application, we have chosen E1=700V, E2=300V and E3=100V. The load voltage is then constituted from fifteen levels as shown in Fig.14. The total harmonics distortion is around 13.30% as depicted in Fig.16. A loop effect is given in the same figure. With such waveform, filters can be then reduced or even avoided.

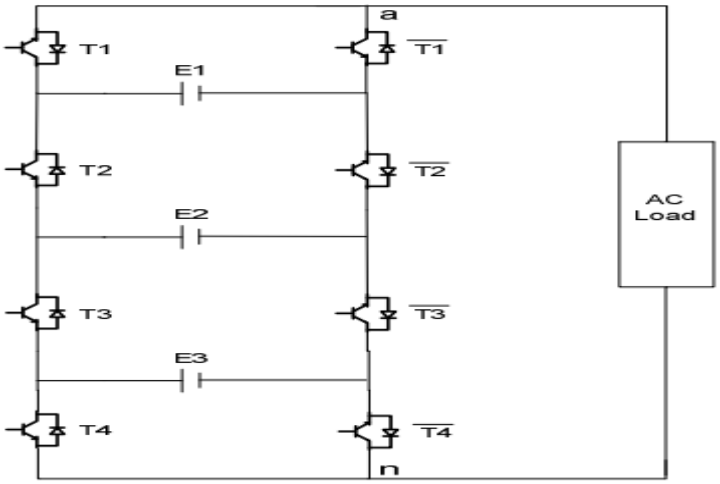

Fig.6. Proposed 15-Level Inverter.

TABLE III. Switching Table of the Proposed 15-Level Inverter

DC sources combination	Switches pulses			
	T1	T2	T3	T4
E1	1	0	0	0
E1-E2+E3	1	0	1	0
E1-E3	1	0	0	1
E1-E2	1	0	1	1
E2	1	1	0	0
E2-E3	1	1	0	1
E3	1	1	1	0
0	1	1	1	1
-E3	0	0	0	1
E3-E2	0	0	1	0
- E2	0	0	1	1
E2-E1	0	1	0	0
E3-E1	0	1	1	0
E2-E1-E3	0	1	0	1
-E1	0	1	1	1

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Table.IV.Comparisons between Different Topologies

TOPOLOGY	NUMBER OF SWITCHES for 7-level	NUMBER OF SWITCHES for 13-level	NUMBER OF SWITCHES for 15-level
Diode Clamped MLI	12	24	40
Flying capacitor MLI	12	24	40
Cascaded II-bridge MLI	12	24	40
Proposed MLI	06	07	08

IV.MATLAB/SIMULINK RESULTS

The following figures.7 shows the Matlab/Simulink diagram of proposed seven level MLI and its output voltage wave form.

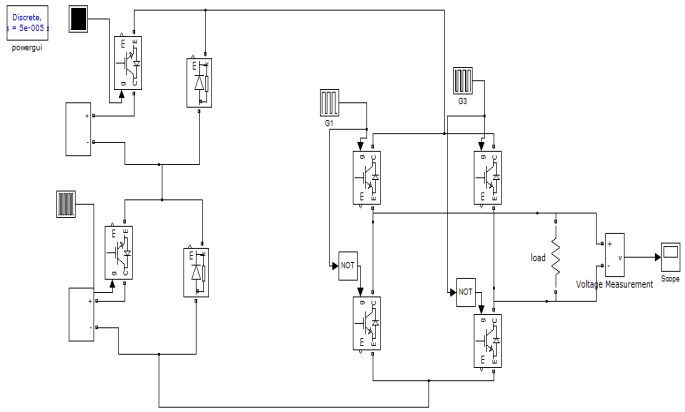
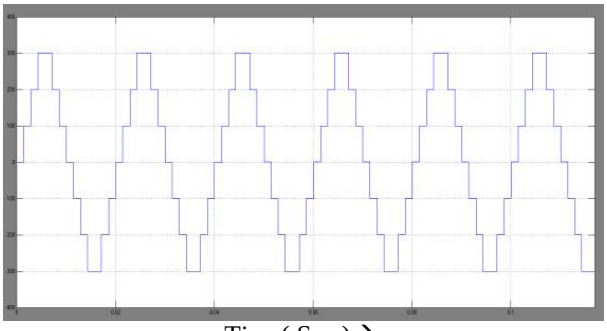


Fig.7.Matlab/Simulink Diagram of Proposed Seven Levels MLI.



Time(Sec.)→

Fig.8. Proposed seven level inverter output voltage.

From figure 8, it is observed that the output voltage of proposed MLI has seven levels with six switches and two diodes. The following figure 8 shows the spectrum analysis of seven level, here the output peak voltage is 300V and each stepping voltage is 300 /3 is 100V.

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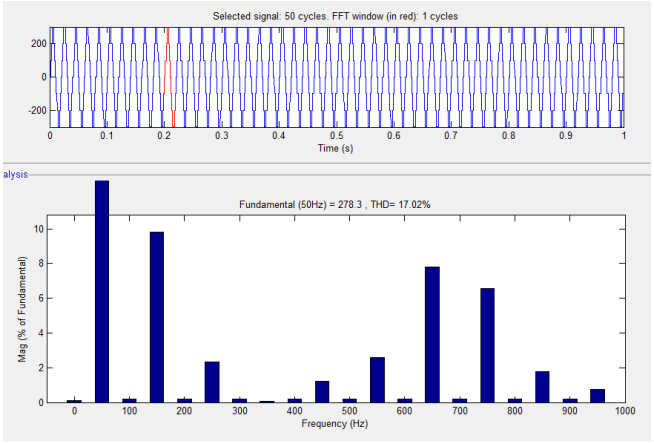

Fig.9. THD of the 7-level proposed inverter.

From figure 9, the THD of the proposed seven level inverter is 17.02%.The following figures.10 and 11 shows the Matlab / Simulink diagram of proposed thirteen levels MLI and its output voltage wave form.

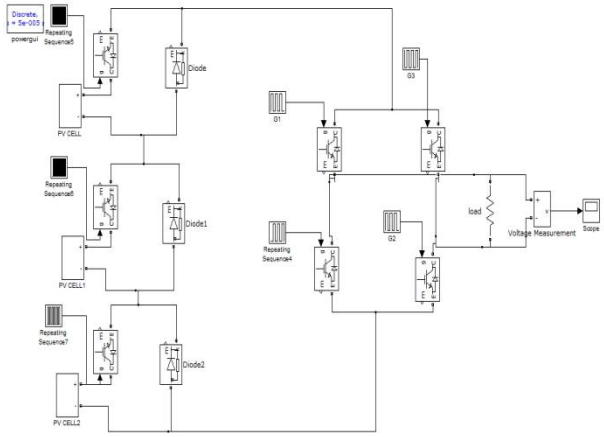

Fig.10. Matlab/Simulink diagram of proposed thirteen level MLI.

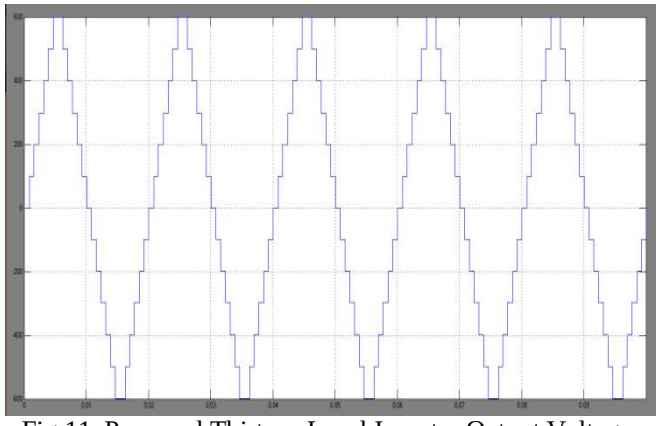

Fig.11. Proposed Thirteen Level Inverter Output Voltage.

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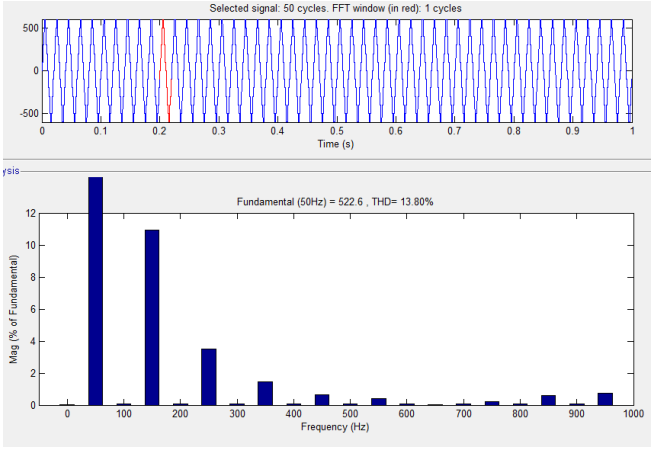

Fig.12.THD of the 13-Level Proposed Inverter.

From figure 12, the THD of the proposed 13 level inverter is 13.80%.

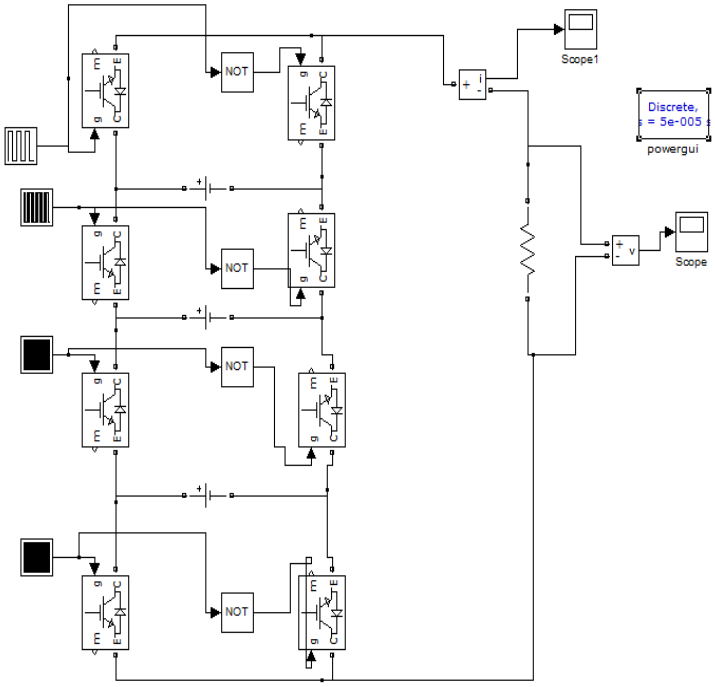

Fig.13. Matlab/Simulink diagram of proposed fifteen level MLI.

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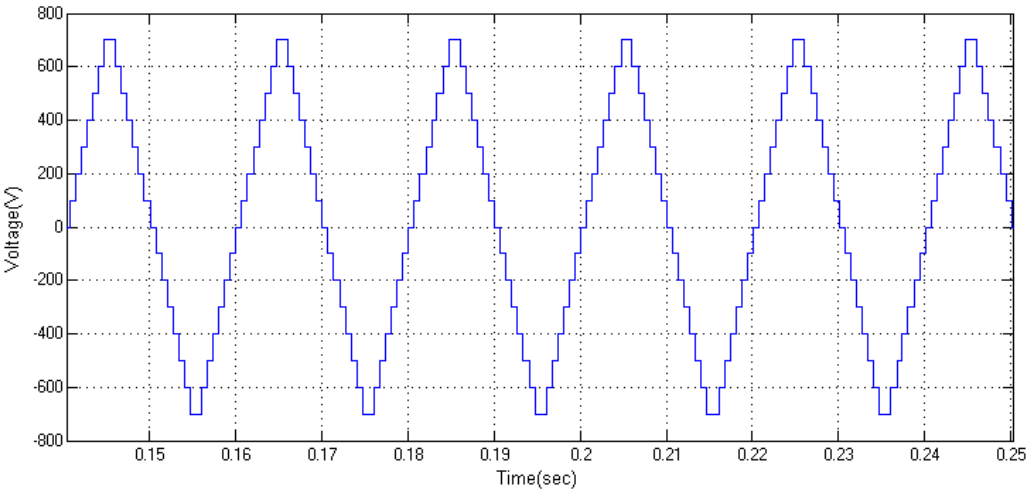

Fig.14. Proposed fifteen Level Inverter Output Voltage.

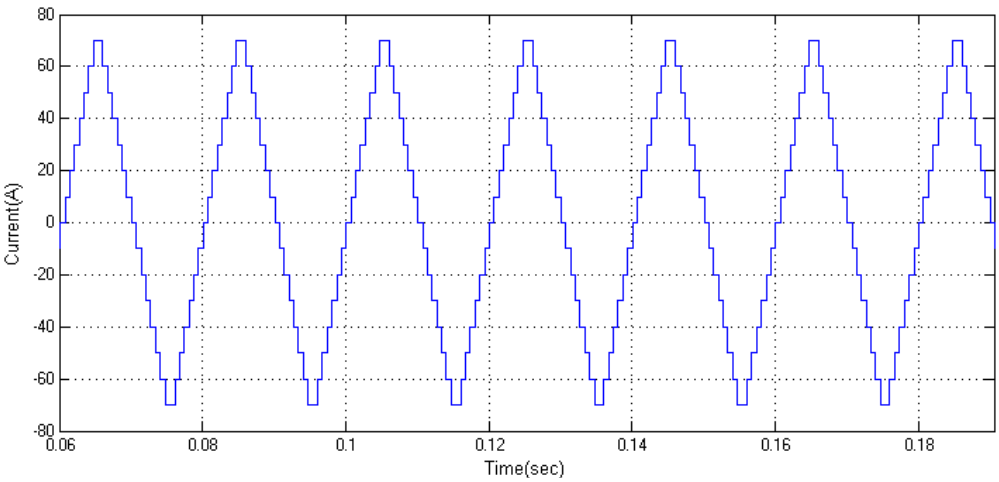

Fig.15. Proposed fifteen Level Inverter Output Current.

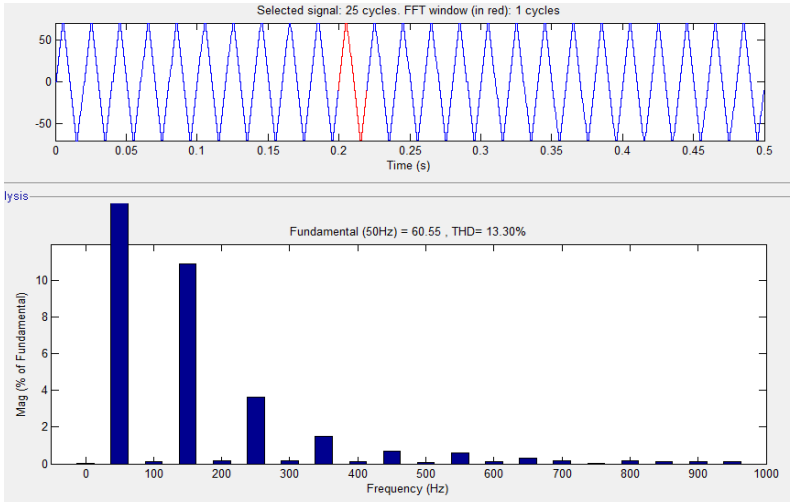

Fig.16.THD of the fifteen-Level Proposed Inverter.

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From figure 16, the THD of the proposed fifteen level inverter is 13.30%.

V.CONCLUSION

The seven, thirteen and fifteen levels of multilevel inverters are modelled and simulated using MATLAB/SIMULINK model. The multilevel inverter uses less number of switches as compared to conventional Multi level Inverters, hence the switching losses and cost of inverter is less. It is preferred that the output voltage has no lower order harmonics because their filtering is makes control complex. From the results, it can be concluded that grid inverter and grid connected loads are in synchronism with each other. Moreover, the magnitude of the blocking voltage of the switches is lower than that of conventional topologies. However, the proposed topology has a higher number of varieties of dc voltage sources in comparison with the others. From the values of percentage total harmonic distortion it can be concluded that as the number of levels of the inverter increases the percentage of the output THD value decreases. As the number of levels reach infinity, the output percentage of THD approaches zero but the cost involved in constructing the higher level inverter is high.

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