ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 6, June 2016

Design of Two Stage Operational Amplifier with High Gain and High CMRR in Deep Sub-Micron Technology

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ABSTRACT: This paper presents a CMOS two stage operational amplifier and a test schematic for Current Steering Digital to Analog Converter (CSDAC). The main aim of the work is to obtain high gain and high CMRR. The Operational amplifier operates at a supply voltage of 1.8v at 0.13 micron (i.e. 130nm). The operational amplifier provides an open loop gain of 68.053 dB and Common Mode Rejection Ratio (CMRR) of 122.974 dB, input common mode voltage ranging between 0.8 V to 1.6 V. The second part of the paper deals with test schematic design of binary weighted and generic CSDAC. The CSDACs designed operate at 1.8v supply using the two stage op-amp as an integral component and consumes power of 0.510mW. The design is carried out using Mentor Graphics tool.

KEYWORDS: Op-amp, CSDAC, DC Power.

I.INTRODUCTION

An operational amplifier (op-amp) is a direct coupled, high gain, differential amplifier. It is an integral part of many analog and mixed-signal systems.

Block diagram [1] of Op-amp is as shown in Fig. 1. The input stage consists of a differential amplifier which provides high CMRR, high input impedance and high voltage gain. The second stage is a gain stage which further increases the gain. Gain stage is a common source amplifier. Circuit symbol of op-amp is shown by Fig. 2. It consists of inverting input and non-inverting input with an output which is amplified version of difference in the inputs. It is a single supply op-amp, whose main advantage is reduced power. However the output voltage swing reduces compared to dual supply op-amp and lies between positive supply and ground. Op-amp characteristics are high open loop gain (ideally infinity), high Bandwidth (ideally infinity), high input impedance (ideally infinity), low output impedance (ideally zero), high CMRR (ideally infinity) and high PSRR (ideally infinity). Op-amp has wide range of applications ranging from filtering, dc bias generation, amplification and data conversion. General purpose applications include addition, subtraction,integration, differentiation, buffering and inversion.

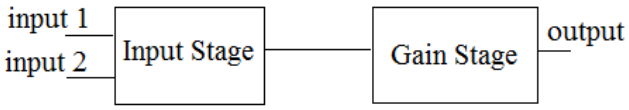

Fig.1. Op-amp Block Diagram

With the advancement in VLSI technology Digital Signal Processing has become more reliable and popular in almost all electronic applications. Digital systems have enormous advantages over analog systems like accuracy, speed, immunity to noise etc. Since all natural signals are Analog, we need an Analog to Digital Converter (ADC) to convert analog data into digital form. Then the digital data is processed using Digital Signal Processor and finally the processed data is

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ISSN (Online): 2278 – 8875

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Vol. 5, Issue 6, June 2016

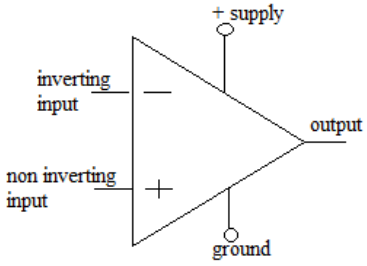

Fig.2. Circuit Symbol of Op-amp

Converted back to analog, using Digital to Analog Converter (DAC). DAC is an integral part of Digital Communication Systems for Data Conversion. DAC converts digital data into analog signal (usually current, voltage or electric charge). CSDAC is the preferred data converter, considering High Speed applications and High Power efficiency, over other DAC architectures.The CSDAC is designed ensuring that it provides acceptable accuracy and moderate power consumption.DACs are used in wide range of applications like Calibration Systems, Display Electronics, Data Acquisition Systems, Software radio, Data Distribution Systems, audio applications, communication and information systems etc. The suitability of various DAC in an application is decided based on various measurements including speed, area, power, resolution, output range, power supply requirement etc.

The outline of the paper is as follows. In section II design specifications, design requirements and design schematic of two stage op-amp is presented. Sections III and IV describes design procedure of binary weighted and generic CSDAC. Experimental results are given in section V and, conclusion is presented in section VI. At last, section VII gives future work, followed by references.

II.DESIGN OF TWO STAGE OPERATIONAL AMPLIFIER

A. DESIGN PROCEDURE

The two stage op-amp is designed using mentor graphics suite. Typical design specifications of op-amp is shown in Table I. Open loop gain of the op-amp is chosen high enough, such that closed loop feedback system achieves adequate linearity [3].

Steps in designing a CMOS op-amp are,

- Creating the basic structure of Op-amp
- Identifying the compensation required , satisfying specification
- Selection of the dc currents and transistor sizes
- Schematic implementation of the design

Two stage Op-amp [8] schematic is shown in Fig. 3, according to the op-amp features. Transistors M1, M2 dimensions are found from GBW. M3, M4 dimensions are found from maximum ICMR. Drain current through M5 is obtained from SR. M5 dimension is obtained from minimum ICMR. M6 and M7 respectively determine maximum and minimum output. C_C is called compensation capacitance or miller's capacitance whose value is very high. C_C is significant in obtaining the required positive PM, using dominant pole concept.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

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TABLE I
OP-AMP DESIGN SPECIFICATIONS

Specifications	Required value
Open Loop Gain (A_V)	≥60dB
GBW	≥35MHz
UGBW	≥30MHz
-3dB BW	≥10KHz
SR	20V/Us
ICMR+	0.8V
ICMR-	1.6V
DC Power	<1mW
PM	>60PM
L (Technology)	130nm
Supply	1.8v
CMRR	>100dB
PSRR	>100dB
C_C	800fF

The M1, M2, M3, M4 transistors form differential input pair circuitry, as the first stage. Transistors M5 and M7 are biasing transistors that ensure the circuit to operate in saturation region. Transistors M6 and M7 form Common source amplifier, which is the second stage. Inclusion of transistors M6 and M7 increases the open loop gain from 40dB to over 60dB.

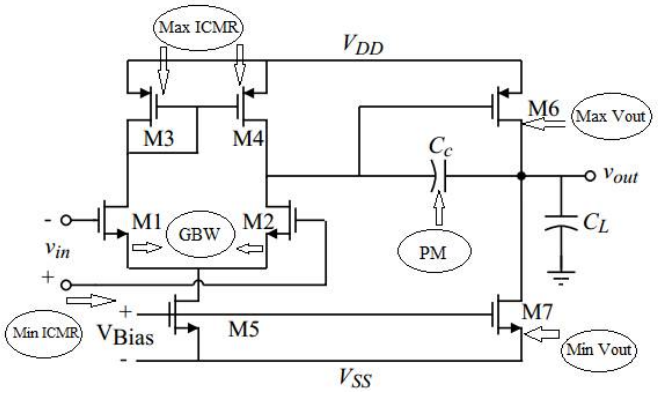

Fig. 3. Op-amp Schematic based on Specification

III.DESIGN OF FOUR BIT BINARY WEIGHTED CSDAC

A. DESIGN PROCEDURE

Binary weighted CSDAC uses binary weighted current sources. Structure of 4-bit Binary weighted CSDAC is as shown in Fig. 4, where digital input is fed through switches.

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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Vol. 5, Issue 6, June 2016

n-bit DAC needs only n current sources. It provides good current drive and also significant reduction in area, compared to generic CSDAC. However, for high resolution matching is difficult, due to switching errors. The output i_{out} is fed to an op-amp, which converts current to voltage.

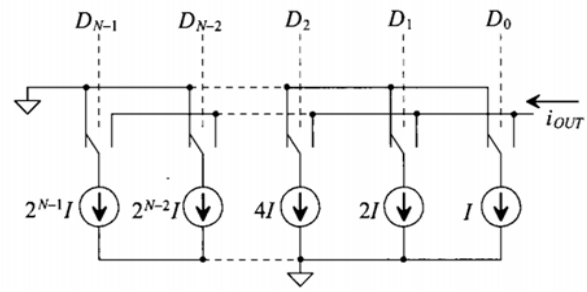

Fig. 4. n-bit binary weighted CSDAC structure

IV. DESIGN OF FOUR BIT GENERIC CSDAC

A. DESIGN PROCEDURE

Generic CSDAC uses n:$2^n - 1$ binary to thermometer Converter (thermometer encoder), which converts digital input to thermometer code, that drive the switches. Truth table of binary to thermometer encoder is as shown in Table III.

TABLE III
THERMOMETER ENCODER TRUTH TABLE

Binary	Thermometer
0000	000 0000 0000 0000
0001	000 0000 0000 0001
0010	000 0000 0000 0011
0011	000 0000 0000 0111
0100	000 0000 0000 1111
0101	000 0000 0001 1111
0110	000 0000 0011 1111
0111	000 0000 0111 1111
1000	000 0000 1111 1111
1001	000 0001 1111 1111
1010	000 0011 1111 1111
1011	000 0111 1111 1111
1100	000 1111 1111 1111
1101	001 1111 1111 1111
1110	011 1111 1111 1111
1111	111 1111 1111 1111

The number of bits required for a thermometer encoder is more than binary coded DAC design, however when the bit is high, they are advantageous. It is because there is only one bit change every time and thus avoids glitches. For example, when binary code switches from 0011 to 0100, three bits change simultaneously, but the corresponding thermometer codes switch from 000 0000 0000 0111 to 000 0000 0000 1111 i.e. change of one bit only and thus reduces glitches effectively. From the truth table the logical relationship can be expressed as follows,

t1=b1+b2+b3+b4
t2=b1+b2+b3
t3=b1+b2+(b3*b4)
t4=b1+b2
t5=b1+b2*(b3+b4)
t6=b1+(b2*b3)
t7=b1+(b2*b3*b4)
t8=b1

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ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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t9=b1*(b2+b3+b4)
t10=b1*(b2+b3)
t11= b1*(b2+(b3*b4))
t12=b1*b2
t13=b1*b2*(b3+b4)
t14=b1*b2*b3
t15=b1*b2*b3*b4

For binary codes b1 is MSB and b2 is LSB. t15 is MSB and t1 is LSB for thermometer codes. Output of thermometer encoder needs $2^n - 1$ current sources. Thus there is area overhead, however, it provides good matching and improves layout regularity, as current sources are equal and of unit value. Structure of n-bit Generic CSDAC is shown in Fig. 5.The output i_{out} is fed to an op-amp, which converts current to voltage.

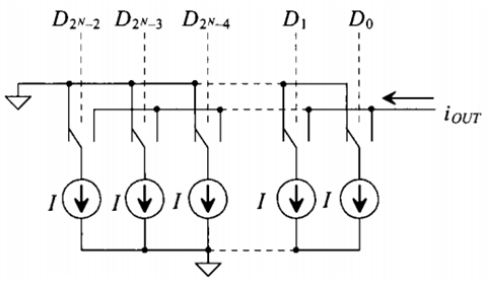

Fig. 5. n-bit generic CSDAC

V. EXPERIMENTAL RESULTS

Mentor graphics tool mapping for two stage op-amp design is shown in Table IV. Pyxis schematic provides complete environment to capture and simulate IC designs. Analog simulator used is eldo, which supports numerous analyses such as, DC analysis, AC analysis, Transient analysis, Sweep analysis etc.

TABLE IV
MENTOR GRAPHICS TOOL MAPPING FOR OP-AMP DESIGN

Design Action	Tool Name
Schematic Entry	Pyxis Schematic
Symbol Creation	Pyxis Schematic
Simulation	Eldo AMS

A. OPERATIONAL AMPLIFIER MEASUREMENT RESULTS

Schematic of two stage op-amp is as shown in Fig. 6. The first stage is a differential amplifier, followed by a common source amplifier. C_C is the coupling capacitor. It is miller's capacitance, used to obtain required phase margin.

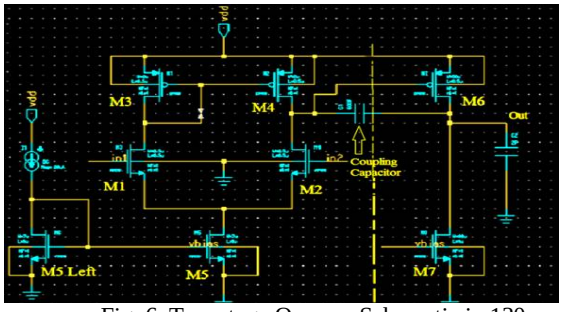

Fig. 6. Two stage Op-amp Schematic in 130nm

Symbol of two stage op-

ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

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amp is as shown in Fig. 7. “inv” is inverting input and “non inv” is non-inverting input. “vdd” is the supply and “out” represents output voltage.

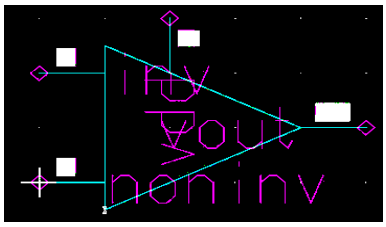

Fig. 7. Symbol of Schematic model

Channel width for MOS transistor is shown in Table V. To avoid channel length modulation effects, a large value of L, close to 1μm was chosen during design.

TABLE V
CHANNEL WIDTH FOR MOS TRANSISTOR DESIGNED FOR 130NM TECHNOLOGY OP-AMP

MOS Transistor	Channel Width	Aspect Ratio (W/L)
M1	0.65	5
M2	0.65	5
M3	0.52	4
M4	0.52	4
M5	0.91	7
M5 Left	0.91	7
M6	13	100
M7	11.44	88

Simulated AC analysis of two stage op-amp is shown in Fig. 8. Open loop gain ($A_{V)}$ is 68.053 dB**.** It has GBW of 37.873 MHz, UGBW of 35.228 MHzand PM of 65.578°. Positive phase margin ensures stability. UGBW is the bandwidth of the op-amp when the gain is 0 dB and GBW is the product of open loop gain and -3 dB BW. –3 dB BW is the cut-off frequency (f_c) of the Op-amp. UGBW and GBW product helps the designer to find the maximum gain that can be extracted from the op-amp for a given bandwidth.

Fig. 8. AC analysis of Op-amp

Simulated Transient analysis of two stage op-amp is as shown in Fig. 9. The input is a sine wave, fed to inverting terminal and thus output is inverted version of input. Here we notice that the output is the amplified version of the input.

ISSN (Print) : 2320 – 3765
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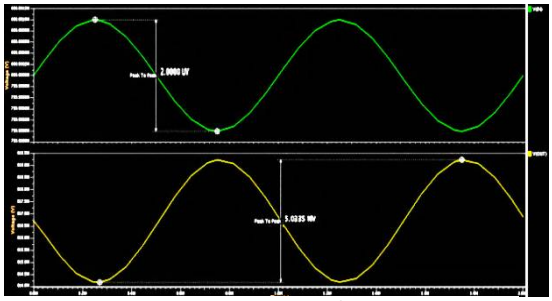

Fig. 9.Transient analysis of Op-amp

Comparison between actual value and simulated value is shown in Table VI. The simulated value of the design meets all the specifications. After tuning, the compensation capacitor is reduced to 600fF. DC power is obtained from DC analysis as 0.511mW. We may further tune the design components and achieve gain higher than 68dB. CMRR is the ability of the op-amp to supress common mode signals. CMRR of 122.974 dB obtained ensures, a high level of noise cancellation. PSRR is power supply rejection ratio [7], which is the ability of the Op-amp to reject the amount of noise from the power supply. PSRR of 145.989dB guarantees that the device is highly immune to supply noise.

TABLE VI
COMPARISON BETWEEN THEORETICAL AND SIMULATION RESULT

Specifications	Actual value	Simulated value
Open Loop Gain (A_V)	≥60dB	68.053dB
GBW	≥35MHz	37.873MHz
UGBW	≥30MHz	35.228MHz
-3dB BW	≥10KHz	14.986KHz
SR	20V/μs	20V/µs
ICMR+	0.8V	0.8v
ICMR-	1.6V	1.6v
DC Power	<1mW	0.511mW
PM	>60PM	65.578°
L (Technology)	130nm	130nm
Supply	1.8v	1.8v
CMRR	>100dB	122.974dB
PSRR	>100dB	145.989dB
C_C	800fF	600fF

B. BINARY WEIGHTED CSDAC MEASUREMENT RESULTS

Schematic of 4-bit binary weighted CSDAC is as shown in Fig. 10. It uses four DC current sources and all the switches are assumed to be closed, so that the digital input is 1111. DC power dissipation is 0.510mw

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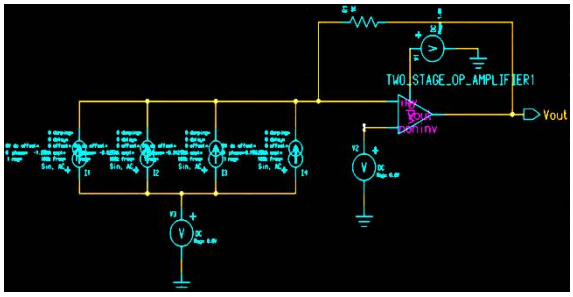

Fig. 10. 4-bit Binary weighted CSDAC

The analog output is given by $V_{out}= (D.V_{ref})/2^n$, where D - digital input, V_{ref} - reference voltage, n - number of bits. The theoretical output value for D=1111 input is 4.6875µV, with reference as 5µV. Simulated transient analysis of 4-bit binary weighted CSDAC is shown in Fig. 11. As seen from the transient analysis the output is 4.6428µV**,** which is nearer to the theoretical value.

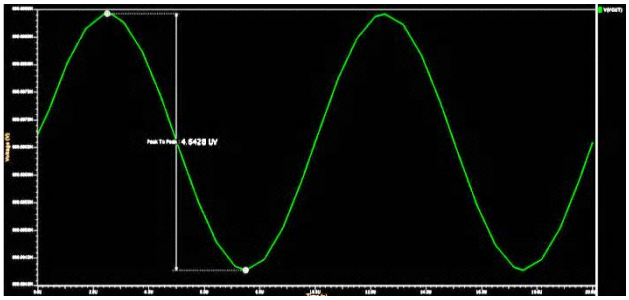

Fig. 11.Transient analysis of binary weighted CSDAC

C. GENERIC CSDAC MEASUREMENT RESULTS

The basic component of generic DAC or Unary DAC is thermometer encoder. Schematic of 4-bit thermometer encoder is shown in Fig. 12. Here we add inverters to obtain similar delay time in every branch of encoder. Inverter is added in pair to retain the logic.

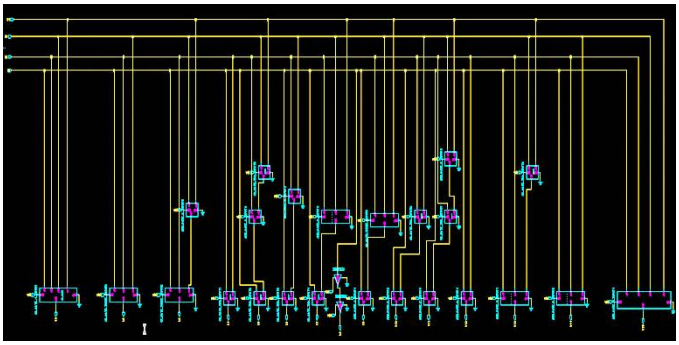

Fig. 12. 4-bit thermometer encoder

Simulated transient analysis of 4-bit thermometer encoder is as shown in Fig. 13. Here bit duration is 50nS and thus transient time duration is from 0 to 800nS. We notice glitches at some instances, which is due to overlapping of rise/fall times of certain input pulses. We may reduce the glitches to zero by adjusting rise/fall times of the input pulse. However they don't affect the circuit operation.

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International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

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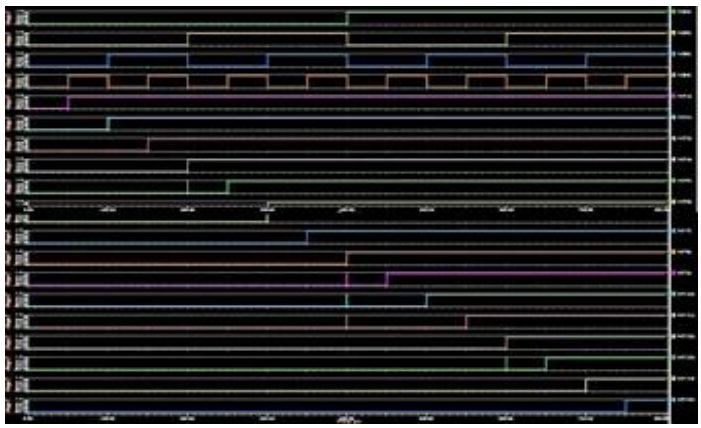

Fig. 13 Transient analysis of 4-bit thermometer encoder

Schematic of 4-bit generic CSDAC is as shown in Fig. 14. It uses fifteen DC current sources and all the switches are assumed to be closed, so that the thermometer encoder input to switches is 111111111111111. Thus with digital input 1111, we have DC power dissipation 0.510mW.

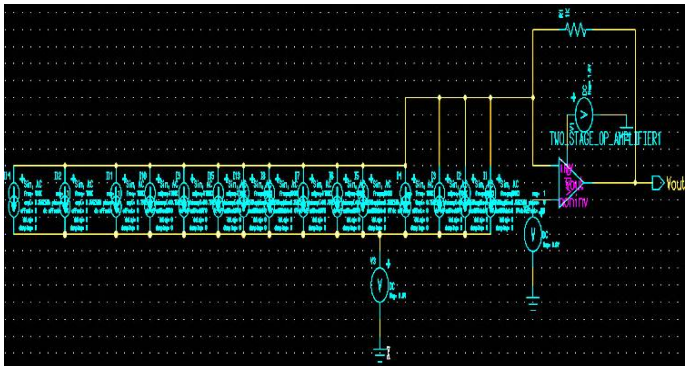

Fig. 14. 4-bit generic CSDAC

The analog output is given by $V_{out}= (D.V_{ref})/2^n$. The theoretical output value for D=1111 input is 4.6875µV, with reference as 5µV. Simulated transient analysis of 4-bit generic CSDAC is shown in Fig. 15. From the transient analysis the output voltage is 4.6429µV, which is nearer to the theoretical value.

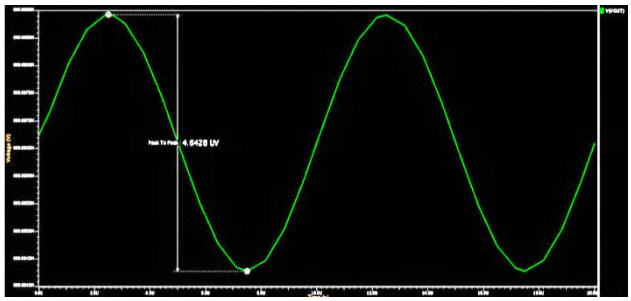

Fig. 15.Transient analysis of generic CSDAC

VI. CONCLUSION

Two stage Op-amp, 4-bit binary weighted and generic CSDAC is designed and simulated in 0.13μm technology using mentor graphics design suite.The main objective of the paper was to design a high gain and high CMRR two stage Op-amp. CMRR is as high as 122.974 dB and with proper tuning of C_C, the gain is highly improved, maintain the stability.

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The op-amp ensures proper operation within input common mode voltage ranging from 0.8V to 1.6V. The op-amp offers good stability with Phase margin of 65.578°. DC power dissipation of the Op-amp also meets the specification and is as low as 0.511mW. Finally, this op-amp is integrated into 4-bit binary weighted and generic CSDAC, for data conversion applications.

VII. FUTURE WORK

The two stage op-amp performance metrics can be improved by gain boosting topologies [3],using buffered op amps, current feedback op-amps [7] etc. Design of CSDAC by replacing current sources by CMOS current mirror is a challenging task. So, this work can be extended for future applications that require CSDAC for high speed applications

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