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Generating Timing and Control Signals for Radar applications Using Spartan 3E

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ABSTRACT: The present work is aimed to fabricate a function generator to meet the requirements of control and process signals to be applied on to several basic constituting functional units of a radar system. The functional units of Radar system includes Exciter, Receiver, Radar Controller, TCSG, Duplexer Antenna .The synchronized pulses generated are operate on functional units is accomplished by generating a reference pulse known as" Inter pulse period". The controlled pulses in the radar systems are categories as Exciter pulse, Transmit pulse, Gating pulse, Blanking pulse and they are generated with respect to "Inter pulse period". All these functions of the different control signals generated for the functioning of radar is conveniently replaced in the present work by FPGA system using Spartan 3E.

KEYWORDS: Timing and control signal generator (TCSG), Ethernet PHY, Spartan 3E FPGA

I. INTRODUCTION

The Spartan-3E of Field-Programmable Gate Arrays (FPGA) systems is particularly intended to meet the necessities of high volume, and practical buyer electronic applications. The execution of FPGA framework can be improved with the acquaintance of day with day changes in their application highlights with practical inclination. The application particular coordinated circuits (ASIC) are additionally utilized to meet the prerequisites of diverse control signs to control and keep up the working of frameworks for the successful working of Radar System. The Spartan-3E is a better option than veil modified ASICs. FPGAs evade the high introductory expense, the protracted improvement cycles, and the innate rigidity of customary ASICs. FPGA programmability licenses outline redesigns in the field with no equipment substitution which is an in conceivable possibility with ASICs. The proposed work to control and process the functioning of Radar and its signals are generated. A ring of IOBs surrounds a regular array of CLBs. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the centre with two at the top and two at the bottom of the device. Interconnect all five functional elements, transmitting signals among them. The main target of this paper is generating timing and control signals to be implemented on to FPGA using xc3s500e to be configured on Spartan 3E.

In this paper, it proposes the reference signal "Inter pulse period" is generated and other signals like Exciter pulse, Transmit pulse, Gating pulse, Blanking pulse are generated with respect to "Inter pulse period". VHDL coding is written for all the signals with different on and off periods by using Spartan 3E.

II. TIMING AND CONTROL SIGNAL GENERATOR (TCSG)

The Timing and control signal generator system generates inter pulse period (IPP) which will be used as a reference to generate different timing and control signals for the operation of various functional units. Timing signals are used to switch different RF switches in both transmit and receive paths where the timing and control signals are used to generate different timing pulses in both transmit and receive paths.

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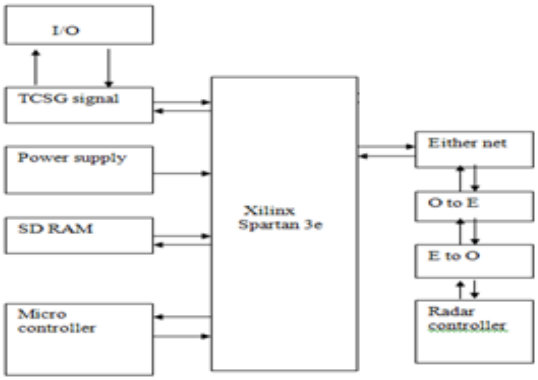

Figure 1 Functional Block diagram of TCSG

The functional blocks are employed in the present work of the present work is shown in figure 2. The communication between radar controller and TR module through Ethernet is depicted. Ethernet provides communication among indoor subsystems. The optical communication between outdoor TR modules is achieved. The interfacing of transmitter and receivers is achieved by Ethernet PHY. Functional block diagram of Ethernet PHY (KSZ 8041TL) is shown figure 2.

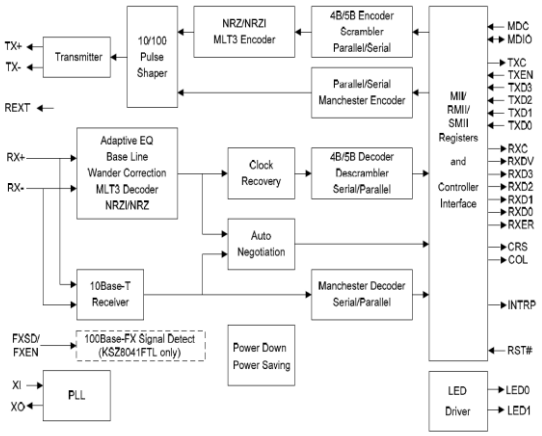

Figure 2 Functional block diagram of Ethernet PHY.

The KSZ8041TL is a single 3.3V operated Fast Ethernet transceiver. On the media side, the KSZ8041TL supports 10Base-T and 100Base-TX with HP auto MDI/MDI-X for reliable detection and Correlation for straight-through and crossover cables. The KSZ8041TL offers a choice of MII, RMII, or SMII data interface connection to a MAC processor. The MII management bus option provides the MAC processor have control over control and status registers. The Interrupt mechanism available in the system bypasses the MAC processor. During The PHY status change, the tranceiving signals are directed with the help of already designed analog circuits. In addition the capability of the performance of the system increases with low power consumption with smaller chip design.

III. OPTICAL DISTRIBUTION NETWORK

The optical distribution network system employed in the present work is shown figure 3. The distance provided between out-door TR module and RC is 140m, for effective communication and control TR modules, which are

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carried out between through optical distribution network. Each TR module needs 16 MHZ CLK and IPP Trigger pulse from the TCSG distribution scheme.

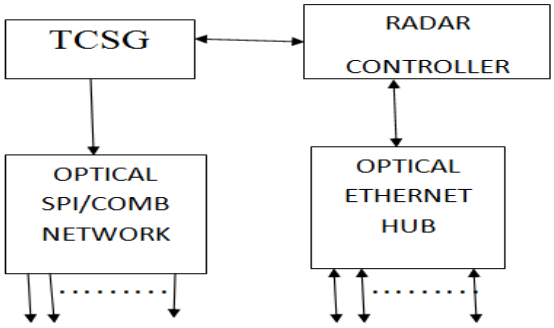

Figure 3 Optical distribution for timing and control signals.

Optical filaments are utilized to convey the Ethernet-Tx, Ethernet-Rx, IPP and CLK signals from the indoor RC to outdoor TR modules. Optical strands are likewise used to convey two extra RF signals, Cal-Tx and Cal-Rx, between the radar controller and TR modules. TR modules of every sub gathering are joined with one 24 port Giga bit Ethernet switch. This switch is shown Figure 4.

Figure 4 Electrical and optical switch

The 16 MHZ CLK Signal and IPP Signal generated by the TCSG are first distributed in electrical domain and then converted into optical signal for transmittance. Optical signal are routed to the respective TR modules through fiber optic cable.

IV. DISTRIBUTED TIMING CONTROL SIGNAL GENERATOR

TR modules are located at out-door field consists of a Xilinx Spartan 3E based TCSG card for control, Communication and monitoring purposes. TCSG card contains the main control unit (MCU) and fiber transceiver unit (FTU). FTU translates the optical domain signal into electrical domain by using optical receivers. MCU is the CPU system with FPGA, ADCS, Micro controller and other circuitry controlling and monitoring purposes. RC pre-loads the user specified experimental parameters in to the TR modules. Depending on the data received from the RC, generates all the timing and control signals based on 8 bit MCU compatible with 8051 family. SDRAM with 64 Mbytes that is used for program execution, it is accessed by Micro Blaze using Multi-Port Memory Controller.

V. IMPLEMENTATION

In this paper, the FPGA proposed strategy is employed along with the Xilinx Spartan3E system is reported .This technique is developed for the functioning of a system as a dedicated processor framework. This system can be attributed as the combination of hardware and software technologies. The hardware component comprises of microprocessor hardware, and allied system .The software is due to HDL Programs of Spartan 3E FPGA system.

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VI. FLOW CHART

The simulation procedures are depicted as a flow chart mention below in figure 5.

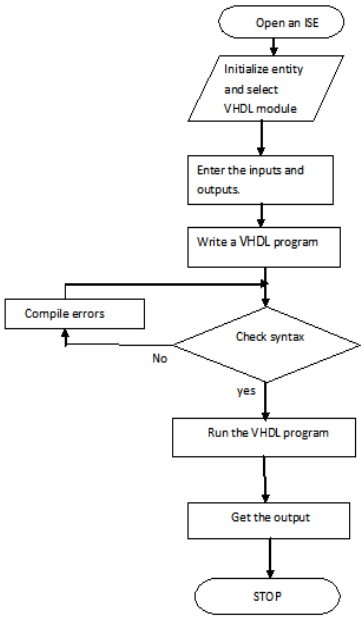

Figure 5 Flowchart

VII. SIMULATION STEPS

The procedure for simulation is as follows:

1. Open a new file and create a new Project. Select the appropriate properties for Spartan 3e device.
2. Create a new source file for VHDL module.
3. Write the VHDL coding and check for syntax errors.
4. Again select a new source file and create a test bench for generating a clock.
5. Run the program and we get the simulation results.

VIII. SIMULATION RESULTS

The controlled pulses required for operation of basic functional units in a radar system with respect to a standard "Inter pulse period" is as follows

Reference pulse = 1us
Tx pulse = 8 us
Blanking pulse = 12 us
Gating pulse = 8 us

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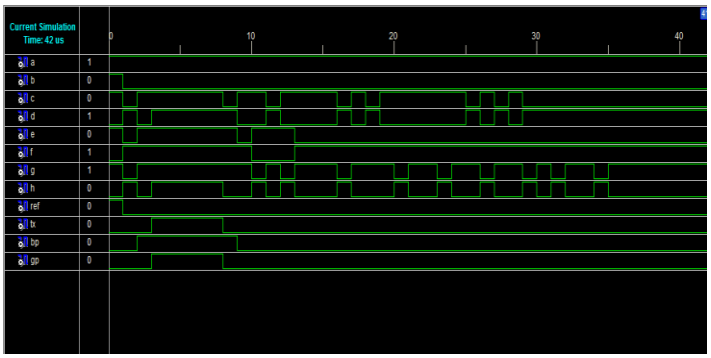

IX. CONCLUTIONS

The timing pulses are generated for effective functioning of Radar system with different time periods are reported. The simulation and configuring FPGA of Spartan3E.This procedure presented is flexible, easy and trustable methodology for effective operation. The configured system can be programmed depending up on requirements by making necessary modifications.

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BIOGRAPHY

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