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Tunnel Field Effect Transistors for Ultra Low Power Applications

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ABSTRACT: In this Work, the analog performance is analyzed for a double-gate n-type tunnel field-effect transistor (DG n-TFET) with a relatively small body thickness (10 nm), which shows good drain current saturation. In DG n-TFET, to increase the on-current value and to reduce ambipolar nature is done by improving the device parameters such as Transconductance$g_m$and intrinsic gain. The device performance of Hetro Double Gate Double Metal Double Oxide n-TFET is compared with DG n-TFET and it shows better performance in the on-current value, device gain and Transconductance (g_m)when used for using ultra low power applications. The Device structure and its parameters in Tunnel FET can be validated by using Technology Computer Aided Design (TCAD).

KEYWORDS: Analog performance, band-band tunneling (BTBT), Double gate n-TFET (DG n-TFET) complementary TFET (CTFET).

I.INTRODUCTION

The Subthreshold Swing SSlimit (~ 60 mv/decade at roomtemperature) for a MOSFET having major disadvantage for further scaling its power supply voltage. The TFETs are the gated p-i-n diode and ambipolar device. The changing voltage polarities using same device is used to N-TFET or P-TFET.the basic principle is based on the Band-to-Band tunneling (BTBT) mechanism. The S-limitation is overcome by using DG-nTFET. TFETs are suffered their low on-current and high leakage current, so improve by use of SiGe in source region, a double gate(DG) architecture, a high-k-die-electric, thin silicon body which makes the very attractive in replacing MOSFET for extending Moore's law. To further increasing on-current and reducing off-current using DG-Ntfet structure.In this paper we analyzed the performance of a DG-nTFETcompared with Hetro Double Gate Double Metal Double Oxide n-TFET.

II.DEVICE STRUCTURE ANDSIMULATIONS

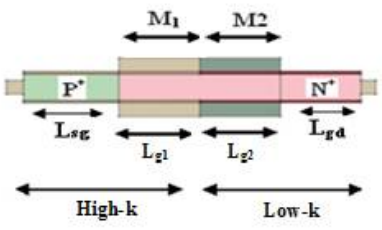

Fig.1.Device Structure for Hetro Double Gate Double Metal Double Oxide n-TFET.

Two-dimensional device simulations are done for theHetro Double Gate Double Metal Double Oxide n-TFET structure using TCAD simulations. The device dimensions are specified by a metallurgical channel length 50nm and the source

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to gate length and gate to drain length is 30nm, theequalient oxide thickness of the gate die-electric is 1nm and gate leakage is negligible in this simulation. The source and Drain contacts are made of aluminumand the gate contact is made of a two metals M_1 is using aluminum and M_2 is usingMolybdenum. The doping concentrationfor the source (p type) 9×10^{19} atoms/cm^3 and Drain (ntype) both regions. The intermediate channel region is made of a moderately doped (1×10^{17} atoms/cm^3)n type layer. The results presented here are TCAD simulations. Although the use of an abrupt doping profile in the device or an alteration in the model parameters for the BTBT model results in some variation in the simulated current levels. We therefore focus more on the general trends and orders of magnitude rather than on the exact values of thedifferent performance parameters in this paper. The source to gate made up of High-k material and gate to drain made up of low-k material. Source material using InAsand drain and channel are using Silicon. In this paper compare DG n-TFET andHetro Double Gate Double Metal Double Oxide n-TFET.

III. RESULTS AND DISCUSSION

A.OUTPUT CURRENT SATURATION MECHANISM:

The current in a TFET strongly depend upon the drain potential V_{DS} for its low values. To investigated the good drain current saturation for DG-nTFET.the V_{DS} small value only take good current saturation by using V_{DS}=0.2V.The simulated device characteristics for the DG-nTFET structure find out gate drive voltage $V_{GT}=V_{GS}-V_T$ used further increasing V_{DS}does not increase I_D.V_T=0.55V pinch-off voltage=1.0V for V_{GT}=0.5V that V_{GS}=1.05V.At low V_{DS} that gate potential induces an accumulation in the channel, which is populated with electrons supplied by the drain.V_{DS} increased 0.8 to 1.0V electron concentration in the channel rapidly decreases more and pulled back to the drain.

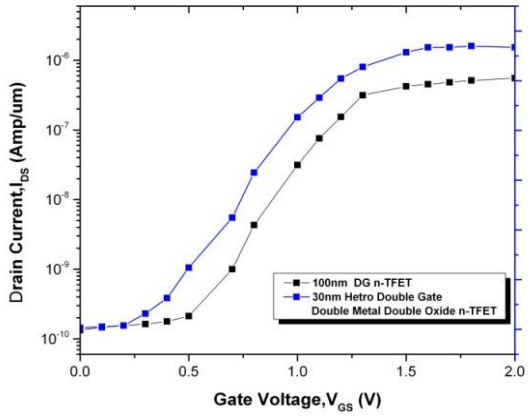

Fig.2. (a) I_{DS}-V_{GS} Characteristics of Existing DG n-TFET and Proposed Hetro Double Gate Double Metal Double Oxide n-TFET.

Fig.2. (a) shows the I_{DS}-V_{GS} Characteristics of Existing and Hetro Double Gate Double Metal Double Oxide n-TFET. The Existing device to given V_{GS}=2.0V achieve the drain current is $5x10^{-7}$and proposed device matches V_{GS} given achieving the drain current is $5.6x10^{-6}$. So, the proposed device is having the better performance compared to Existing Structure Double Gate n-TFET (DG n-TFET).

For large V_{DS} lateral electric field from drain can't penetrate. The Drain Induced Barrier Lowering (DIBL) is absent this device. TFET independent of channel length down to about 20nm.The drain current based on the different V_{DS} values. To give the V_{DS} to drain region only current flow the device.

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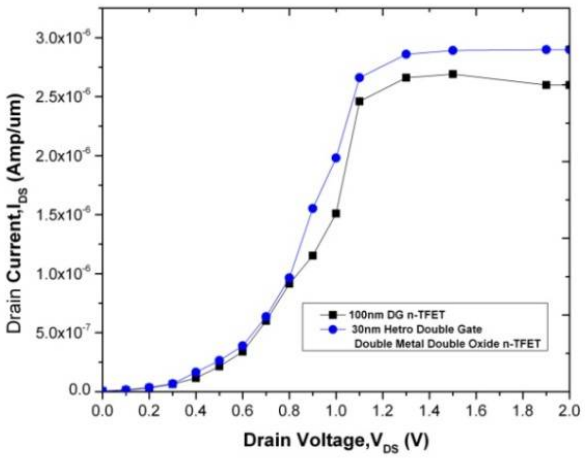

Fig.2. (b).I_{DS}-V_{DS} Characteristics of Existing DG n-TFET and Hetro Double Gate Double Metal Double Oxide n-TFET.

Fig.2. (b) shows the I_{DS}-V_{DS} Characteristics of Existing and Hetro Double Gate Double Metal Double Oxide n-TFET. The Existing device to given V_{GS}=2.0V achieve the drain current is $2.5x10^{-7}$, the proposed device coincides V_{GS} given achieving the drain current is $3.2x10^{-6}$. So, the proposed device is having the better performance compared to Structure Double Gate-n-TFET (DG n-TFET).The electron concentration in the TFET is high, so high leakage current is produced reduced this effect using Hetro Double Gate Double Metal Double Oxide n-TFETfor provide effective gate controlcompared DG-nTFET.

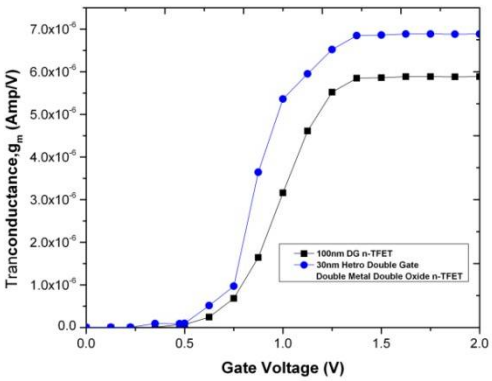

Fig.3. Vg Vsgm comparison of DG n-TFET and Hetro Double Gate Double Metal Double Oxide n-TFET.

Fig.3 shows the V_gVsg_m Characteristics of DG n-TFET and Hetro Double Gate Double Metal Double Oxide n-TFET. The DG n-TFET device to given V_{GS}=2.0V achieve the Transconductance (g_m) is $5.5x10^{-6}$ but proposed device same V_{GS} given achieving the drain current is $5.8x10^{-6}$. So, the proposed device is having the better performance compared to Existing Structure Double Gate-n-TFET (DG n-TFET).

B.DEVICE PERFORMANCE FOR ANALOG APPLICATIONS:

To get higher value of transconductance to drain current ratio g_m/I_D is obtained reduced gate overdrive voltage V_{GT}. DG n-TFET is capable of producing higher gain than a DG n-MOSFET the same power level. An intrinsic gain is $g_m.R_O$. The DG n-TFET gain is 10^1 andHetro Double Gate Double Metal Double Oxide n-TFET is having 10^2.Gate to source C_{gs} and gate-to-drain C_{gd} capacitance at V_{DS}=1V. Unity gain cut-off frequency is expressed as the$g_m/2\pi$ (C_{gs} + C_{gd}).Low

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value of I_D is have TFET so improve the I_D using InAsin the source is expected further improve the analog performance parameters of a TFET.

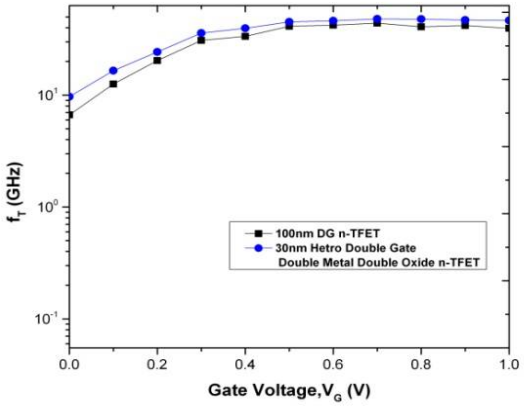

Fig.4.1. V_{GS} Vsf_T Curve of DG n-TFET and Hetro Double Gate Double Metal Double Oxide n-TFET.

Fig.4.1Shows the V_{GS} Compared f_TCharacteristics Curve of DG n-TFET and Hetro Double Gate Double Metal Double Oxide n-TFET. The Existing device to given V_{GS}=1.0V achieve the f_T is 8GHz butHetro Double Gate Double Metal Double Oxide n-TFET device same V_{GS} is given achieving the f_T is10GHz. So, the proposed device is having the better performance compared to Existing Structure Double Gate-n-TFET (DG n-TFET).The parallel combination of output resistance of p- and n-channel devices. Much larger values of output resistance in TFETs due to good output current saturation produce such larger values of voltage gain for the CTFET amplifier shown fig.4.2.

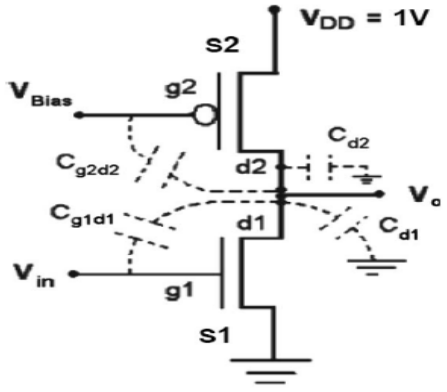

Fig.4.2.Complementry TFET Amplifier Structure

Different parasitic capacitances at the output node of the complementary amplifier configuration as shown in Fig.4.2 are extracted from ac simulation at Vo = V_{DD}/2 = 0.5 V to find C_{Total}= C_{g1d1} + C_{g2d2} + C_{d1} + C_{d2} where C_{g1d1} is the capacitance between the input gate of the n-channel driver and the output node C_{g2d2} is the capacitance between the gate of the p-channel load and the output node Cd1 and C_{d2} are the capacitances between the output node and the ground for the n-channel driver and p-channel load respectively. The gain bandwidth product (GBW) of the amplifier is expressed as GBW = g_m/C_{Total}. The *C*Total and GBW for both CTFET and CMOS amplifiers are plotted as a function of V_{Bias} in Fig.4.2.

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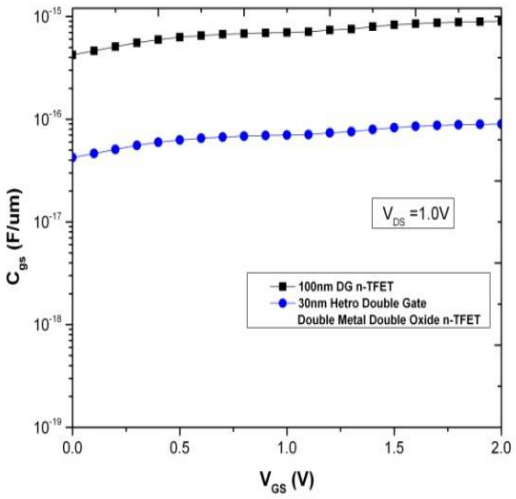

Fig.4.3. (a). V_{GS}VsC_{gs}Curve of DG n-TFET and Hetro Double Gate Double Metal Double Oxide n-TFET.

Fig.4.3.(a) shows the V_{GS}VsC_{gs}Curve of Existing DG n-TFET and Proposed Hetro Double Gate Metal and Double oxide Double Gate n-TFET.
The DG n-TFET device to given V_{GS}=2.0V achieve the C_{gs} is $1.14x10^{-15}$,the proposed device same V_{GS} given achieving the $C_{gs}$is $1.25x10^{-16}$. So, the proposed device is having the reduced parasitic capacitance value so reduced leakage current and to improve the on current. All the capacitance is extracted from the small signal AC simulations at a frequency of 1MHZ.Cgd decreased means increasing V_{DS}. For saturation Cgs is constant as expected as the additional cannot affect the tunneling junction. g_m is high only the tunneling probability is increased.

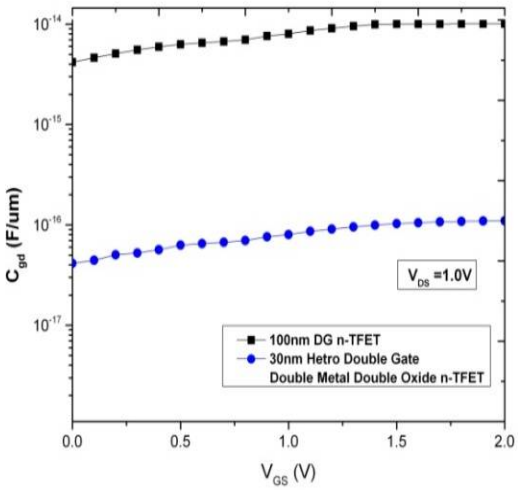

Fig.4.3. (b).V_{GS}VsC_{gs}Curve of Existing DG n-TFET and HetroDouble Gate Double Metal Double Oxide n-TFET.

Fig.4.3.(b) shows the V_{GS}VsC_{gs}Curve of Existing DG n-TFET and Hetro Double Gate Double Metal Double Oxide n-TFET. The Existing device to given V_{GS}=2.0V achieve the $C_{gd}$is $1.23x10^{-15}$and proposed device Similar V_{GS} given achieving the $C_{gs\ is}$ $1.28x10^{-16}$. So, the proposed device is having the reduced parasitic capacitance value so reduced leakage current and to improve the on current. It may also be seen in Fig.4.2 that the gain increases for increasingV_{Bias}

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for both types of amplifiers. For larger values of V_{Bias} the current in the p-channel device that biases the n-channel driver decreases.

IV.CONCLUSION

In this paper,we analyzed the performance of Hetro Double Gate Double Metal Double Oxide n-TFET which provides higher device gain, high on-current, low off-current compared to DG n-TFET. By reducing the parasitic capacitance we can improve the on-current value and device performance.When using InAs as source material, we can improve the on-current value (I_{on}), and thereby reducing the off-current value (I_{off}). Hence Hetro Double Gate Double Metal Double Oxide n-TFET can be used for ultra low power applications like sensors and digital circuits.

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