



## International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 11, November 2013

# Effects of gate insulator thickness and diameter over on/off current ratio in ballistic CNTFETs

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**ABSTRACT:** This paper deals with the changes of the gate insulator thickness and diameter of the nano tube on the carbon nano tube field effect transistor (CNTFET). With a large CNT diameter and thinner gate oxide enhanced on-state current can be profound. On the other hand, the off-state current improves in CNTFETs with thinner gate oxide. Also the simulation results show that the variance of insulator thickness on the threshold voltage, has no effect on the off-state current. In this way an optimum values of gate insulator thickness and diameter of the nano tube are identified to offer highest on/off current ratio of the device.

**Keywords:** CNTFET, CNT diameter, oxide thickness, on-off current ratio.

### I.INTRODUCTION

One of the most imaging features of carbon nanotube is its application on electronics field especially in Carbon nanotube field effect transistor (CNTFET). The motivation of research in CNFET is fuelled by the unique electrical characteristics of carbon nanotube especially the semiconducting characteristic. Just like MOSFET it supplies electrons from source terminal to drain terminal from collection. In other words, current is actually flowing from drain to source terminal [1],[2].Single-walled carbon nanotube(SWCNT) was discovered by Iijima [3],[4] and his group through experiment work. This finding of SWNT is more important since the structure is more fundamental and became the basis for theoretical studies of large bodies. For modelling a CNTFET, mesoscopic physics analysis gives different accepts of CNTFET and their structures. CNTFETs are mainly divided into Schottky barrier CNTFETs (SB CNTFETs) with metallic electrodes which form Schottky contacts and MOSFET-like CNTFETs with doped CNT electrodes which form Ohmic contacts. This paper details with SB CNTFET structures. Normally, a potential barrier known as Schottky barrier (SB) exists at every contact between metal and semiconductor. The barrier height is determined by the filling of metal-induced gap states. These states become available in the energy gap of semiconductor due to interface formed with the metal. The SB is controlled by the difference of the local work functions of the metal and the carbon nanotube. SB is also extremely sensitive to changes of local environment at the contact [5]. For example, gas adsorption changes the work function of metal surfaces. Since this device employs metal as its source/drain terminals and has Schottky barrier at its terminal contact between nanotube and metal, therefore it is called Schottky-barrier CNFET (SB-CNFET). In the field of CMOS technology, power constrained environment can be acquainted by low switching energy per logic transition. To obtain this phenomenon supply voltage has to be minimal along with an acceptable on/off current ratio. Due to small intrinsic behaviour and size CNT has a considerable advantages. Here, this paper investigates with the on/off current ( $I_{on}/I_{off}$ ) ratio based on gate insulator parameters with respect to the changes in co-axial diameter of CNT. Also this paper justifies the reason behind this phenomenon with the obtained results in details.

### II.RELATED WORKS

Unique electrical properties like large mean free path, excellent carrier mobility and improved electrostatics at nanoscales makes CNTs deserving solution for the limitation of scaling devices in the silicon (Si) channel transistors.[6]There are few numerical studies on CNTFETs' performance based on changes in gate insulator parameters [7],[8] especially at different ambient temperatures for CNTFET devices. They are mainly done on SB FET structures. Recently there are works on the doping effects on the channel at different diameters. The on/off ratio has an



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inverse relation with the doping level [10]. It also depends upon the diameter value of nano tube. In case of oxide thickness, So intensive researches are implanted on the effect of diameter and oxide thickness of CNTFETs.

### III. MATHEMATICAL ANALYSIS FOR BALLISTIC CNTFET

This paper involves simulation study to investigate the I-V characteristic of CNFET. The simulation study is carried out using MATLAB based on surface potential model described by Rahman *et. al.* [9]. This is a simple, analytical model that can be used to investigate the I-V characteristic of CNFET. According to the ballistic CNT ballistic transport theory, the drain current caused by the transport of the non-equilibrium charge across the nanotube can be calculated using the Fermi-Dirac statistics as follows:

$$I_D = \frac{2qKT}{\pi h} \left[ f_0\left(\frac{U_{SF}}{KT}\right) - f_0\left(\frac{U_{DF}}{KT}\right) \right] \quad (1)$$

where  $f_0$  represents the Fermi-Dirac integral of order 0,  $k$  is Boltzmann's constant,  $T$  is the temperature,  $h$  is reduced Planck's constant,  $U_{scf} = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) + U_C \Delta N$  and  $U_C = \frac{q^2}{C_\Sigma}$  is the charging energy. Now

$$\Delta N = N_s + N_D - N_0 \quad (2)$$

Here,  $N_s$  is the density of positive velocity states filled by the source,  $N_D$  is the density of negative velocity states filled by the drain and  $N_0$  is the equilibrium electron density. And  $C_\Sigma$  is the parallel combination of the three capacitance for the ballistic nano transistors.

### IV. RESULTS AND DISCUSSION

#### A. Effect of oxide thickness:

In this paper, the effect of oxide insulator thickness ( $t_{INS}$ ) on the CNFET performance is simulated. For simulation, the CNT diameter ( $d_{CNT}$ ) is set to 1 nm with the temperature, T is at 300 K, high-k gate dielectric is fixed at  $k=3.9$ . Now, the  $t_{INS}$  is varied from 2-6 nm. Figure 1 shows the plot of drain-source current,  $I_{DS}$  vs gate-source voltage,  $V_{GS}$  and their dependence with  $t_{INS}$  in linear scale.

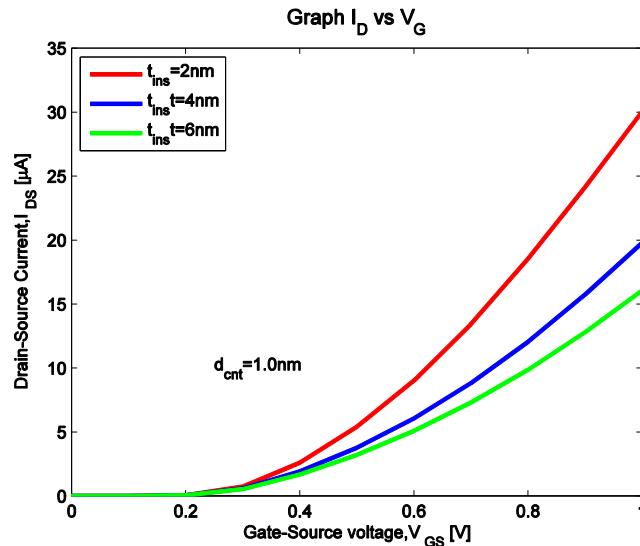


Fig. 1 Effect of insulator thickness on  $I_{DS}$  vs.  $V_{GS}$  in linear scale. To obtain the  $I_{on}$  current the curve is shown in linear scale.

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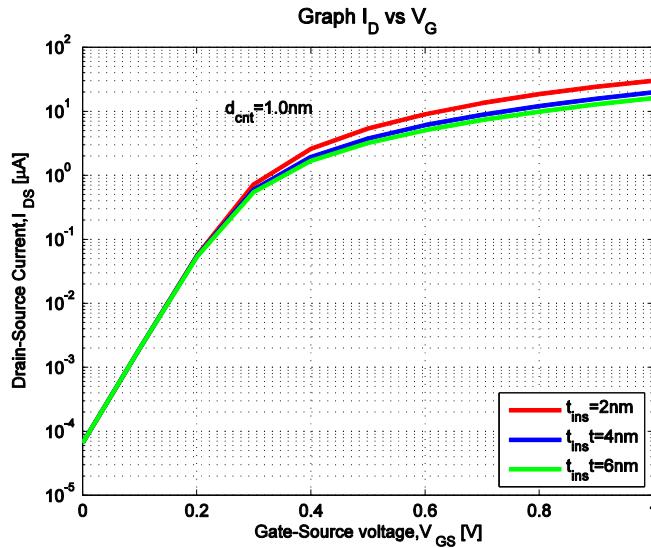


Fig. 2 Effect of insulator thickness on  $I_{DS}$  vs.  $V_{GS}$  in logarithmic scale. To obtain the  $I_{off}$ , the curve is shown in logarithmic scale.

The figure 1 shows the inverse proportionality of conductivity towards the  $t_{INS}$ . Again, if the insulator thickness is small then the effect of  $V_{GS}$  in the CNT would be much greater. Since the modulating of barrier height is controlled by the  $V_{GS}$ , so the conductivity will increase when  $t_{INS}$  decreases. For smaller value of oxide thickness, the height of potential barrier becomes high and tunnelling concept becomes prominent which leads to higher thermionic emission (TE) current and hence on current is increased [10]. On the other hand, figure 2 shows the impact of off current. In this case, the variance of insulator thickness on the threshold voltage,  $V_{TH}$  and off-state current,  $I_{DS}$  (OFF) is unchanged and that leads to the suppression of the ambipolar characteristics. As a result,  $I_{on}/I_{off}$  ratio degrades in higher values of oxide thickness.

## B. Effect of diameter:

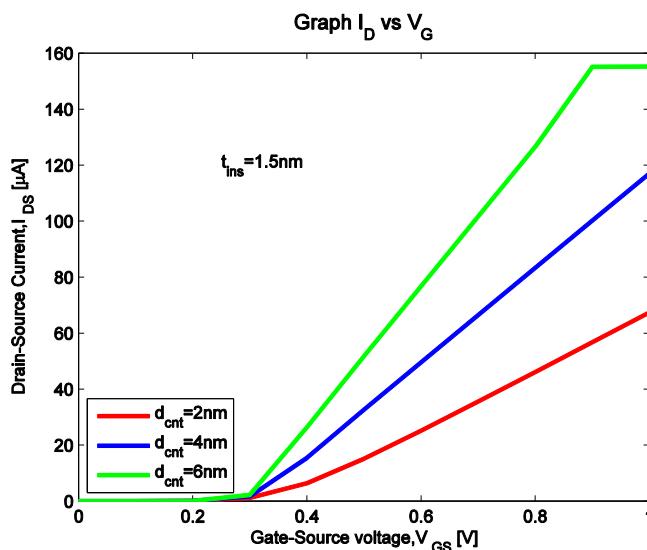


Fig. 3 Effect of insulator thickness on  $I_{DS}$  vs.  $V_{GS}$  in linear scale. To obtain the  $I_{on}$  current the curve is shown in logarithmic scale.

Here, the  $t_{INS}$  is set to 1.5nm, while T is at 300K and the diameter  $d_{CNT}$  varies from 2-6 nm. Figure 3 shows the  $I_D$  and  $V_{GS}$  dependence with  $d_{CNT}$  in linear scale. The result shows that the conductivity is proportional to the CNT diameter. The same  $V_{TH}$  and  $I_{DS}$  for different  $d_{CNT}$  is also observed. Due to the proportional characteristics, the  $I_{DS}$  conductivity

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increase enormously with slightly increase in the  $d_{CNT}$ . Hence, larger  $d_{CNT}$  will give larger current. The valence band edge of channel is closer to the conduction band edge of the source at the same gate field for lower value of diameter of CNT. For leakage current increases [10]. As a result on current is increased.

In figure 4, the effect of diameter on the off current is shown. As the off current is very small, the curve is shown in logarithmic scale. In general, with an increase on the diameter of nano tube, the on current state increased accordingly. On the other hand, the off state remainsunchanged.

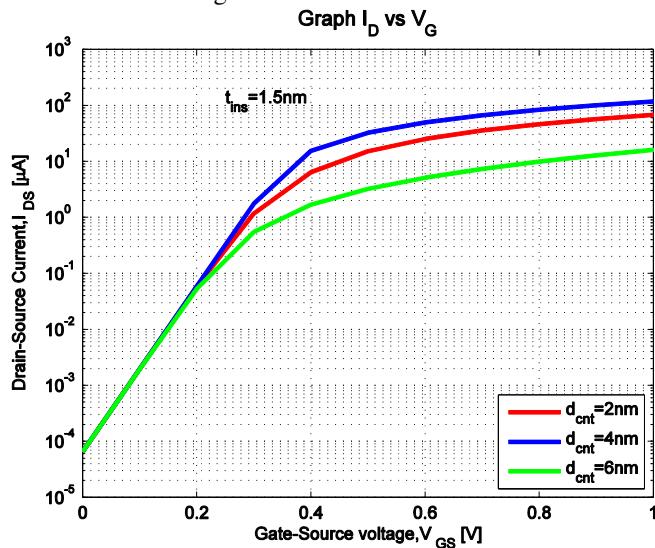


Fig4: Effect of diameter of CNT on  $I_{DS}$  vs.  $V_{GS}$  in logarithmic scale. To obtain the  $I_{off}$ , the curve is shown in logarithmic scale.

### C. Effect of $I_{on}/I_{off}$ current ratio on CNT diameter and oxide thickness:

In this section, for figure 5, the gate oxide thickness is fixed at 1.5nm while the nanotube diameter  $d_{CNT}$  is varied from 2-6 nm. Figure 5 presents the  $I_{on}/I_{off}$  current ratio as a function of the nanotube diameter.  $I_{ON}$  is obtained at  $V_{GS} = 1$  V.  $I_{OFF}$  is defined as the current obtained for  $V_{GS} = 0$  V. In both cases, the drain voltage is kept constant at 1 V. It can be observed that  $I_{on}/I_{off}$  currentratio is improved with increase in the nanotube diameter. Using a larger diameter reduces the band gap, therefore both the onand the leakage current increases rapidly. Thus a significant increase of the  $I_{on}/I_{off}$  ratiois observed with a larger nanotube diameter. So this point must be carefully taken into account to obtain the best electrical characteristics in perspective to build reliable logic circuits based on CNTFETs.

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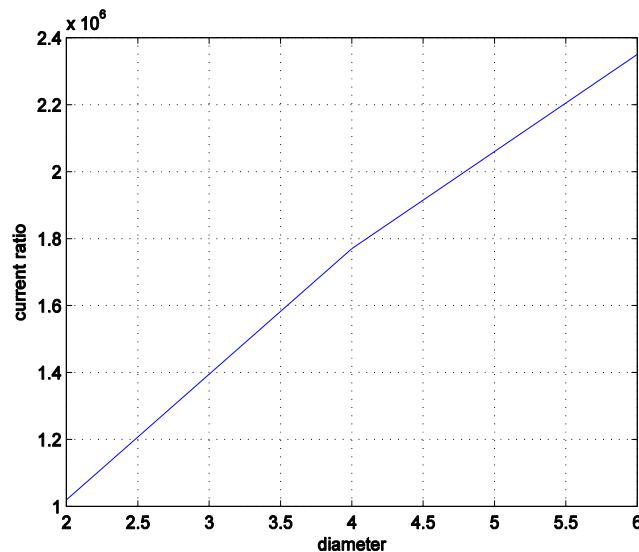


Fig 5:  $I_{on}/I_{off}$  current ratio vs. diameter of CNT with same conditions as in fig 1

Now for oxide thickness variation, in figure 6,  $I_{ON}$  is measured at  $V_{DS} = 1V$  and  $V_{GS}=1V$ .  $I_{OFF}$  defined as the current obtained for  $V_{DS} = 1V$  and  $V_{GS}=0V$ . It can be seen from the figure 6 that with decrement of  $t_{INS}$ , makes the  $I_{on}/I_{off}$  ratio increases and lead to a high on- state current. This is associated with superior control of the gate voltage over the channel, which helps in reducing the off- state current. As the on state current largely depends upon the higher energy level and flow of TE current, it becomes insensitive for device parameter compare to  $I_{off}$ [10].

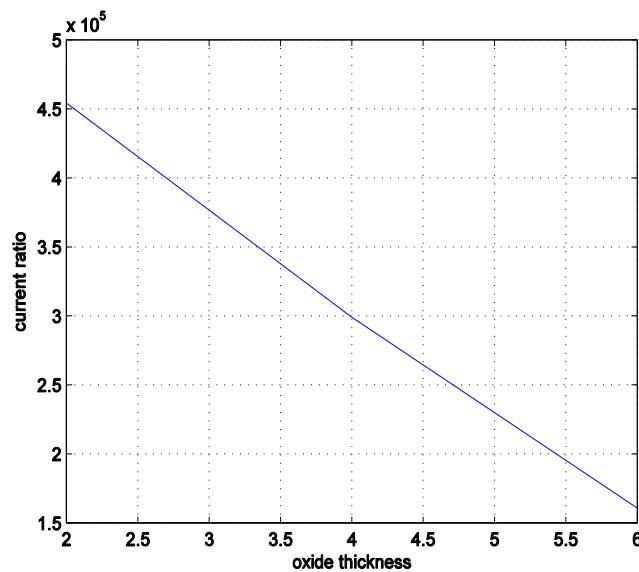


Fig 6:  $I_{on}/I_{off}$  current ratio vs. oxide thickness with same conditions as in fig 1

## V. CONCLUSION

Finally it is observed that using large CNT diameter and thinner gate oxide are caused by the enhancement in on-state current, and off-state current improves in CNTFETs with thinner gate oxide, but they become worse in CNTFETs with large nanotube diameter. It was observed that the impact of diameter and oxide thickness on the drain current is noticeable. At the end of these analysis, it shows that both parameters actually affects the drain current and hence the performance of ballistic CNTFET. As a conclusion, CNTFET has large potential that can be exploited to be an



ISSN (Print) : 2320 – 3765  
ISSN (Online): 2278 – 8875

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effective switching device. CNFET is still far to be a commercial device in electronic industry but the researchers are pushing very hard to improve its performance in order to replace MOSFET as the heart of digital applications.

## VI. ACKNOWLEDGEMENT

The author would like to acknowledge with gratitude to the Dept. of EEE, AUST for providing unfailing support to the work.

## REFERENCES

- [1] R.H. Baughman, A.A. Zhakidov, W.A. deHeer, Science 297, 787 (2002)
- [2] P.G. Collins, P. Avouris, Sci. Am. 283, 62 (2000)
- [3] S. Iijima and T. Ichihashi. Nature, 363:603-605, 1993.
- [4] D. S. Bethune, C. H. Kiang, M. S. Devries, G. Gorman, R. Savoy, and J. Vazquez. Nature, 363:605-607, 1993.
- [5] S.J. Tans, A.R.M. Verschueren, C. Dekker, Nature 393, 49 (1998)
- [6] Thompson, Scott E., and Srivatsan Parthasarathy. "Moore's law: the future of Si microelectronics." Materials Today 9.6 (2006): 20-25.
- [7] R. Martel, T. Schmidt, H.R. Shea, T. Hertel, P. Avouris, Appl.Phys. Lett. 73, 2447 (1998)
- [8] K. Alam, R.K. Lake, J. Appl. Phys. 100, 24317 (2006)
- [9] Rahman, A. et. al. "Theory of Ballistic Nano transistors". IEEE Transactions on Electron Devices, 50(9): 1853-1864 2003
- [10] Shirazi, Shaahin G., and Sattar Mirzakuchki. "Dependence of carbon nanotube field effect transistors performance on doping level of channel at different diameters: On/off current ratio." Applied Physics Letters 99.26 (2011): 263104-263104.

## BIOGRAPHY



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