



# **MATLAB SIMULATION OF A DC-AC-DC CONVERTER WITH ZERO-VOLTAGE- SWITCHING**

**B.Surendra<sup>1</sup>, R.Mahendhar<sup>2</sup>, Dr.Himani<sup>3</sup>**

PG Student [Power Electronics], Aurora's Engg College, Bhongir, AP, India<sup>1</sup>

Asst. Professor, Dept.of EEE, Aurora's Engg College, Bhongir, AP, India<sup>2</sup>

HOD, Dept. of EEE, Aurora's Engg College, Bhongir, AP, India<sup>3</sup>

**ABSTRACT:** A full-bridge dc–dc converter is proposed featuring zero-voltage-switching (ZVS) of active switches over the entire conversion range. In contrast to conventional techniques the stored energy in the auxiliary inductor of the proposed converter is minimal under full load condition and it progressively increases as the load current decreases. Therefore, the ZVS operation over the entire conversion range is achieved without significantly increasing full load conduction loss making the converter particularly suitable in applications where the output is required to be adjustable over a wide range and RL load, and variable load for practical is to be calculated.

**Keywords:** DC–DC power conversion, soft-switching, zero-voltage-switching (ZVS).

## **I.INTRODUCTION**

The zero-voltage-switching (ZVS), Zero voltage switching can best be defined as conventional square wave power conversion during the switch's on-time with switching transitions. For the most part, it can be considered as square wave power utilizing a constant off-time control which varies the conversion frequency, or on-time to maintain regulation of the output voltage. For a given unit of time, this method is similar to fixed frequency conversion which uses an adjustable duty cycle, regulation of the output voltage is accomplished by adjusting the effective duty cycle, performed by varying the conversion frequency. This changes the effective on-time in a ZVS design. The foundation of this conversion is simply the volt-second product equating of the input and output. It is virtually identical to that of square wave power conversion, and vastly unlike the energy transfer system of its electrical dual, the zero current switched converters. During the ZVS switch off-time, the L-C tank circuit resonates. This traverses the voltage across the switch from zero to its peak, and back down again to zero. At this point the switch can be reactivated, and lossless zero voltage switching facilitated. Since the output capacitance of the MOSFET switch ( $C_{o\&}$ ) has been discharged by the resonant tank, it does not contribute to power loss or dissipation in the switch. Therefore, the MOSFET transition losses go to zero - regardless of operating frequency and input voltage. This could represent a significant savings in power, and result in a substantial improvement in efficiency. Obviously, this attribute makes zero voltage switching a suitable candidate for high frequency, high voltage converter designs. Additionally, the gate drive requirements are somewhat reduced in a ZVS design due to the lack of the gate to drain (Miller) charge, which is deleted when  $V_{\&}$  equals zero. The technique of zero voltage switching is applicable to all switching topologies; the buck regulator and its derivatives (forward, half and full bridge), the fly back, and boost converters, to name a few. This presentation will focus on the continuous output current, buck derived topologies, converter (FBZVS converter), [1]–[5], is the most popular topology for dc–dc converters due to fixed switching frequency, ZVS operation, high efficiency, low circulating reactive energy and moderate device stresses. By using a dc blocking capacitor and a saturable inductor in series with primary winding, the primary current during the free-wheeling interval can be reduced to zero. This circuit is called as the zero-voltage and zero-current-switching (ZVZCS) FB converter [6] wherein the lagging-leg switches operate at ZCS and leading-leg switches operate with ZVS. The major limitation of the FBZVS converter has been the limited range of operation over which ZVS can be achieved. When the load current is low, the ZVS of the lagging-leg switches is lost as the energy stored in the leakage inductance of the transformer is insufficient to discharge the switch



# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

**Vol. 2, Issue 8, August 2013**

and transformer capacitances. The loss of ZVS results in increased switching losses and electromagnetic interference (EMI). In the case of high-power converters using insulated gate bipolar transistor (IGBT), an external snubber capacitor is connected to reduce the rate of rise of voltage and turn-off losses. Therefore, in high-power converters, the loss of ZVS additionally results in the discharge of snubber capacitor in IGBT. The resulting surge current can be detrimental to IGBT and capacitor in the long run and it increases EMI problem. Further, the resonant voltage overshoots due to resonance between the snubber capacitor and wiring/lead inductance can exceed IGBT voltage rating. Therefore, it is important to maintain ZVS operation over the entire range of operation or the conversion range. The following solutions have been proposed in the past. Using higher series inductance increases the ZVS range but results in increased loss of duty cycle and ringing across secondary-side rectifier diodes. With consequent reduction in transformer turns ratio, primary reflected current and switch conduction loss increases [2], [5].

- 1) Using saturable inductor instead of a linear inductor, ZVS range can be increased without significantly losing the duty ratio [7], [8]. However, a large-size core is required to implement the saturable inductor.
- 2) The energy stored in the magnetizing inductance can also be used to aid the ZVS operation. The switch current and the conduction loss is significantly increased [9]. In the converter proposed in [10] and [11], the stored energy in the magnetizing inductance of auxiliary transformer (which is independent of load) is used to extend the ZVS range.
- 3) Using a passive auxiliary “pole” circuit, full-range ZVS operation can be achieved [12] but the fixed circulating

Current results in additional conduction loss. In the above listed techniques, except for (2), the range of ZVS operation can be extended at the expense of increased full-load conduction loss. Ideally, additional energy storage is not required under full-load condition since the energy stored in transformer leakage inductance is sufficient for ZVS operation. The additional stored energy is required only when the load current is less. FBZVS converters featuring this kind of adaptive energy storage using coupled inductors are reported in [13] and [14]. A passive auxiliary add-on circuit for conventional FBZVS converter using a transformer and an uncoupled inductor to achieve ZVS operation over the entire conversion range is recently proposed [15]. In this paper a new topology of FBZVS converter is proposed to achieve ZVS over entire conversion range with minimum additional conduction loss. The proposed converter does not use auxiliary coupled inductor or transformer, rather, the main power transformer is divided into two half-rated transformers and an uncoupled inductor is used to achieve ZVS over entire conversion range. It is particularly suitable in applications where the output is required to be adjustable over a wide range and load resistance and Inductance is fixed (e.g. an electromagnet power supply). The proposed converter and its operating principle are described in Sections II and III, respectively. The design considerations are discussed in Section IV. Experimental results on a 100 kHz, 500 W prototype converters are presented in Section V demonstrating full-range ZVS operation. The proposed converter is expected to exhibit higher efficiency even at part-load operation either in its low-power (e.g., up to 1–2 kW) high-frequency (300–500 kHz) application using MOSFETs or in its high-power (e.g., 5–20 kW) low-frequency (25–50 kHz) application using IGBTs. Simplified loss analysis for a high-power application of proposed FBZVS converter with IGBTs and calculations with design parameters of a 18 kW electromagnet power supply presented in Section VI, illustrate its higher part-load efficiency.

## *A.ZVS Benefits*

Zero power “Lossless” switching transitions, Reduced EMI / RFI at transitions, No power loss due to discharging Goss, No higher peak currents, (i.e. ZCS) same as, square wave systems, High efficiency with high voltage inputs at, and any frequency Can incorporate parasitic circuit and component L & C Reduced gate drive requirements (no “Miller” effects) Short circuit tolerant

## *B.ZVS Differences*

Variable frequency operation (in general), Higher off state voltages in single switch, unclamped topologies Relatively new technology - users must climb the earning curve Conversion frequency is inversely proportional to load current A more sophisticated control circuit may be required

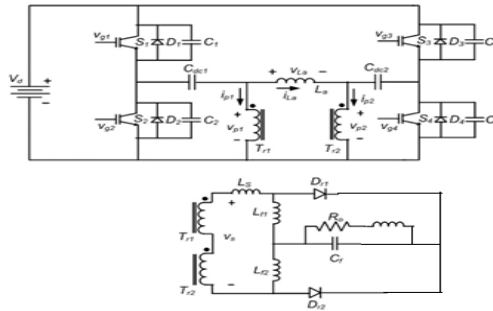
# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 8, August 2013

## II. PROPOSED FBZVS CONVERTER

In Fig. 1 shows the circuit diagram of the proposed FBZVS converter. Four MOSFET or IGBT switches,  $S_1$ – $S_4$ , four anti-parallel diodes,  $D_1$ – $D_4$ , and four snubber capacitors,  $C_1$ – $C_4$  constitute the full-bridge switching circuit. The differences between the proposed and conventional FBZVS converter are as follows.



- The dc blocking capacitor of conventional converter is split into two capacitors,  $C_{dc1}$  and  $C_{dc2}$ , in the proposed circuit.
- While the conventional converter uses a single high-frequency transformer, it is divided into two transformers  $T_{r1}$  and  $T_{r2}$  (with primary-to-secondary turns ratio of  $N:1$ ) in the proposed circuit.
- The proposed circuit has additional inductor  $L_a$  which adaptively stores additional energy for ZVS operation when the stored energy in transformer leakage is inadequate

The secondary windings of the transformers are connected in series. The leakage inductances of both the transformers are shown as a lumped inductor  $L_s$  in series with secondary windings. The diodes  $D_{r1}, D_{r2}$ , inductors  $L_{f1}, L_{f2}$  and capacitor  $C_f$  form the output current double rectifier and filter.  $R_o$  is the load resistance and  $L_o$  is the load inductance, where  $V_d$  is the input dc voltage source. The current double rectifier on the secondary side in Fig. 1 can be replaced with the full-wave bridge and centre tap rectifiers if suitable. Primary and secondary connections of the transformers for alternative rectifier configurations are shown in Fig. 2.

## III. PRINCIPLE OF OPERATION

The idealized waveforms of the converter with proposed auxiliary circuit in the steady-state are shown in Fig. 3. The details of switching transitions are not shown explicitly in the figure because the intension is to describe the operating principle of adaptive energy storage in the auxiliary inductor which aids the full-range ZVS operation and the mechanism of ZVS transitions in FB converters is well understood. Let  $D$  be

## International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

**Vol. 2, Issue 8, August 2013**

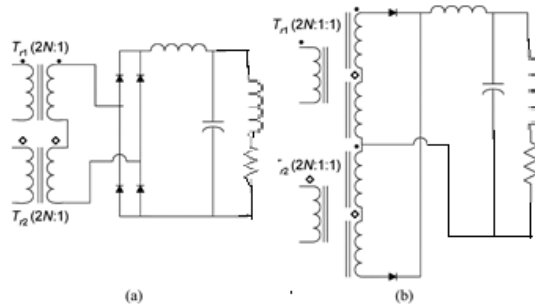


Fig 2

the duty cycle of the output voltage,  $v_s$ , at the terminals of series-connected secondary windings of transformers  $T_{r1}$  and  $T_{r2}$ . The key waveforms for the operation when  $D$  is low are shown by the solid dark lines in Fig. 3. The voltages  $v_{g1} - v_{g4}$  are the gate voltage signals for switches  $S_1 - S_4$ , respectively. In steady-state the voltage across the capacitors  $C_{dc1}$  and  $C_{dc2}$  is equal to  $(V_d/2)$ . The resulting voltage waveforms across the primary windings of the two transformers are shown as  $v_1$  and  $v_2$ . Due to the series connection of the secondary windings as shown in Fig.1,  $v_s = (v_1 + v_2)/N$ . The waveform of  $v_s$  is a three-step bipolar square-wave voltage waveform with amplitude equal to  $\pm(V_d/N)$  and duty cycle  $D$ . The waveform of transformer primary current is shown as  $i_1$  and  $i_2$ . The load current is low and the energy stored in transformer leakage inductance is not sufficient to itself achieve ZVS of all the switches  $S_1 - S_4$ . Under this condition it is desired that the sufficient energy should get stored in  $L_a$  so that ZVS of switches can be achieved. The voltage across  $L_a$  can be written as  $v_{La} = (v_{p1} - v_{p2})$ . The waveform of  $v_{La}$  is a three-step bipolar square-wave voltage waveform with amplitude equal to  $\pm V_d$  and duty cycle  $(1-D)$ . Therefore, when  $D$  is low and load current is less, the duty cycle of  $v_{La}$  is high. The peak value of  $i_{La}(I_{La})$  is high. Sufficient energy is thus available in  $L_a$  to achieve the ZVS operation.  $I_{La}$  is derived as

$$I_{La} = \frac{V_d}{4L_a F_s} (1 - D) = I_{La, \max} (1 - D) \dots (1)$$

Where  $F_s = (1/T_s)$  is the switching frequency the changes in relevant waveforms for the operation of circuit when  $D$  is high are shown by the dashed lines in Fig. 3. The load current is high and energy stored in the transformer leakage inductance itself is sufficient to achieve ZVS of the switches. Under this condition it is desired that the energy storage in  $L_a$  is minimal. It is quite clear from the above discussion and from the waveforms of Fig. 3 that the duty cycle of  $v_{La}$  is low. Therefore,  $I_{La}$  is lower and so is the energy stored in inductor  $L_a$ .

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 8, August 2013

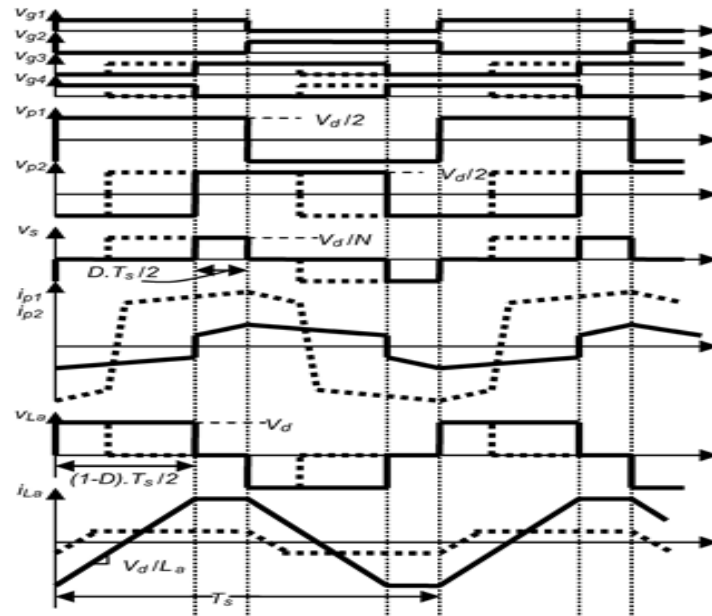


Fig 3

In the applications where output is fixed (e.g. voltage regulator modules),  $D$  is ideally independent of load if output filter inductor current is continuous. This continuous conduction mode (CCM) of operation is, however, practically restricted to typically up to 20% of the maximum load current otherwise the required value and size of filter inductor becomes very large. In discontinuous conduction mode (DCM)  $D$  reduces with load current at No-Load condition.  $D \approx 0$ . In applications where the output is required to be adjustable over a wide range and load resistance and Inductance is fixed (e.g., an electromagnet power supply), the expression for load current (neglecting duty ratio loss) can be written as

$$I_o = \frac{v_d}{2NR_o} D = I_{o, \max} D \dots (2)$$

Thus, the load current and the auxiliary inductor current in the proposed circuit vary opposite to each other. When  $D$  is high, load current is high. Energy stored in transformer leakage inductance is sufficient for ZVS operation. Auxiliary current is low causing low additional conduction losses in the devices. When  $D$  low, load current is low and energy in transformer leakage inductance is insufficient for ZVS operation. Auxiliary current increases and assists to achieve ZVS operation. Thus the trade-off between the ZVS operation and conduction losses is optimally resolved and full-range ZVS is achieved without significantly increasing full-load conduction losses. Although the proposed FBZVS converter has two transformers, the combined rating of the two transformers is the same as one transformer in the conventional FBZVS converter. The primary voltage of the individual transformer in proposed converter ( $\pm V_d/2$ , peak) is half as compared to that in conventional converter ( $\pm V_d$ , peak). Thus the total volt-ampere rating of two transformers in proposed converter is the same as single transformer in conventional converter. In high-power applications two half-rated transformers in proposed converter can ease thermal management. Similarly, the worst case dc voltage ( $\pm V_d$ ) that might appear across two dc blocking capacitors in the proposed converter is the same as that in the conventional FBZVS converter.

## IV. DESIGN CONSIDERATIONS

With the same gate pulse sequence as shown in Fig. 3, in the conventional FBZVS converter, the ZVS operation of right-leg switches,  $S_3$  and  $S_4$ , is lost for load current lower than a certain value since energy stored in only the transformer leakage inductance (plus additional series inductor, if placed) is responsible for ZVS operation. Note that in



## International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 8, August 2013

the proposed FBZVS converter also, in absence of auxiliary inductor  $L_a$  the ZVS operation of right-leg switches,  $S_3$  and  $S_4$ , is lost for lower load currents. It can be noticed from the waveforms of Fig. 3 that switches  $S_1$  and  $S_2$  turn-off when transformer primary current  $i_1$  and the auxiliary inductor current  $i_{La}$  are at maximum. Snubber capacitors  $C_1$  and  $C_2$  are charged and discharged by the total energy stored in inductors  $L_{f1}/L_{f2}$ , leakage inductance of  $T_{r1}$  &  $L_a$ . For higher load current, energy stored in  $L_{f1}/L_{f2}$  is significant, contribution of that in the leakage inductance of  $T_{r1}$  is negligible and since  $I_{La}$  is low; energy stored in  $L_a$  is also insignificant. For lower load currents energy stored in  $L_{f1}/L_{f2}$  still may be sufficient for ZVS operation, and in addition, ZVS of  $S_1$  and  $S_2$  is assisted by energy stored in  $L_a$  as  $I_{La}$  is proportionately increased. However, energy stored in  $L_{f1}/L_{f2}$  is not available for ZVS operation of switches  $S_3$  and  $S_4$  and charging and dis-charging of  $C_3$  and  $C_4$  relies on energy stored in the leakage inductance of  $T_{r2}$  &  $L_a$ . Under the assumption that the trans-formers  $T_{r1}$  and  $T_{r2}$  are identical having the same leakage inductance and neglecting transformer winding capacitances, the energy balance during switching transition for ZVS operation can be written as

$$\frac{1}{2} L_a I_{La}^2 + \frac{1}{2} \frac{L_s}{2} \left( \frac{I_a^2}{4} \right) \geq C V_d^2 \dots (3)$$

Where  $C_3 = C_4 = C$ .

A suitable design of approach can be to minimize the trans-former leakage inductance to minimize the duty cycle loss as well as the overshoot and ringing on the secondary side. This will also maximize the turns ratio of the transformer reducing primary-side conduction loss. The energy stored in  $L_a$  achieves ZVS operation. From (1) and (3)

$$L_a \leq \frac{(1-D)^2}{32CF_s^2} \dots (4)$$

However, if it is minimized, the energy stored in transformer leakage inductance may not be sufficient to achieve ZVS on its own even near full-load condition, i.e. with  $D \approx 1$ . Energy storage in  $L_a$  is therefore also required even near full-load condition to achieve ZVS operation. Equation (3) gives smaller value of  $L_a$  for  $D \approx 1$ . Smaller  $L_a$  in turn result in large  $I_{La}$ , particularly under operating conditions with  $D \approx 0$ , increasing conduction loss in the switches. Therefore, it is felt that instead of minimizing transformer leakage inductance, its value can be optimally chosen to simultaneously achieve full-range ZVS operation and improve overall efficiency over the entire conversion range. However, such an optimization is beyond the scope of this paper.

Additional condition can be imposed for the choice of  $L_a$  based on time  $\Delta t$  allowed to charge/discharge the

$$L_a = \frac{\Delta t(1-D)}{8CF_s} \dots (5)$$

Output voltage of the proposed converter is given by

$$V_o = V_d(D - \Delta D)/2N \dots (6)$$

Where  $\Delta D$  the duty ratio is lost and is given by

$$\Delta D = \frac{2NL_s I_a}{V_d T_s} \dots (7)$$

Solving, (6) and (7)

$$N = \frac{V_d D}{2V_o \left( 1 + \frac{L_s}{R_o T_s} \right)} \dots (8)$$

$$\Delta D = \frac{L_s D}{L_s + R_o T_s} \dots (9)$$

### V. EXPERIMENTAL RESULTS

The full-range ZVS operation in the proposed FBZVS converter is verified on an experimental 500 W prototype converter operating at 100 kHz. The converter operates from a 250 V dc input and delivers 50 A maximum in a load resistance of  $0.2\Omega$ , load inductance 5h. The output current variation is specified in the range of 2 to 50 A. The switches  $S_1-S_4$  are IRF840 MOSFETs. In the trans-formers  $T_{r1}$  &  $T_{r2}$ ,  $N=9$  and  $L_s=0.14\mu H$ . The output filter is:  $L_{f1}=L_{f2}=22\mu H$  and  $C_f=10\mu F$ . The value of auxiliary inductor is  $L_a=240\mu H$  and  $C_{dc1}=C_{dc2}=1\mu F$ . The control circuit was implemented



## International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 8, August 2013

with controller UC3875. The waveforms of input voltage of secondary rectifier  $v_{La}$  and  $i_{La}$  for operation at various values of  $D$  are shown in Fig. 4. Fig. 4(a) shows the waveforms for  $D=0.9$ . As the output current is high, the energy stored in transformer leakage inductance is sufficient for ZVS operation. The duty ratio of  $v_{La}$  is 0.1 and therefore  $I_{La}$  is small causing minimum additional conduction loss. As  $D$  progressively reduces to  $D=0.5$ , as shown in Fig. 4(b), the duty ratio of  $v_{La}$  increases to 0.5, thereby increasing  $I_{La}$ . The reduced energy stored in transformer leakage inductance is supplemented by the energy stored in  $L_a$  to achieve ZVS operation. As  $D$  further reduces to 0.1, as shown by the waveforms of Fig. 4(c), the output current is low and the energy stored in  $L_s$  is not sufficient for ZVS operation. However, the duty ratio of  $v_{La}$  increases to 0.9 increasing  $I_{La}$  and stored energy in  $L_a$  to achieve ZVS operation. The gate-source and drain-source voltage waveforms during turn-on of the left-leg switch  $S_2$  are shown in Fig. 5(a) and (b) for  $D=0.1$  and  $D=0.9$ , respectively. Similarly, the gate-source and drain source voltage waveforms during turn-on of the right-leg switch  $S_4$  are shown in Fig. 6(a) and (b) for  $D=0.1$  and  $D=0.9$ , respectively. Since in all the waveforms, the gate-source voltage is applied after the drain-source voltage drops to zero, the ZVS operation of all the switches over the entire conversion range is demonstrated. Plot (1) of Fig. 7 shows the conversion efficiency of the developed prototype of the proposed converter. Maximum conversion efficiency is limited to 0.8 primarily because the secondary-side drops become comparable with the low output voltage (10 V). The prototype converter was then re-configured as the conventional FBZVS converter by connecting the primary windings of the two transformers in series, and connecting them between the midpoints of both the legs. To demonstrate the advantage of adaptive auxiliary current over the fixed auxiliary current, a “pole” was added to the lagging-leg of the full bridge with 120  $\mu$ H inductor (to keep the peak circulating current same as that in the proposed converter) and capacitive voltage divider using two 1  $\mu$ F capacitors across the input dc bus. The efficiency of conventional FBZVS converter with pole on lagging leg is shown as plot (2) in Fig. 7. From full-load to approximately 20% part-load, efficiency of the proposed converter is observed to be higher. This is because the auxiliary current in the proposed converter is lesser than that in the conventional FBZVS converter with pole on lagging leg. For lower output power, the efficiency of the proposed converter is observed to be lesser. The reason is that in the conventional FBZVS converter with pole on lagging leg, the auxiliary current is circulating in only two switches whereas in the proposed converter auxiliary current is circulating in all the four switches causing more conduction loss. A pole on leading leg is also added to conventional FBZVS converter to achieve ZVS of all the switches over the entire load range. Therefore to compare the efficiencies of proposed converter and conventional FBZVS converter with pole on both legs, another pole with 120  $\mu$ H was added to the configured conventional FBZVS converter on the leading leg along with pole of 120  $\mu$ H on lagging leg. The efficiency of this conventional FBZVS converter with poles on the both legs is shown as the plot (3) in Fig. 7. The efficiency is observed to be further de-graded at full-load and also over the entire range as compared to the efficiency of the proposed converter. The improvement in efficiency with the proposed converter with respect to the conventional FBZVS converter at part-load operation depends on the trade-off between switching losses saved by maintaining ZVS operation and the additional conduction loss in the switches due to circulating current plus losses in the auxiliary inductor. The savings in the switching losses which will be larger if either switching frequency is high (typically 300–500 kHz in low-power applications, e.g., up to 1–2 kW, using MOSFET) or the snubber capacitors are larger (tens of nano farads) in high-power converters (e.g. up to 5–20 kW, using IGBT). Simplified loss analysis and calculations described in Section VI illustrates this. Nevertheless, the full-range ZVS operation achievable in the proposed converter without additional loss penalty at full-load, is the major advantage as safe operation of semiconductor devices, snubber capacitors is guaranteed and overall reliability is increased.

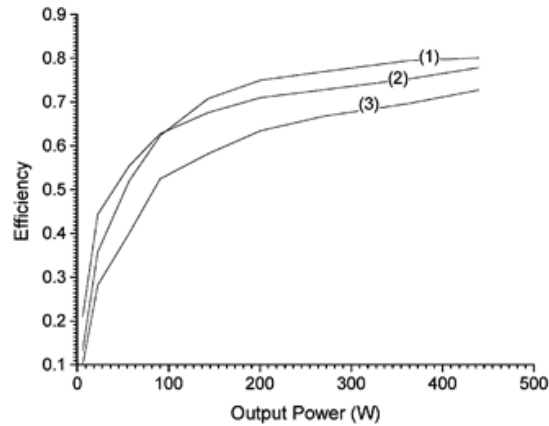


Fig.7 The plots of experimental efficiency. (1) Proposed converter with  $L_a = 240$  H. (2) Conventional FBZVS converter with pole on only lagging-leg. Pole inductance = 120 H. (3) Conventional FBZVS converter with poles on both the legs. Pole inductances = 120 H each.

## VI. SIMPLIFIED LOSS ANALYSIS OF THE PROPOSED FBZVS CONVERTER WITH IGBT SWITCHES

IGBTs are used for the high-power application of proposed FBZVS converter. To calculate the conduction losses in the IGBT switches and anti-parallel diodes as well as the losses in the auxiliary inductor over the entire conversion range, following simplifying assumptions are made.

- 1) The output current is ripple-free; therefore transformer primary current is square-wave.
- 2) Transformer leakage inductance is small; therefore the slew interval (during which the transformer primary current reverses its direction) is absent.
- 3) The average power loss in an IGBT and a diode is proportional to the respective average currents.

### A Device Conduction Loss

The current flowing out of the midpoint of the leading leg is the sum of  $i_{l1}$  and  $i_{La}$  (see Fig. 1). Similarly the current flowing out of the midpoint of lagging leg is the difference between  $i_{l2}$  and  $i_{La}$ . The amplitude of  $i_{l1}$  and  $i_{l2}$  is equal to  $(I_o/2N)$  where  $I_o$  is given by (2). Two distinctive modes can be observed depending on whether  $I_{La} < (I_o/2N)$  or  $I_{La} > (I_o/2N)$ .



# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 8, August 2013

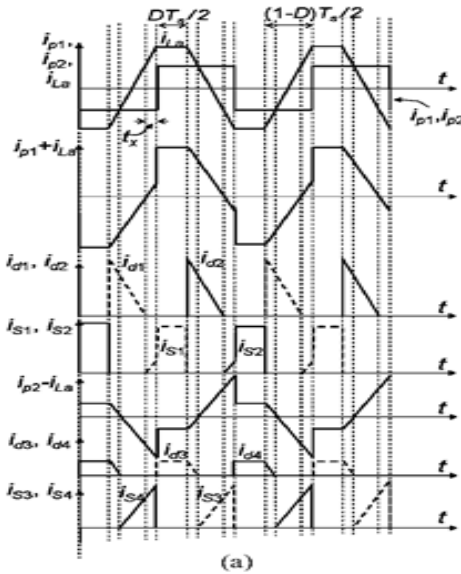


Fig.8

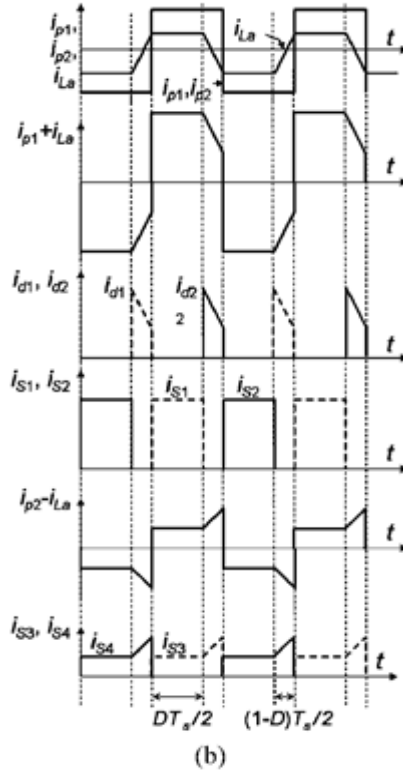


Fig.8

The boundary between the two modes can be derived by equating  $I_{La}$  to  $(I_o/2N)$ , The duty ratio, where the two currents have same amplitude is termed as  $D_{bounda}$  and can be derived as

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

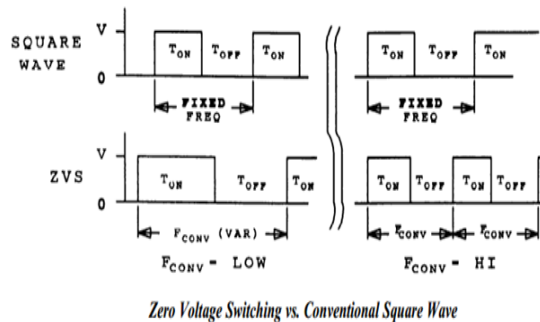
**Vol. 2, Issue 8, August 2013**

$$D_{boundary} = \frac{N^2 R_o}{N^2 R_o + F_s L_a} \quad (10)$$

Fig. 8(a) and (b) shows various current waveforms for  $D < D_{boundary}$  and  $D > D_{boundary}$  respectively. The expressions for average currents in all IGBT switches ( $I_{S1} - I_{S4}$ ) and antiparallel diodes ( $I_{D1} - I_{D4}$ ) of the full-bridge circuit are summarized in Table I. Expressions for the total conduction losses in these devices,  $P_{cond}$ , can then be derived as follows.

For  $D < D_{boundary}$

$$P_{cond} = \frac{V_d}{8L_a F_s} (V_{on} + V_{di}) - D^2 \times \left[ \frac{V_d}{4N^2 R_o} \left( V_{di} - V_{on} - \left( \frac{V_{on} + V_{di}}{2} \right) \frac{L_a F_s}{N^2 R_o} \right) + \frac{V_d}{8L_a F_s} (V_{on} + V_{di}) \right] \quad (11)$$



**TABLE I**  
SUMMARY OF EXPRESSIONS FOR AVERAGE DEVICE CURRENTS

	$D < D_{boundary}$	$D > D_{boundary}$
$I_{D1}, I_{D2}$	$\frac{1}{2} \left( I_{Lo} + \frac{I_o}{2N} \right) \left( \frac{(1-D)}{2} - \frac{t_x}{T_s} \right)$	$\frac{I_o}{4N} (1-D)$
$I_{D3}, I_{D4}$	$\frac{1}{2} \left[ \left( I_{Lo} - \frac{I_o}{2N} \right) D + \frac{t_x}{T_s} \left( I_{Lo} - \frac{I_o}{2N} \right) \right]$	0
$I_{S1}, I_{S2}$	$\frac{1}{2} \left[ \left( I_{Lo} + \frac{I_o}{2N} \right) D + \frac{t_x}{T_s} \left( I_{Lo} - \frac{I_o}{2N} \right) \right]$	$\frac{1}{2} \left( \frac{I_o}{2N} + I_{Lo} \right) D$
$I_{S3}, I_{S4}$	$\frac{1}{2} \left( I_{Lo} + \frac{I_o}{2N} \right) \left( \frac{(1-D)}{2} - \frac{t_x}{T_s} \right)$	$\frac{1}{2} \left( \frac{I_o}{2N} - D I_{Lo} \right)$

For  $D < D_{boundary}$

$$P_{cond} = \frac{V_d}{4N^2 R_o} [D(V_{on} + V_{di}) + D^2(V_{on} - V_{di})] \quad (12)$$

### B. Core and Winding Loss in Auxiliary Inductor

The core loss of ferrites is often expressed in the form of following curve-fit equation.

$$P_{core} = k F_s^\alpha B^\beta \quad (13)$$



## International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 8, August 2013

Where  $k$ ,  $\alpha$  and  $\beta$  are the constants and their values depend on the material grade. In the auxiliary inductor of the proposed converter,  $F_s$  is constant and  $B$  is proportional to  $I_{La}$ , which from (1), is proportional to  $(1-D)$ . Therefore, core loss in the auxiliary inductor can be expressed as

$$P_{core} = P_{core,max}(1 - D)^\alpha \quad (14)$$

where  $P_{core,max}$  is the maximum designed core loss corresponding to  $I_{L,max}$ .

Winding loss in the auxiliary inductor are given by

$$P_{winding} = I_{La,rms}^2 R_{coil} \quad (15)$$

where  $R_{coil}$  is the winding resistance and  $I_{L,rms}$  is the rms value of  $i_{La}$ , given by

$$I_{La,rms} = \frac{V_d(1 - D)}{4\sqrt{3}L_a F_s} \sqrt{(2D + 1)}. \quad (16)$$

### C. Total Primary-Side Losses and Comparison With

#### Conventional FBZVS Converter

The total primary-side losses in the proposed converter are given by

$$P_{total} = P_{cond} + P_{core} + P_{winding}. \quad (17)$$

For conventional FBZVS converter, the expression for the total primary-side loss (equal to the conduction loss in IGBTs and anti-parallel diodes),  $P_{total-conv}$  can be derived as

$$P_{total-conv} = \frac{V_d}{4N^2 R_o} [D(V_{on} + V_{di}) + D^2(V_{on} - V_{di})]. \quad (18)$$

For a 18 kW (60 V/300 A) output electromagnet power supply with designed parameters listed in Table II, Fig. 9 compares the total primary-side losses in the proposed and conventional FBZVS converter over the entire conversion range. These plots are obtained using (10)–(18) and the parameters of Table II. It can easily be seen that the total primary-side losses in the proposed converter are the same as conventional FBZVS converter for operation with higher values of  $D$  (full-load operation). For the lower values of  $D$ , the device conduction plus magnetics losses are higher (e.g. 111 W at  $D=0$ ) in the proposed FBZVS converter due to auxiliary circulating current. However, the loss of ZVS with 15 nF snubber capacitors in the conventional FBZVS converter would have resulted in total  $(1/2CV_2F_s)$  loss of 187.5 W. Therefore, the proposed converter improves the overall efficiency for lower values of  $D$  in addition to the full-range ZVS operation.

### VII. CONCLUSION

A new FBZVS converter is proposed with ZVS of active switches over the entire conversion range. The principle of operation and design considerations of the circuit are described. The experimental results on a 500 W prototype converter demonstrate the adaptive auxiliary current which is high at lower duty ratio assisting the ZVS operation and low at higher duty ratio minimizing the additional conduction loss. The experimental results confirm the full-range ZVS operation. The proposed converter is therefore deemed suitable particularly for high-power applications where full-range ZVS operation is desired without the penalty of additional losses at full-load not only for the saving of switching losses but also for the reliable operation due to elimination of current and voltage stresses on the devices and EMI which results from the non-ZVS operation.

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 8, August 2013

**TABLE II**  
DESIGN PARAMETERS FOR A 18 kW ELECTROMAGNET POWER SUPPLY USED FOR LOSS CALCULATIONS SHOWN IN FIG. 9

Parameter	Value	Parameter	Value
$V_d$	500 V	$L_o$	150 $\mu$ H
$V_o$	0 – 60 V	$P_{core,max}$	35 W
$I_o$	0 – 300 A	$\alpha$	2.5
$F_s$	25 kHz	$R_{coil}$	2.5 m $\Omega$
$N$	3.2	$V_{on}$	2.5 V
$C_1 - C_4$	15 nF	$V_{dr}$	1.5 V

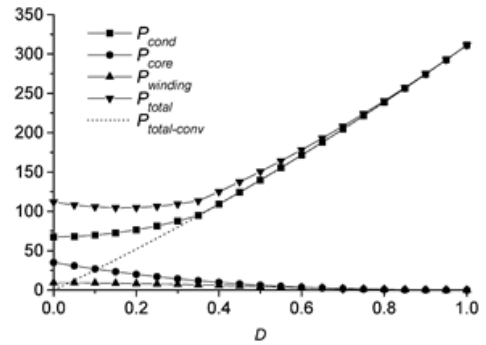
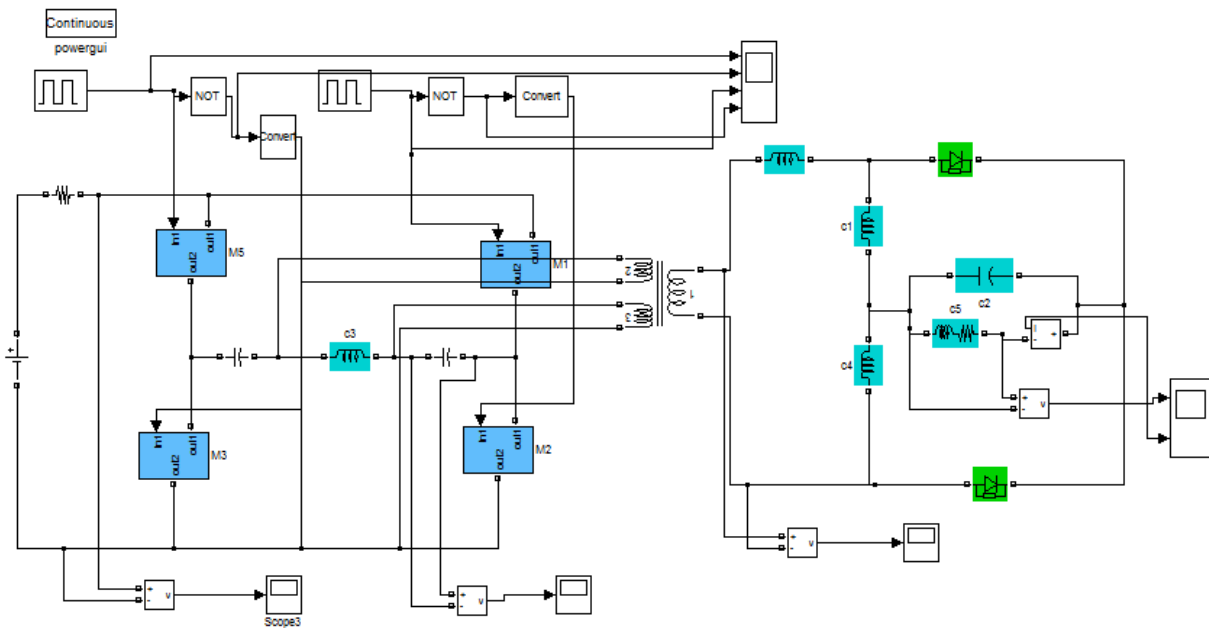


Fig.9

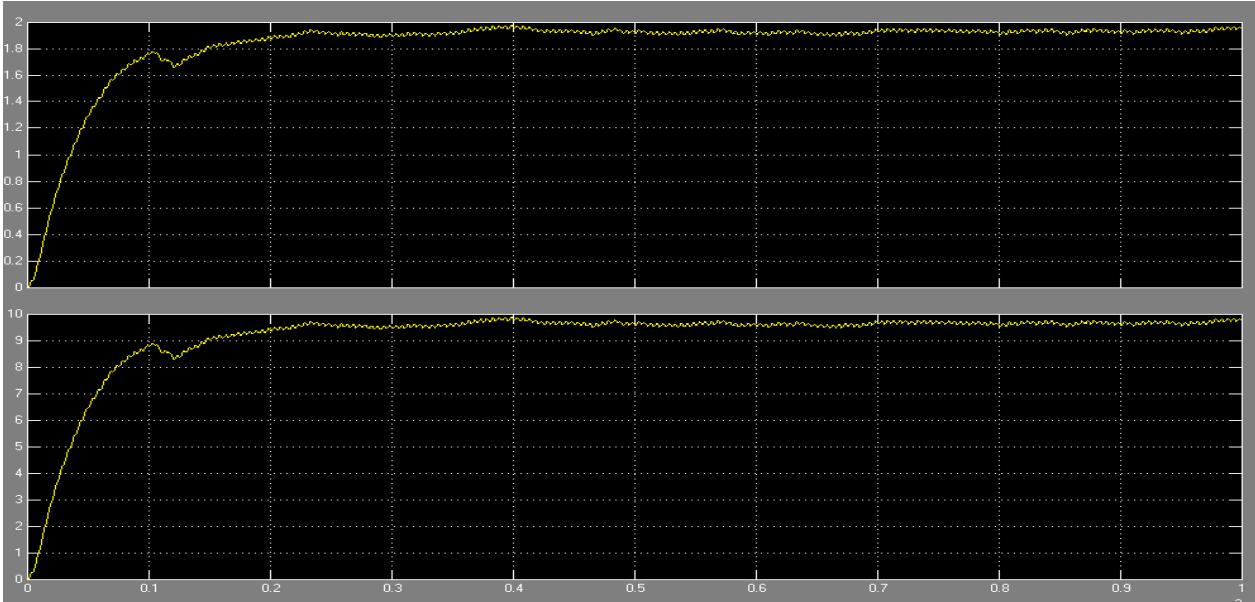


Matlab SIMULATION OF A DC-AC-DC Converter with Zero-Voltage-Switching

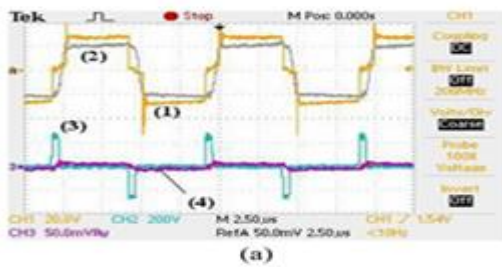
# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

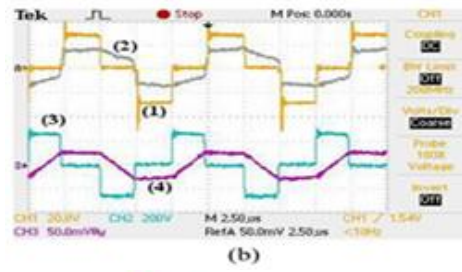
Vol. 2, Issue 8, August 2013



OUTPUT OF SIMULATION



(a)



(b)

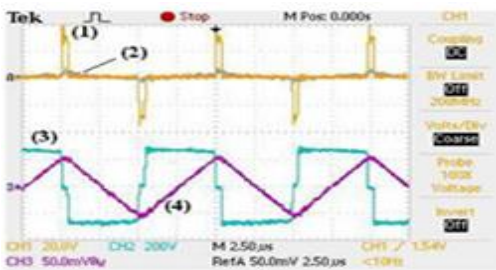
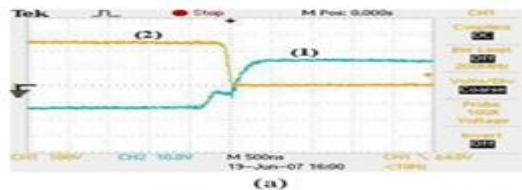


Fig 4



(a)

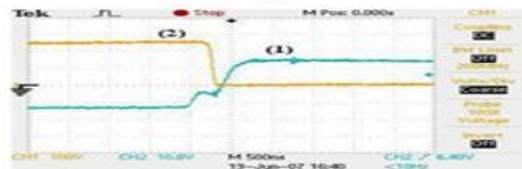


Fig 5

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 2, Issue 8, August 2013

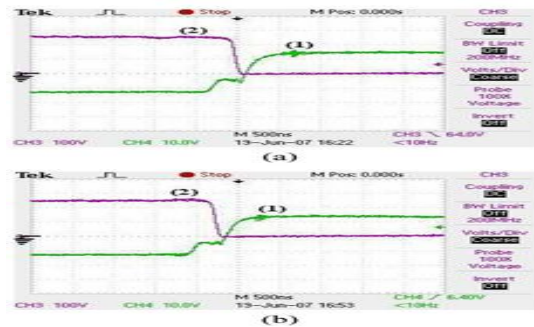


Fig.6

## REFERENCES

- [1] R. A. Fischer, R. D. T. Ngo, and M. H. Kuo, "A 500 kHz, 250Wdc-dc converter with multiple outputs controlled by phase-shifted PWM and magnetic," in Proc. High Freq Power Conv., May 1988, pp. 100–110.
- [2] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho, "Design considerations for high-voltage high-power full-bridge zero voltage switching PWM converter," in Proc. IEEE Appl. Power Electron. Conf. (APEC), 1990, pp. 275–284.
- [3] D. Dalal, "A 500 kHz multi-output converter with zero voltage switching," in Proc. IEEE Appl. Power Electron. Conf. (APEC), 1990, pp. 265–274.
- [4] F.-S. Tsai, "Small-signal and transient analysis of a zero-voltage switched, phase controlled PWM converter using averaged switch model," IEEE Trans. Ind. Appl., vol. 29, no. 3, pp. 493–499, May/Jun. 1993
- [5] A. W. Lotfi, Q. Chen, and F. C. Lee, "Non-linear optimization tool for the full-bridge zero-voltage-switched dc-dc converter," Proc. Inst. Elect. Eng. B, vol. 140, no. 5, pp. 289–296, Sep. 1993.
- [6] J. G. Cho, J. A. Sabate, G. Hua, and F. C. Lee, "Zero-voltage and zero-current-switching full bridge PWM converter for high power applications," IEEE Trans. Power Electron., vol. 11, no. 4, pp. 622–627, Jul. 1996.
- [7] G. Hua, F. C. Lee, and M. M. Jovanovic, "An improved full-bridge zero-voltage-switched PWM converter using a saturable inductor," IEEE Trans. Power Electron., vol. 8, no. 4, pp. 530–534, Oct. 1993.
- [8] S. Hamada and M. Nakaoka, "Analysis and design of a saturable reactor assisted soft-switching full-bridge dc-dc converter," IEEE Trans. Power Electron., vol. 9, no. 3, pp. 309–317, May 1994.
- [9] Watson and F. C. Lee, "Analysis, design and experimental results of a 1-kW FB-ZVS-PWM converter employing magma secondary side control," IEEE Trans. Ind. Electron., vol. 45, no. 5, pp. 806–814, Oct. 1998.
- [10] R. Ayyanar and N. Mohan, "Novel soft-switched dc-dc converter with full ZVS-range and reduced filter requirement—Part I: Regulated-output applications," IEEE Trans. Power. Electron. vol. 16, no.2, pp. 184–192, Mar. 2001.
- [11] R. Ayyanar and N. Mohan, "Novel soft-switched dc-dc converter with full ZVS-range and reduced filter requirement—Part II: Constant input, variable-output applications," IEEE Trans. Power. Electronics. vol. 16, no. 2, pp. 193–200, Mar. 2001.
- [12] P. K. Jain, W. Kang, H. Soin, and Y. Xi, "Analysis and design considerations of a load and line independent zero voltage switching full bridge DC/DC converter topology," IEEE Trans. Power Electron., vol.17, no. 5, pp. 649–657, Sep. 2002.
- [13] Y. Jang, M. M. Jovanovic, and Y. Chang, "A new ZVS-PWM full bridge converter," IEEE Trans. Power Electron., vol. 18, no. 5, pp.1122–1129, Sep. 2003.
- [14] Y. Jang and M. M. Jovanovic, "A new family of full-bridge ZVS converters," IEEE Trans. Power Electron., vol. 19, no. 3, pp. 701–708, May 2004.
- [15] M. Borage, S. Tiwari, and S. Kotaiah, "A passive auxiliary circuit achieves zero-voltage-switching in full-bridge converter over entire conversion range," IEEE Power Electron. Lett., vol. 3, no. 4, pp..
- [16] A. W. Lotfi, Q. Chen, and F. C. Lee, "Non-linear optimization tool for the full-bridge zero-voltage-switched dc-dc converter," Proc. Inst. Elect. Eng. B, vol. 140, no. 5, pp. 289–296, Sep. 1993.

## BIOGRAPHY



B. Surendra<sup>1</sup>, born '85, Diploma in EEE from J.N.G.P College Hyderabad, Graduated in Electrical Engg, from S.R.R Engg College, Khammam, JNT.U'ty, (AP), India. He is currently pursuing MTech. (Power Electronics) at Aurora's Engg College. He is interested fields are Power Electronics.



ISSN (Print) : 2320 – 3765  
ISSN (Online): 2278 – 8875

## International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

*(An ISO 3297: 2007 Certified Organization)*

**Vol. 2, Issue 8, August 2013**



R. Mahendhar<sup>2</sup>, graduated in electrical engg, presently working as asst. professor, EEE dept, aurora's engg college. He is interested fields are Power Electronics.



DR HIMANI<sup>3</sup>, graduated in Electrical Engg. From Mumbai, M Tech (IIT-R), PhD (IIT-D), LLB, MBA (Pune). She is currently working as HOD and Professor at Aurora's Engg College. She is interested fields are Power Electronics.