



Five-Input Complex Gate using Quantum Dot Cellular Automata

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ABSTRACT: This paper presents the basics of quantum dot cellular automata along with the QCA logic devices such as the QCA wire, inverter and the majority gate. The four phases of the clocking have been discussed and also the implementations of the complex gate have been done using the QCADesigner tool. The logical structures such as AND and OR gates using a quantum dot cellular automata 3-input majority gate have been discussed based on which the five-input complex gate have been designed and can be configured into logical structures such as four input AND and OR.

Keywords: QCA, majority gate, logic structures, complex gate, QCADesigner.

I. INTRODUCTION

Current silicon transistor technology faces challenging problems, such as high power consumption and difficulties in feature size reduction. Nanotechnology is an alternative to these problems. The Quantum dot cellular automata (QCA) is one of the attractive alternatives [1]. Since QCAs were introduced in 1993 by Lent et al, and experimentally verified in 1997. QCA is expected to achieve high device density, extremely low power consumption and very high switching speed. QCA structures are constructed as an array of quantum cells with in which every cell has an electrostatic interaction with its neighboring cells [2]. QCA applies a new form of computation, where polarization rather than the traditional current, contains the digital information. In this trend, instead of interconnecting wires, the cells transfer the information throughout the circuit [4].

This paper describes the design of different logical structures in QCA such as AND and OR. These structures are designed based on the basic logical devices. The paper is organized as follows; the background of QCA technology is explained in section 2. Section 3, provides the QCA clocking and section 4 describes the QCA Designer tool. Section 5 shows the design and implementation of logical structures in QCA using majority gate. Simulation results follow in section 6 and conclusions are presented in section 7.

II. BACKGROUND

A. QCA Basics

QCA technology is based on the interaction of bi-stable QCA cells constructed from four quantum dots. The cell is charged with two free electrons, which are able to tunnel between adjacent dots. These electrons tend to occupy antipodal sites as a result of their mutual electrostatic repulsion. Thus, there exist two equivalent energetically minimal arrangements of the two electrons in the QCA cell, as shown in Fig. 1. These two arrangements are denoted as cell polarization $P = +1$ and $P = -1$. By using cell polarization $P = +1$ to represent logic “1” and $P = -1$ to represent logic “0,” binary information is encoded in the charge configuration of the QCA cell [2][5].

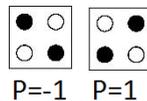


Fig. 1. QCA cell polarization.

B. QCA Logic Devices

The fundamental QCA logic primitives include a QCA wire, QCA inverter, and QCA majority gate [4]-[6], as described below.

QCA Wire: In a QCA wire, the binary signal propagates from input to output because of the electrostatic interactions between cells. The propagation in a 90° QCA wire is shown in Fig. 2. Other than the 90° QCA wire, a 45° QCA wire can also be used. In this case, the propagation of the binary signal alternates between the two polarizations [4].

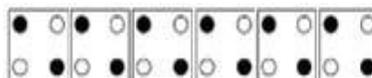


Fig. 2.1. QCA wire (90°)

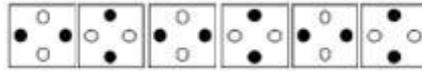


Fig. 2.2 QCA wire (45°)

QCA Inverter: The QCA cells can be used to form the primitive logic gates. The simplest structure is the inverter shown in Fig. 3, which is usually formed by placing the cells with only their corners touching. The electrostatic interaction is inverted, because the quantum-dots corresponding to different polarizations are misaligned between the cells [3].

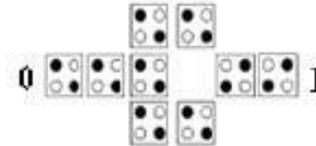


Fig. 3. QCA inverter

QCA Majority Gate: The QCA majority gate performs a three-input logic function. A layout of a QCA majority gate is shown in Fig. 4.1. Assuming the inputs are a, b and c, the logic function of the majority gate is

$$M(a, b, c) = ab + bc + ac. \quad (1)$$

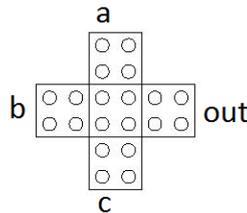


Fig. 4.1. QCA majority gate

The tendency of the majority device cell to move to a ground state ensures that it takes on the polarization of the majority of its neighbours. The device cell will tend to follow the majority polarization because it represents the lowest energy state [3]. By fixing the polarization of one input to the QCA majority gate as logic “1” or logic “0” an AND gate or OR gate will be obtained, respectively, as shown in Fig. 4.2.

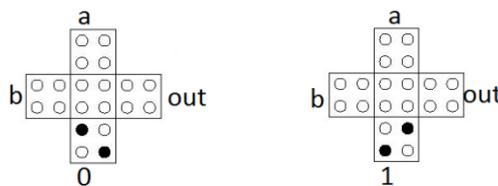


Fig. 4.2. 2-input AND and 2-input OR gates

III. CLOCKING

The QCA circuits require a clock, not only to synchronize and control information flow but also to provide the power to run the circuit since there is no external source for powering cells. With the use of four phases clocking scheme in controlling cells, QCA processes and forwards information within cells in an arranged timing scheme. Cells can be grouped into zones so that the field influencing all the cells in the zones will be the same. A zone cycles through 4 phases. In the **Switch** phase, the tunneling barriers in a zone are raised. While this occurs, the electrons within the cell can be influenced by the Columbic charges of neighboring zones. Zones in the **Hold** phase have a high tunneling barrier and will not change state, but influence other adjacent. Lastly, the **Release** and **Relax** decrease the tunneling barrier so that the zone will not influence other zones. These zones can be of irregular shape, but their size must be within certain limits imposed by fabrication and dissipation concerns. Proper placement of these zones is critical to design efficiency. This clocking method makes the design of QCA different from CMOS circuits. [7].

The Fig. 5. Shows the four available clock signals. Each signal is phase shifted by 90° degrees. When the clock signal is low the cells are latched. When the clock signal is high the cells are relaxed and have no polarization. In



between the cells are either latching or relaxing when the clock is decreasing/increasing respectively.

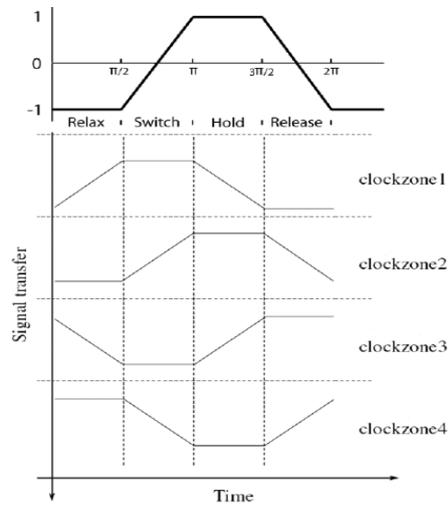


Fig. 5. Four phases of the clock.

IV. QCA DESIGNER TOOL

QCA logic and circuit designers require a rapid and accurate simulation and design layout tool to determine the functionality of QCA circuits. QCADesigner gives the designer the ability to quickly layout a QCA design by providing an extensive set of CAD tools. As well, several simulation engines facilitate rapid and accurate simulation. It is the first publicly available design and simulation tool for QCA. Developed at the ATIPS Laboratory, at the University of Calgary, QCADesigner currently supports three different simulation engines, and many of the CAD features required for complex circuit design. [8],[9].

V. QCA IMPLEMENTATION

The AND and OR gates are realized by fixing the polarization to one of the inputs of the majority gate to either $P=-1$ (logic 0) or $P=1$ (logic 1).

The same logic is used in the five-input complex gate. This gate is composed of a 3-input majority gate which is placed in the middle of the complex gate. Here the input 'e' functions as a control input that is used to specify the functionality of the circuit. The remaining four inputs a, b, c and d are used to implement logical functions such as AND and OR. The functionality of this gate for four input AND and OR configurations has been simulated using QCA Designer. Fig. 6 shows five-input complex gate with a majority gate placed in the middle.

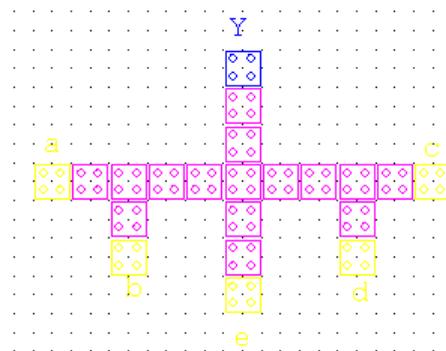


Fig.6 Five-Input complex gate

A. Four-Input AND Gate

The five-input gate of Fig. 6 can be used to form a four input AND gate as shown in Fig. 7.1 by restricting input e to have a fixed polarity that is equal to -1. The selection of 'e' is unique. For the example circuit as shown in Fig.7.1, the function represented is $Y=abcd$.

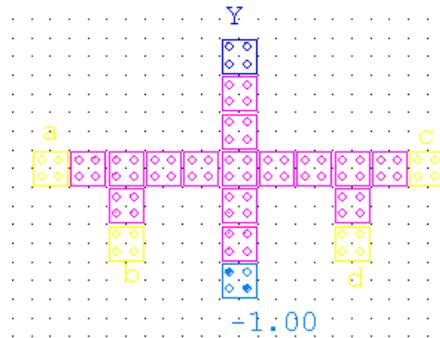


Fig.7.1 Four input AND gate

B. Four-Input OR Gate

Similarly, the five-input gate of Fig. 6 can also be used to form a four input OR gate as shown in Fig. 7.2. For this configuration the input e is restricted to have a fixed polarity that is equal to 1. As for the AND gate, the selection of e is unique. For the remaining cells, the same symmetry is present in the OR gate as in the previously described AND gate. The function represented is $Y=a+b+c+d$.

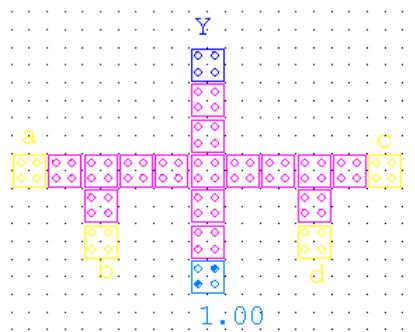


Fig. 7.2 Four input OR gate

VI. SIMULATION RESULTS

With QCADesigner, the circuit functionality is verified. The following parameters are used for a bistable approximation: Cell size 18nm, Number of samples 12800, Convergence tolerance 0.001000, Radius of effect 65nm, Relative permittivity 12.9, Clock high 9.8e-22J, Clock low 3.8e-23J, Clock amplitude factor 2, Layer separation 11.5nm, Maximum Iterations per sample 100.

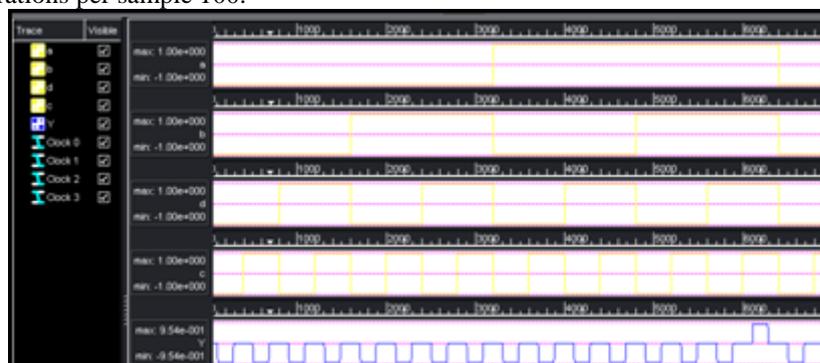


Fig.8.1 Simulation result for four input AND gate

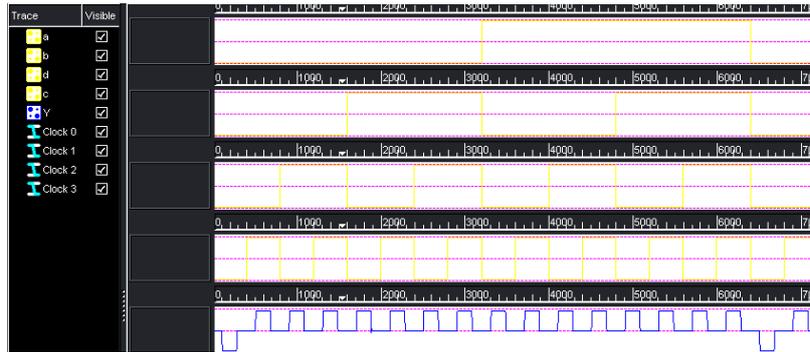


Fig.8.2 Simulation results for four input OR gate

VII. CONCLUSION

The logical structures such as AND and OR using five-input complex gate composed of a 3-input majority gate have been designed. One of these inputs typically functions as control inputs to determine the logical structure formed by the four other inputs to the circuit. This five-input gate can be configured as a four-input AND gate and a four-input OR gate which are verified through simulation results.

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