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Quadruple Boost Switched Capacitor-Based Inverter forStandalone Applications

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ABSTRACT: Conventional energy sources will not be sufficient to meet future electrical demands, and also pollute the environment. Therefore, to meet their electrical energy needs, and maintain clean and green environmental conditions, people are focusing more on renewable energy sources. Small-scale PV solar standalone AC loads or grid integration applications need high voltage at a desired level, transformer/inductor less operation, high gain DC-DC front-end converters, and DC-AC converters. To achieve all the above objectives, this paper proposes a step-up quadruple boost nine-level inverter, it works on switched capacitor technique with a reduced count of components for the application of renewable energy systems. The proposed topology balances the capacitor voltages with the control scheme itself without using any sensors. A level- shifted pulse-width modulation (LPWM) technique can be used in the control strategy of the proposed topology. This paper covers the operational modes of the proposed topology, voltage stress calculations, capacitors calculations, and losses calculations at various stages and compared with recent literature, that reveals this topology is more advantageous in terms of less total standing voltage, switch count, cost factor, better efficiency and the number of gate driver circuits. The theoretical performance can be validated through MATLAB/Simulink-based simulation and their results are validated through prototype experimentation. Further, the experimental results contain modulation index variations, frequency modulation, switching frequency variations, input voltage variations, and load variations. Finally, the max efficiency of 96.5% is achieved for the experimental prototype of the proposed topology.

KEYWORDS: Switched capacitor, high gain inverter topologies, solar PV, self-voltagebalance, level shifted pulse width modulation.

I. INTRODUCTION

The demand for electrical energy can increase rapidly throughout the world from day to day. Electrical energy is majorly generated by the combustion of fossil fuels like coal, petroleum, natural gas, and nuclear materials. Those materials can expose harmful gases to the environment, which leads to an environmental imbalance that can exist throughout the world. The solution to meet the demand for increasing electrical energy, with environmentally friendly renewable energy sources is gaining more popularity. Renewable energy generating stations are far away from the load centers. There- fore, the transmission and distribution losses are increased to deliver the electrical energy from generating stations to load centers.To overcome this problem, rooftop distributed solar PV systems are introduced in current years. The available power and voltage ratings for small-scale solar PV rooftop systems are 0.5kw-5kw and 60-100v [1], [2], [3]. To supply the AC powerat distributed voltage levels, the available R.M.S voltages are 230V for a single phase and 415V for a three-phase system. Solar rooftop PV cells can generate power in D.C nature at lower voltage levels.

II. OBJECTIVE

- Maximizing energy conversion efficiency to make the system suitable for off-grid and standalone applications where energy resources are limited.
- Enhancing voltage boosting capabilities to efficiently convert low-voltage inputs, such as those from renewable energy sources like solar panels or wind turbines, into usable AC power.
- Minimizing system size, weight, and cost to improve portability and affordability for deployment in remote or rural areas.
- Ensuring reliability and robustness to withstand variations in input voltage, load fluctuations, and environmental conditions commonly encountered in standalone power systems.
- Facilitating seamless integration with energy storage systems, enabling the system to store excess energy for use during periods of low generation or high demand.
- Optimizing control algorithms for efficient operation and management of the inverter under various operating

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conditions.

- Conducting performance evaluations and validation tests to demonstrate the effectiveness and viability of the proposed inverter design for standalone applications.

III. EXISTING METHODOLOGY

- For the generation of pure sinusoidal signal, SPWM is the most popular technique.
- In SPWM a digital waveform is generated and the duty cycle is modulated such that the average voltage of the waveform is corresponds to a pure sine wave.
- SPWM moves the voltage harmonic components to the higher frequencies.
- The SPWM technique treats each modulating voltage as a separate signal and compared to the common carrier triangular waveform.

IV. PROPOSED METHODOLOGY

The proposed topology has the following dominant features :

- Single DC source is used to get 9 levels with quadruple voltage gain.
- Less number of components (10 switches and 2 capacitors)
- Self-balancing of the capacitors with the control scheme.
- For charging the capacitor,only 01 switch is enough. So, conduction losses are reduced
- Four out of 10 switches have only one transition in a cycle. So, switching losses are minimised.

IV. BLOCK DIAGRAM

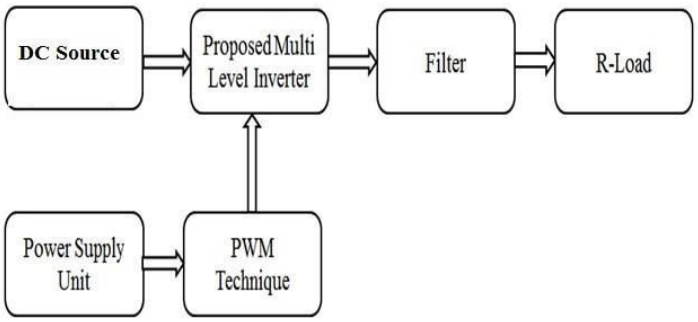

Fig.1 – Block Diagram

V. PROPOSED TOPOLOGY

V_O	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	C_1	C_2
$+4V_{dc}$	0	0	1	1	0	0	1	0	0	1		↓
$+3V_{dc}$	1	0	0	1	1	0	1	0	0	1	-	↓
$+2V_{dc}$	0	1	1	0	0	1	1	0	0	1	↓	↑
$+V_{dc}$	1	1	0	0	1	0	1	0	0	1	↑	-
0	0	0	0	0	0	0	1	0	1	0	-	-
$-V_{dc}$	1	1	0	0	1	0	0	1	1	0	↑	-
$-2V_{dc}$	0	1	1	0	0	1	0	1	1	0	↓	↑
$-3V_{dc}$	1	0	0	1	1	0	0	1	1	0	-	↓
$-4V_{dc}$	0	0	1	1	0	0	0	1	1	0	↓	↓

Fig.2 - Proposed Topology

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VI. PROPOSED TOPOLOGY WORKING

SWITCHING STRESS AND TSV CALCULATIONS:

In this topology, switches S_7, S_8, and S_9, and S_{10} operate in complement mode, with a peak inverse voltage (PIV) of 4Vdc. The suffix even number switches S_2, S_4, and S_6 having peak inverse voltage 2Vdc. The suffix odd number switches S_1, S_3, and S_5 have peak inverse voltage 1Vdc. TSV of the proposed inverter is less because more switches have lesser peak inverse voltage (PIV). The mathematical expression for TSV calculation is represented in TSV of the proposed topology is 6.25, then each switch's peak inverse voltages at various output voltage levels are plotted in a bar chart with different colors.

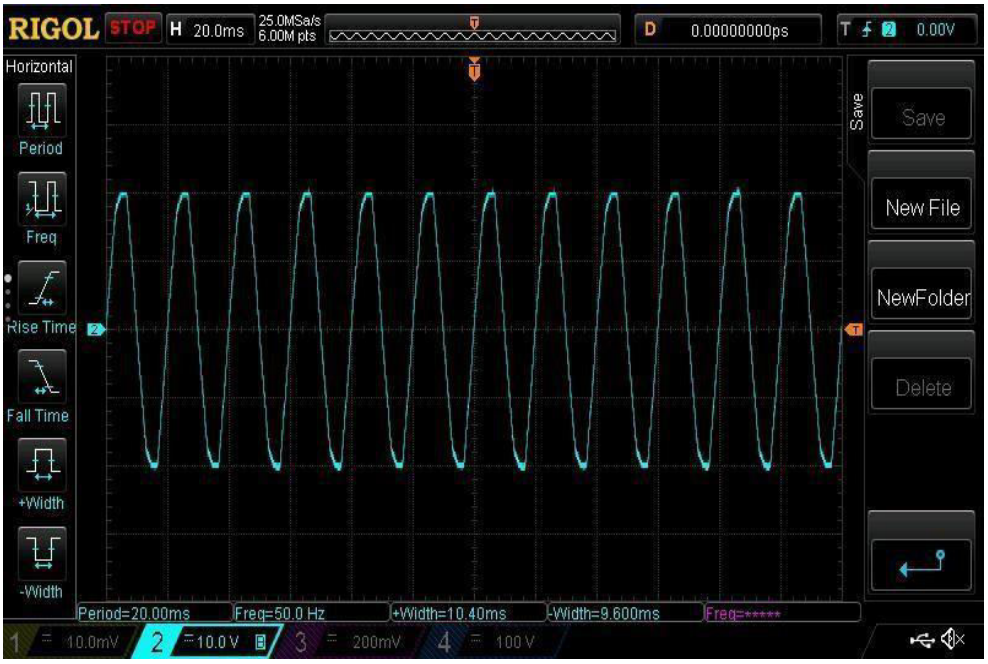

Fig.3 - AC link Voltage from Grid

Fig.4 - Buck Mode Pulses

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WAVEFORM -2

Fig.5 - Main AC source

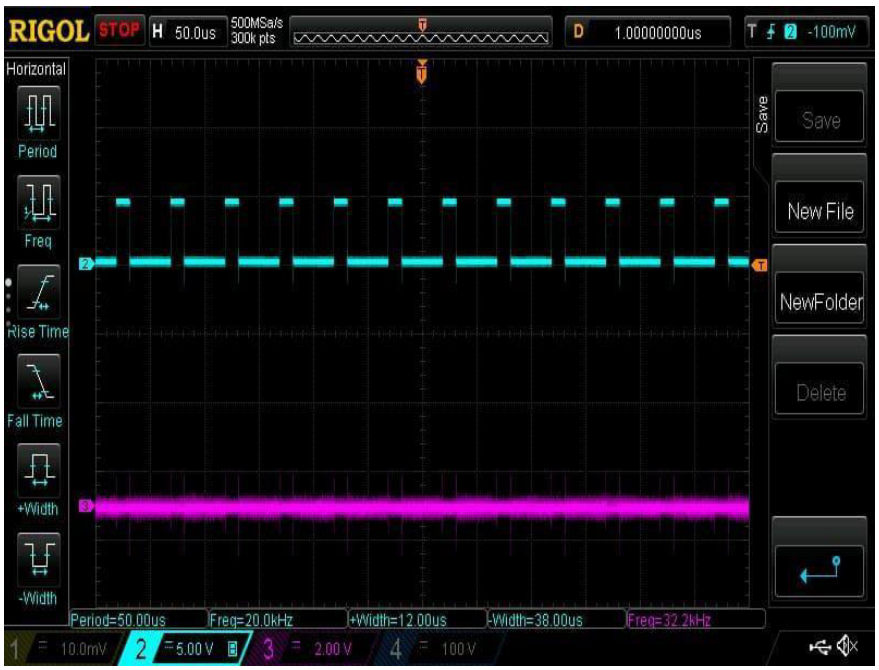

Fig.6 - Boost Mode Pulses

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VII. CIRCUIT DIAGRAM

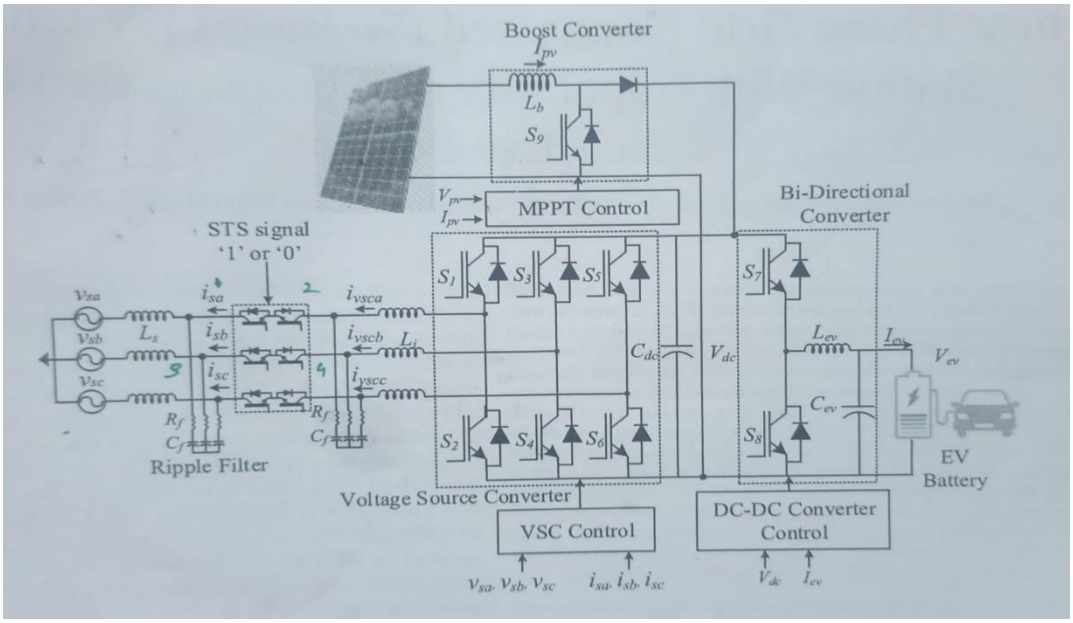

Fig.7 – Circuit Diagram Quadruple Boost Switched Capacitor-Based Inverter

VIII. OFTWARE UNIT

MICROPROCESSOR:

This Versatile programmer is a dedicated PIC Micro controller Programmer. All the PIC series of IC's except the 17 series can be programmed with this Hardware through RS232 Port of PC. This programmer also supports ICSP programming for on board programming of supported flash PIC devices. MPLAB IDE, PIC CCS C compiler Demo softwarewith MPLAB Plug-in, and programming instructions are provided in CD-ROM. The programmer software is compatible to Windows 98, Windows 2000, and Windows XP platforms. A Soft copy of the user manual is also included in the CD, inaddition to the hard copy provided with the Kit. This Dedicated programmer is for programming a wide range of PIC Microcontrollers including EEPROMS, PIC12 series, PIC16 series & PIC18 series of IC's.

SPECIFICATIONS:

- Auto detection of programmer by software
- Regulated Power supply 5,13.5V
- Auto Flash upgrades through serial port
- 16 MHz crystal Oscillator
- Built in RS232 connector
- ZIF socket for easy programming
- External ICSP Interface for on board programming
- Programmable configuration and ID
- Selective Erase and programming for supported PIC Devices
- Manual / Auto Reset
- Configurable COM Port.
- Program, Read, Verify and Blank check Modes
- Hex Code Editor
- Program & Verify fly Window
- Switchable to MPLAB software
- Extensive Integrated Help
- Debug vector Read & write

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- Oscal value read & program (for selected chips)

MPLAB:

MPLAB Integrated Development Environment (IDE) is a free, integrated toolset for the development of embedded applications on Microchip's PIC and dsPIC microcontrollers.

HI-TECH Software is an Australian-based company that provides ANSI C compilers and development tools. Founded in 1984, the company is best known for its HI-TECH C PRO compilers with whole-program compilation technology, or Omniscient Code Generation (OCG). HI-TECH Software was bought by Microchip on 20 February 2009, whereupon it refocused its development effort exclusively on supporting Microchip products.

The HI-TECH C Compiler for PIC10/12/16 MCUs (Lite mode) is a freeware compiler. It supports all PIC10, PIC12and PIC16 series devices.The features of HI-TECH C Compiler are listed as followings:

- Fully compatible with Microchip's MPLAB IDE
- Fully ANSI-compliant
- Includes Library source - for standard libraries and sample code for I/O drivers
- Includes macro assembler, linker, preprocessor, and one-step driver
- Runs on 32/64-bit Windows, Linux and Mac OS X

PROTEUS:

This package splits into three parts very conveniently namely: -
- ISIS : Intelligent Schematic Input System - for drawing circuit diagrams etc.
- ARES : Advanced Routing and Editing Software - for producing pcb layout drawings.
- LISA : Labcenter Integrated Simulation Architecture - for simulation of circuit diagram. Separate handout.

PROTUES VIRTUAL SYSTEM MODELLING (VSM):

PROTUES combines advanced schematic capture, mixed mode SPICE simulation, PCB layout and auto routing tomake a complete electronic design system. The PROTUES product range also includes our revolutionary VSM technology, which allow you to simulate micro-controller based design, complete with all the surrounding electronic.

INTELLIGENT SCHEMATIC INPUT SYSTEM (ISIS):

ISIS lies right at the heart of the PROTUES system and is far more than just another schematic package. It has powerful environment to control most aspects of the drawing appearance. whether your requirement is the rapid entry of complex design for simulation & PCB layout, Or the creation of attractive Schematic for publication **ISIS** is the right tool for the job.

IX. CONTROLLER UNIT

A Microcontroller (sometimes abbreviated µC, uC or MCU) is a small computer on a single integrated circuit containing a processor core, memory, and programmable input/output peripherals. Program memory in the form of NOR flash or OTP ROM is also often included on chip, as well as a typically small amount of RAM. Microcontrollers are designed for embedded applications, in contrast to the microprocessors used in personal computers or other general purpose applications.

PICs are popular with both industrial developers and hobbyists alike due to their low cost, wide availability, largeuser base, extensive collection of application notes, availability of low cost or free development tools, and serial programming (and re-programming with flash memory) capability. Microchip announced on September 2011 the shipment

X. WORKING

- It has one DC voltage source, two capacitors (C1,C2), and ten switches (IGBT/MOSFET), of which three are Bi-

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directional switches (S1, S2, S6) and seven are unidirectional switches (S3, S4, S5, S7, S8, S9, S10).

- To prohibit a short circuit between the DC voltage source and the capacitors, the switches S7, S8, and S9, S10 work in conjunction with one another.
- The two capacitors (C1, C2) are charged and discharged parallel and in series to DC voltage source to produce the desired voltage levels.
- The capacitors C1, as well as C2, are charged and discharged to +1Vdc and +2Vdc respectively. Hence, the voltages across the capacitors are self-balanced.
- The output voltage levels across the load are ±4Vdc, ±3Vdc, ±2Vdc, and ±1Vdc. The charging and discharging of the capacitors are done by the parallel/series technique.
- Either the two switches of the upper arm or lower arm are switched ON to attain the zero-voltage level. The single switch is enough to charge capacitors. Therefore, the **13** proposed topology can reduce switching losses.

XI. IMPLEMENTATION

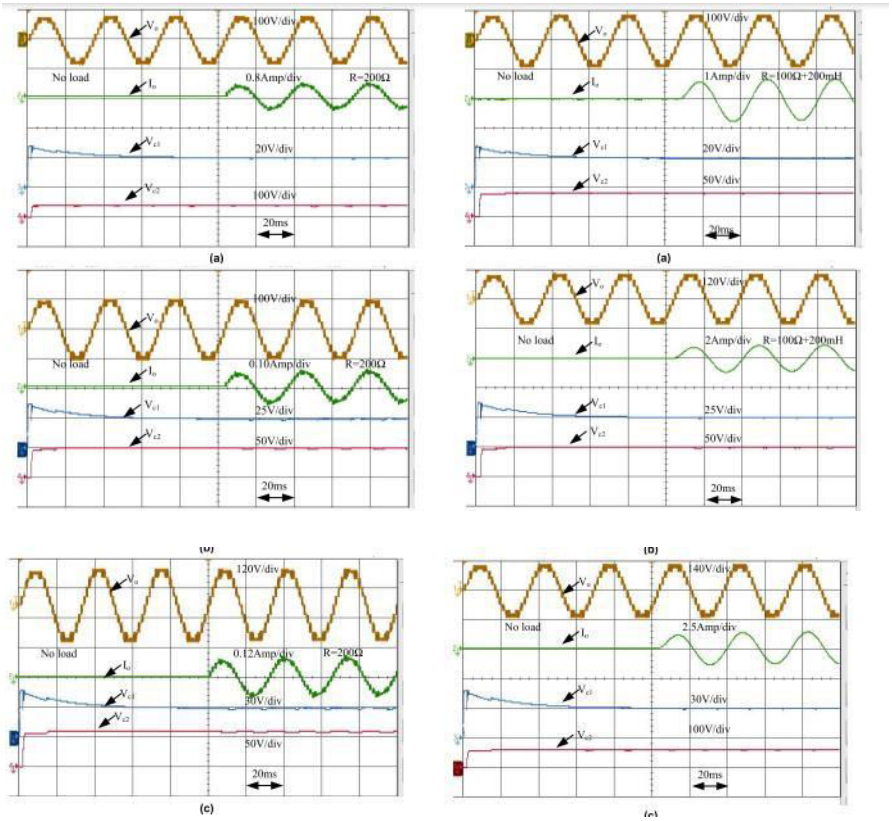

Fig.8 - Waveform

XII. CONCLUSION

In this article, a single DC Source new step up nine level inverter was reported with a reduced count of components for solar PV stand alone system. The proposed topology with quadruple voltage gain capability operates with the parallel/series-charging/discharging technique of the capacitor. An LSPWM technique was used for balancing the capacitor voltages to achieve the desired output voltage and also to get lower stress on the components. Furthermore, the experimental setup of the proposed topology can be tested at different load conditions, input voltage variations, amplitude modulation variations, switching frequency variations, and frequency modulation variations. The THD of the output voltage and voltage ripples of the capacitors are within the limits. Moreover, a comparative analysis reveals that the proposed topology has simple structure, lower switch count, quadruple boosting capability, higher efficiency, less cost factor and less T.S.V(p.u) .

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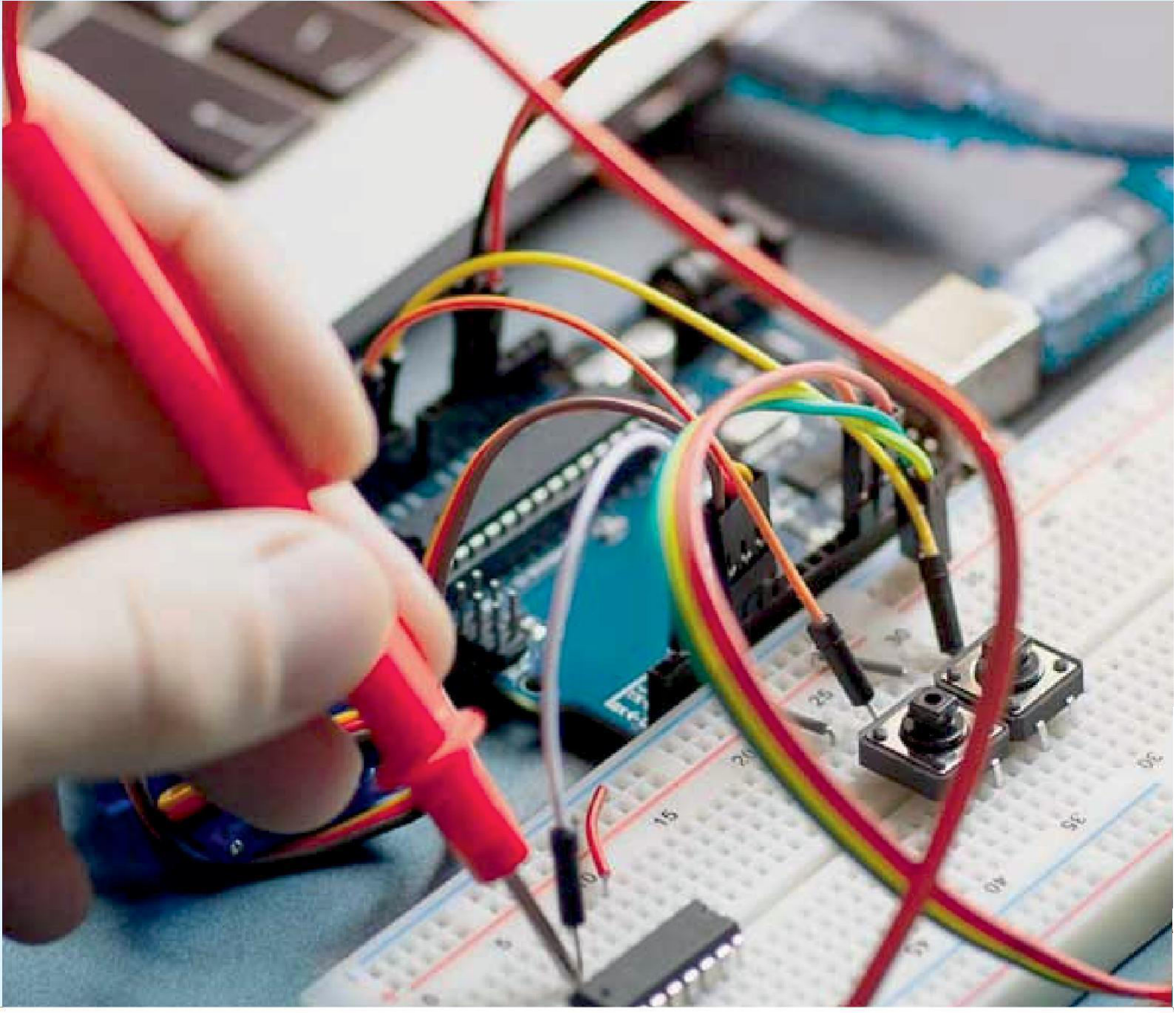

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