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Area Efficient Virtual Channel Router Architecture for Scalable Network on Chips

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ABSTRACT: Network on Chips (NoCs) have emerged as the standard communication fabric for connecting cores and memory modules on the chip. Current multi-core chips consist of hundreds of cores and future projections call for thousands of cores. However, today, NoCs consume a large portion (approximately 10%-36%) of the entire chip's power budget. The problem will be further exacerbated by the continuous scaling of transistor feature size. This calls for innovative static power reduction techniques for future NoCs design. Considering the NoC components, as crossbars, arbiters, buffers, and links, in the experiments realized by the buffers were the largest leakage power consumers, dissipating approximately 64% of the whole power budget. In this way, the buffers were considered as candidates for leakage power optimization, since even at high loads, there were still 85% of idle buffers. Regarding dynamic power, the buffers' consumption is also high, and it increases rapidly as the packet flow throughput increases. In this project, we propose a novel Shared Buffer Virtual Channel Router with Easy Pass Switch Architecture for NoC which reduces the static power using power gating and bye pass routing and reduces dynamic power using shared buffer while increasing overall .

KEYWORDS: Network-on-Chips, Power Gating, Energy Efficient

I. INTRODUCTION

Network-on-chip (NoC) architectures are essential modules for both general-purpose chip multiprocessors (CMPs) and application-specific systems-on chips (SoCs). As the number of processors on a single chip and the computing complexity increases day by day, the interconnection and communication method between the processors became essential factors affecting the performance of chip-multiprocessor. It requires more effective interconnection and communication among the processors to improve its performance, rather than depending only on the processing speed. The system requires a complete set of communication demands and characteristics of all kinds of processors, and should provide better data transmission performance in limited conditions such as chip area, power consumption, data bandwidth,etc. Therefore, it requires higher demands for on-chip communication, such as high speed, high bandwidth, high throughput while small area and low power consumption. Traditional interconnection architecture of the chipmultiprocessor, such as on-chip bus and crossbar cannot satisfy these requirements due to problems like reusability, flexibility and scalability. It needs a more perfect and effective interconnection technology

Similarly, as the numbers of cores in the processor increases, the interconnection network between the cores play a vital role in the chip multiprocessor's (CMPs) overall performance. Usually, shared buses have been used as communication medium for CMPs with a few numbers of cores. As transistors improved, resulting in higher clock frequencies, the number of clock cycles required to pass from one end of the chip to the other increases due to the reason that chip size remains the same. This results in slower bus speed than that of clock frequency of cores, as the delay of cores depends on local wires which range with transistors. As simple shared buses are unsuitable for future CMPs with hundreds to thousands of cores, the Networkon-Chips (NoCs) have emerged as a solution for designing interconnection fabric in CMPs.

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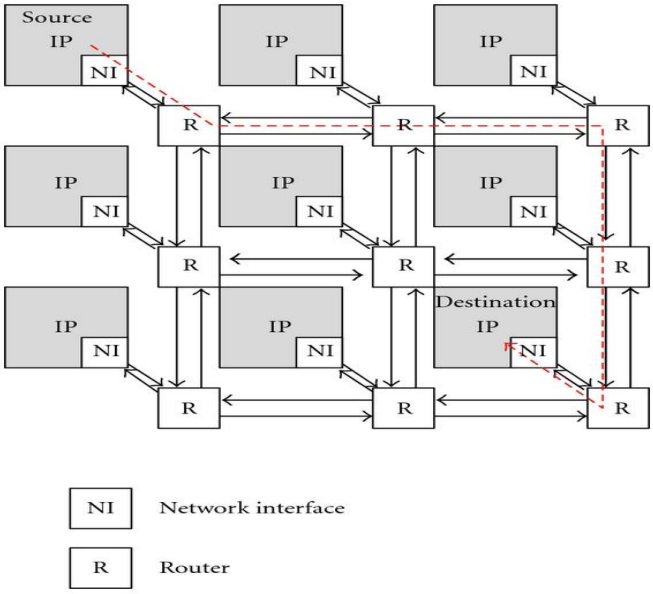

Figure 1: Typical NoC structure in a mesh topology

II. NoC ROUTER ARCHITECTURE

A typical NoC architecture consists of multiple segments of wires and routers as shown in Figure 1. In a tiled, city-block style of NoC layout, the wires and routers are configured much like street grids of a city, while the clients (e.g., logic processor cores) are placed on city blocks separated by wires. A network interface (NI) module transforms data packets generated from the client logic (processor cores) into fixed-length flow-control digits (flits). The flits associated with a data packet consist of a header (or head) flit, a tail flit, and a number of body flits in between. This array of flits will be routed toward the intended destination in a hop-by-hop manner from one router to its neighboring router.

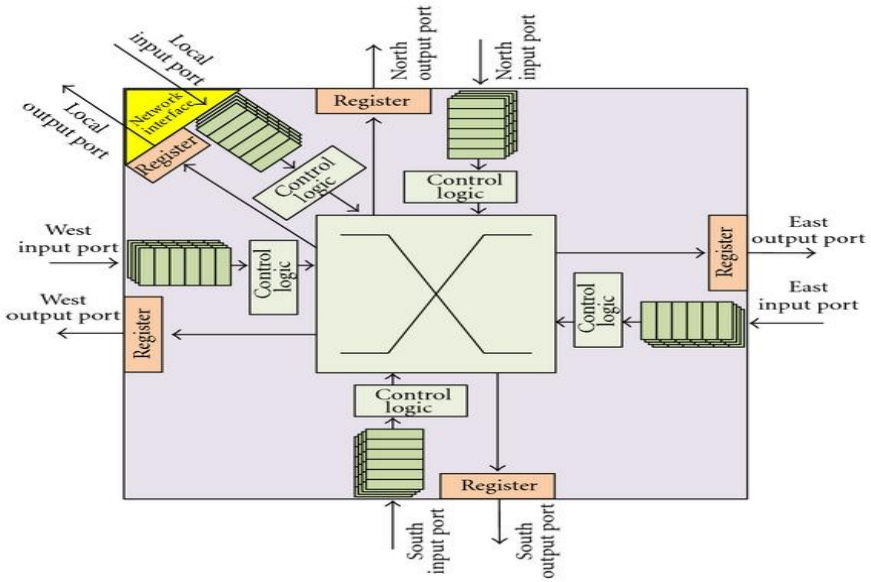

Figure 2: Typical NoC router architecture

In general, each router has five input ports and five output ports corresponding to the north, east, south, and west directions as well as the local processing element (PE). Each port will connect to another port on the neighboring router via a set of physical interconnect wires (channels). The router's function is to route flits entering from each input port to an appropriate output port and then toward the final destinations. To realize this function, a router is equipped with

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an input buffer for each input port, a 5 × 5 crossbar switch to redirect traffic to the desired output port and necessary control logic to ensure correctness of routing results.
Networks-On-Chip (NoC) architectures are becoming the effective fabric for both general-purpose chip multi-processors and application-specific systems-on-chip designs. In the design of NoCs, high throughput and low latency are both important design parameters and the router micro architecture plays a vital role in achieving these performance goals. High throughput and low latency are both important design parameters and the router micro architecture plays a vital role in achieving these performance goals. High throughout routers allow a NoC to satisfy the communication needs of multicore applications, or the higher achievable throughput can be traded off for power saving by using fewer resources to attain a target bandwidth. Ultimately, a routers role lies in the efficient multiplexing of packets over the network links.

III. PROPOSED ARCHITECTURE

A Shared Buffer Virtual Channel (VC) Router with a Easy Pass Switch based solution to the above stated problems. The Easy Pass (EZ-Pass) router which remedies the large wake-up latency overheads while providing significant static power savings. EZ Pass router consists of a conventional router that is used for high traffic mode and EZ-Pass switch for handling sporadic and low traffic modes. This allows incoming flits to be routed without fully waking up the powered-off router. The EZ-Pass switch represents a by-pass route and consists of single-flit latches, multiplexers (MUXs) and demultiplexers (DEMUXs). For example, when the router is powered-off, the incoming flits will be buffered into the single-flit latch. The EZPass control logic routes the flit using an arbitration scheme to the NI instead of the conventional router. The NI processes the incoming flit and switches it to the designated output port. The NI also records the VC information to be used later by the flow control policy.

When the traffic load becomes heavy, the router allows utilizing **shared buffers** reducing packet stall times at input ports hence it can achieve higher throughput than a full-Xbar VC router; while at low-load packets can bypass shared queues hence has low latency similar to a WH router. EZ Pass router helps to reduce static power while shared buffer helps to reduce dynamic power and assure high performance than conventional routers with pipelined route.

A packet from an input queue simultaneously arbitrates for both shared queues and an output port; if it wins the output port, it would be forwarded to the downstream router at the next cycle. Otherwise, that means having congestion at the corresponding output port, it can be buffered to the shared queues. Intuitively, at low load, the network would have low latency because packets seem to frequently bypass shared queues. While at heavy load, shared queues are used to temporarily store packets hence reducing their stall times at input ports that would improve the network throughput.

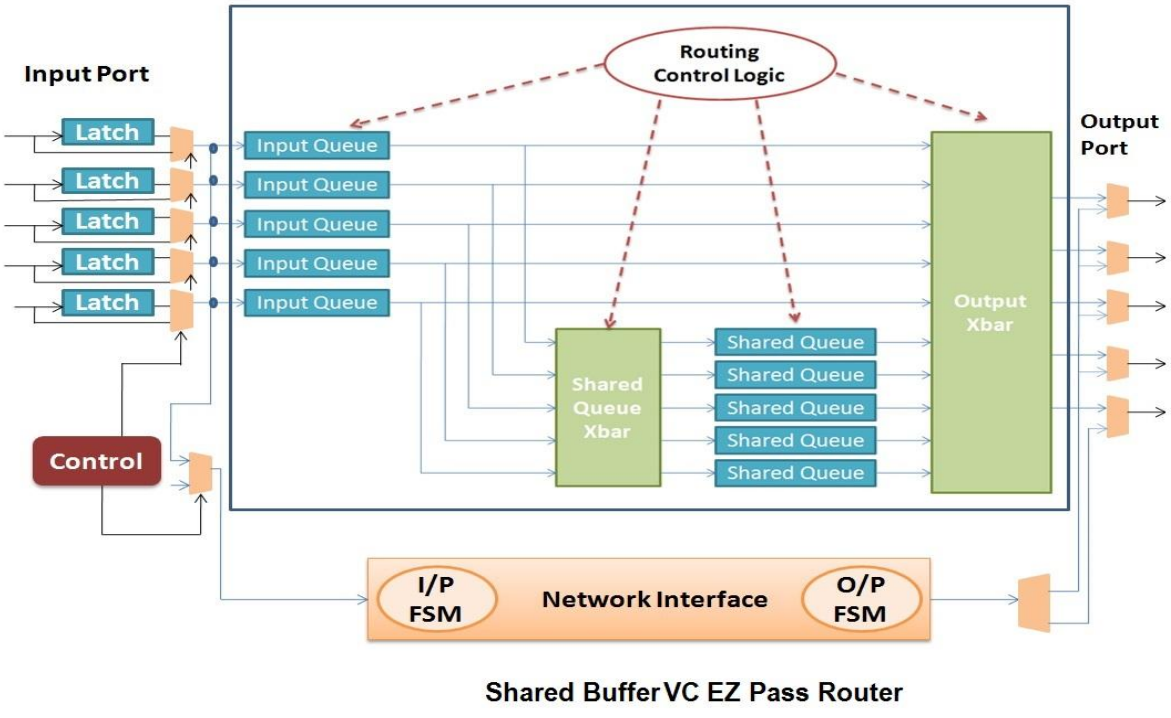

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Figure 3: Proposed EZ Pass Shared Buffer Router Architecture

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IV. SIMULATION RESULTS

Simulation Waveforms of Proposed EZ Pass Router

- When the router is power off and there is low traffic EZ Pass will work. In this waveform, depends on the input request flits are by passed to the respective output ports through NI and blue line indicating the router is power off.

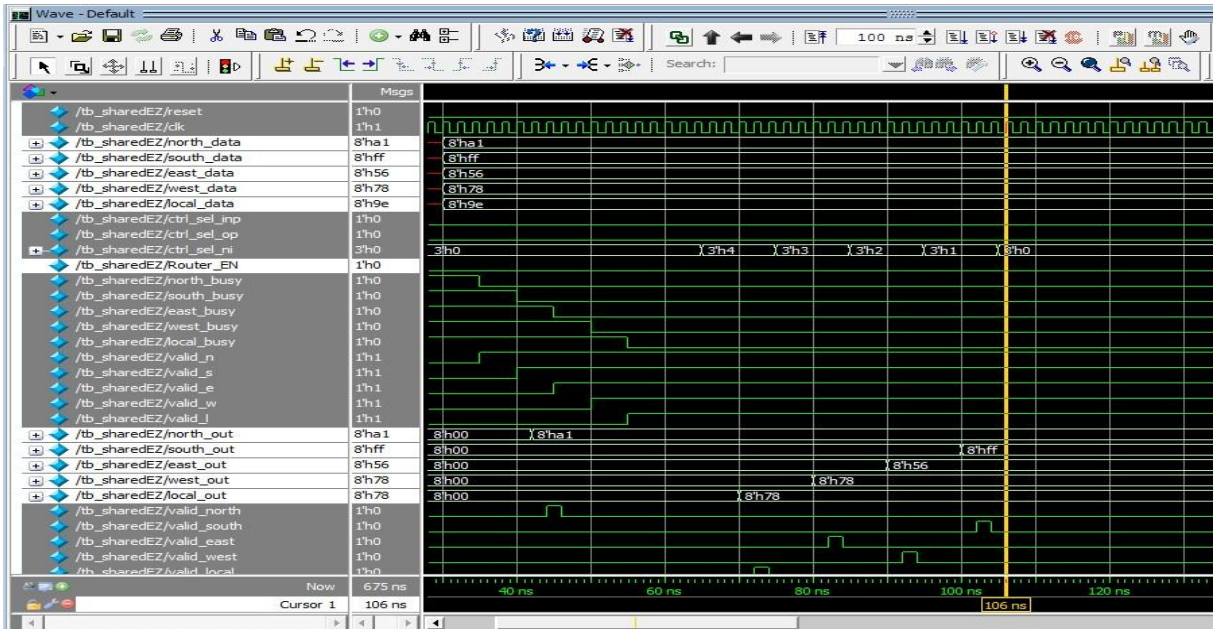

Figure 4: Simulation Waveforms of Proposed EZ Pass Router

Shared Buffer VC Router with less Network Traffic

- VC Router will work in both lower and heavy network traffic, here is the below waveforms for both the scenario.
- If it is low traffic, then the flits are routed with respect to the request signals.
- During heavy traffic, along with the request it will route with respect to priority. We assume that the priority for the ports are N, S, E, W, L(low → high)

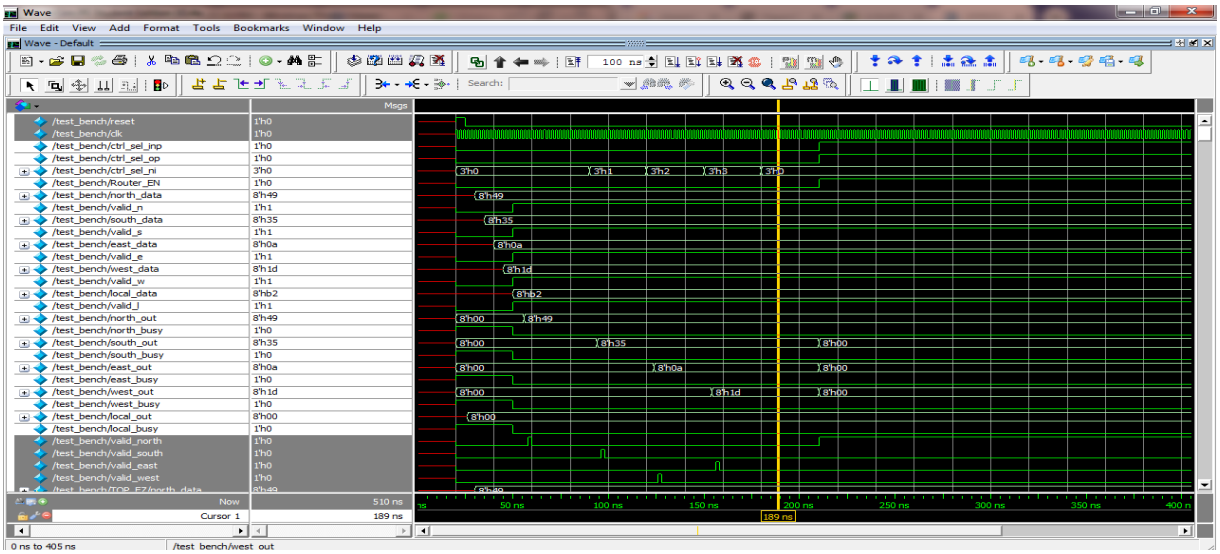

Figure 5: Shared Buffer VC Router with less Network Traffic

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Shared Buffer VC Router with heavy Network Traffic

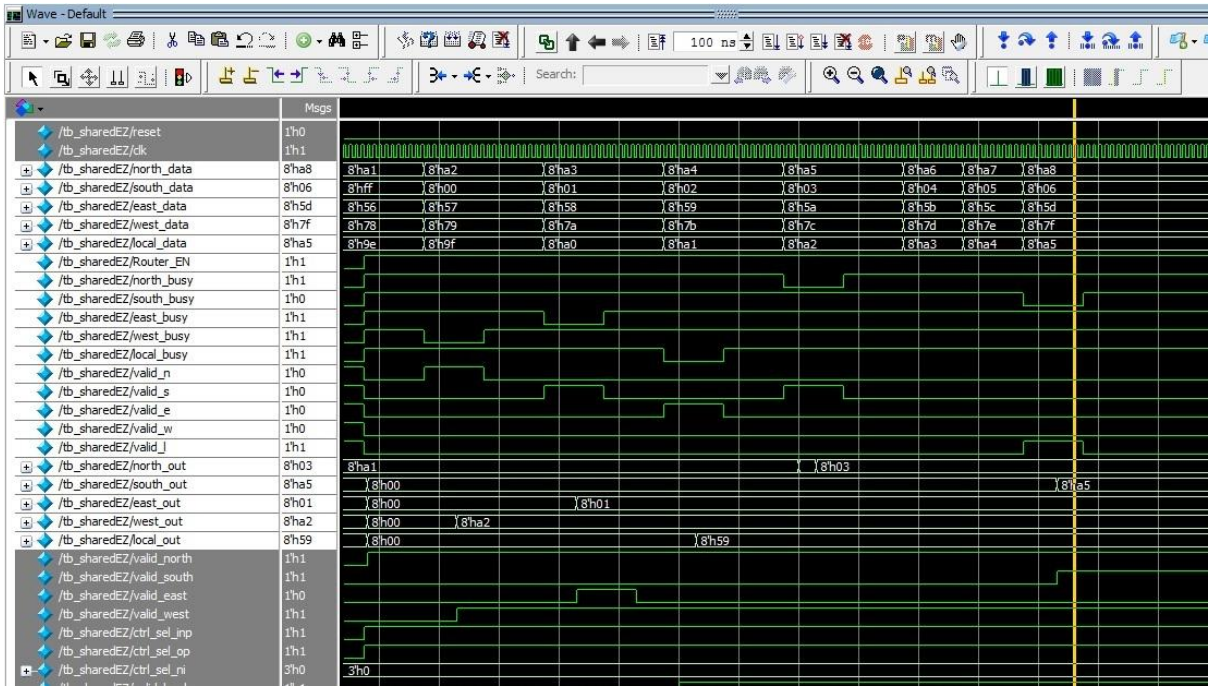

Figure 6: Shared Buffer VC Router with heavy Network Traffic

V. UTILIZATION AND POWER ANALYSIS

Resource	Utilization	Available	Utilization %
FF	349	866400	0.04
LUT	115	433200	0.03
I/O	103	1000	10.30
BUFG	2	32	6.25

Table 1: Area Utilization for Shared Buffer VC Router

Total On-Chip Power	7.145 W
Junction Temperature	31.1°C
Thermal Margin	53.9°C (61.5 W)
Power supplied to off-chip devices	0 W

Table 2: Power Values for Shared Buffer VC Router

VI. FUTURE SCOPE

As the future of Network on Chip will be much more complex, the cores in CMPs will become even hungrier. The packet-switched networks are assured to take a major role in addressing the complex system design and throughput problems of future complex systems-on-chip. Hence we need to focus towards the development of self repairable, fault resilient and fully adaptive routing architectures. The concept of 3D NoC is also considered to be another promising alternative for next generation nano system design. We can improve and modify our proposed EZ Pass VC Router architecture in the context of 3D NoCs / 3D MPSoC chips. Since our VC router uses more buffers in each port for routing, there is another important scope of buffer sharing logic towards achieving dynamic power reduction of VC Router. Error correction mechanism can be added inside Network Interface (NI) Unit as an additional feature.

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VII. CONCLUSION

The proposed router architecture is a deadlock-free and can support any network topology in NoCs. The EZ pass router offers Low latency & High throughput which is also most energy efficient and suitable for emerging massive NoC chips in the current IP industry. Unlike previously proposed routers for NoCs, the proposed architecture provides a simple by-pass routing mechanism to route messages during low traffic without completely waking up the powered-off router. This efficient mechanism improves power savings and network latency. Our results can prove that overall network latency and static power can be reduced by significantly. The proposed EZ Pass Router architecture makes the on chip communication faster and provides higher communication bandwidth. With the availability of VC router for higher traffic, it also ensures concurrent execution of processing elements, incurring modularity in the network. The proposed architecture effectively utilizes the Network Interface (NI) unit. It acts as intermediary system between the routers and processing elements and is responsible for generating, transmitting, and receiving of data packets amongst IP cores at same time working as a channel for by pass switch during low traffic.

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