



DC Power Balance during Charging of Electric Vehicles

Pooja Suman¹, Dr. M. S. Raviprakash²

PG Scholar (CAID), Dept. of Electrical Engineering, MCE, Hassan, Karnataka, India¹

Vice Principal, Professor, Dept. of Electrical Engineering, MCE, Hassan, Karnataka, India²

ABSTRACT: The charging station based on the neutral-point-clamped (NPC) converter, which is used as a central high power converter can bring many merits, but it has unbalanced power problems in the bipolar DC bus. This issue can be overcome by the use of comprehensive dc power balance management (PBM) in conjunction with high-power three-level dc-dc converter based fast charger is proposed. The control model for the fast charger with comprehensive DC power balance management uses the advantages of active DC power balance management (APBM) and passive DC power balance management. The APBM is proposed to assist the central NPC converter in balancing power so that the additional balancing circuit is eliminated. Also a passive DC power balance management (PPBM) is proposed to eliminate the fluctuating neutral-point currents to ensure the balanced operation of fast chargers. The MATLAB/Simulink based simulation studies are being carried out to arrive at the results.

KEYWORDS: Electric vehicles (EVs), Bipolar DC bus architecture; Neutral point clamped (NPC) converter, three level DC-DC converter, Comprehensive DC power balance management.

I. INTRODUCTION

The EVs are increasing their market due to the fact that the reduced green house gas effects, less impact on the environmental pollution when compared to internal combustion engine vehicles (ICEVs). The main concerns of the consumers when purchasing an EV are the range per charge, availability of the charging station, charging time. Hence there is a urgent need to develop the high power charging station architecture all over towns and cities so that the use of EV also increases.

This high power charging station architecture uses a common AC bus and common DC bus architecture. The use of common DC bus architecture for the purpose of fast charging is more in use due the use of lesser converter stages, reduced voltage stress, flexibility of operation. The main advantage of this is it allows easy integration of the renewable energy resources and the storage system for the effective load management. This architecture can be realized by the unipolar DC bus architecture with voltage source converter and bipolar architecture with three level high powers NPC converter. Fig. 1 shows the bipolar DC bus architecture with central high power three level NPC converter which acts as a grid interface.

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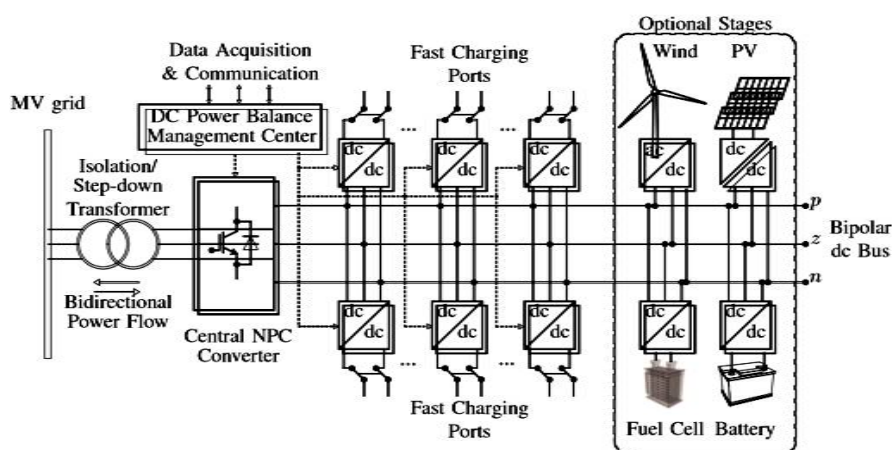


Figure 1. Bipolar DC bus architecture with central high power NPC converter.

This NPC converter has many advantages than a two level voltage source converter like it reduces dv/dt ratio, reduces voltage stress, reduces THD and provide superior harmonic performances. In spite of these advantages it suffers from the power imbalance problems as the loads can be connected to all the three buses and that loads in the system are not constant and they show stochastic behavior. This imbalance power leads to current fluctuations on the load grid side which results in unbalanced voltage and even damages the equipment. This problem can be overcome by the use of three level DC-DC converter, where it balances the power allowing the NPC converter to control the fluctuating current on the grid side.

II. THREE LEVEL DC-DC CONVERTER

The proposed structure of the three level DC-DC converters for high power fast chargers is presented in figure 2. It mainly consists of two parallel three level DC-DC converter units that handle the high charging current. The terminals p, z, n directly fit to bipolar DC bus of central charging station. Each unit consists of 4 commutation devices IGBT/diodes, two output inductors. As it contains common input filter capacitors C_{i1} , C_{i2} and common output filter capacitor C_f the power capacity can be easily scaled up to the required range. By using this configuration in fig.2 four stages of operation can be performed. The waveforms produced by the inner switches are complimentary to that produced by the outer switches. The four stages of operation are presented in fig. 3. Where the numbers 23, 13, 24, 14 indicates which switches are turned on. If the switches 23 and 14 are turned on then $V_0=0$ and $V_0=2V_i$. The gate signals has no phase difference (gate signal has 0 phase difference) as there is no flow of current through the neutral point. When switches 13 and 24 are turned on $V_0=V_i$, but there is opposite flow of current in neutral point which affects the power balance (the gate signal has 180° phase difference). When these switches are turned on there is a need to do the power balancing principles to overcome the imbalance power.

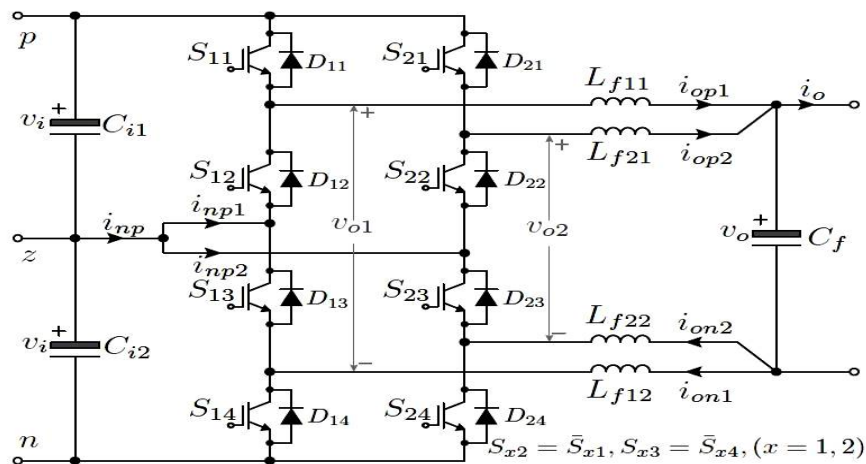


Figure 2. Three level DC-DC converter configuration.

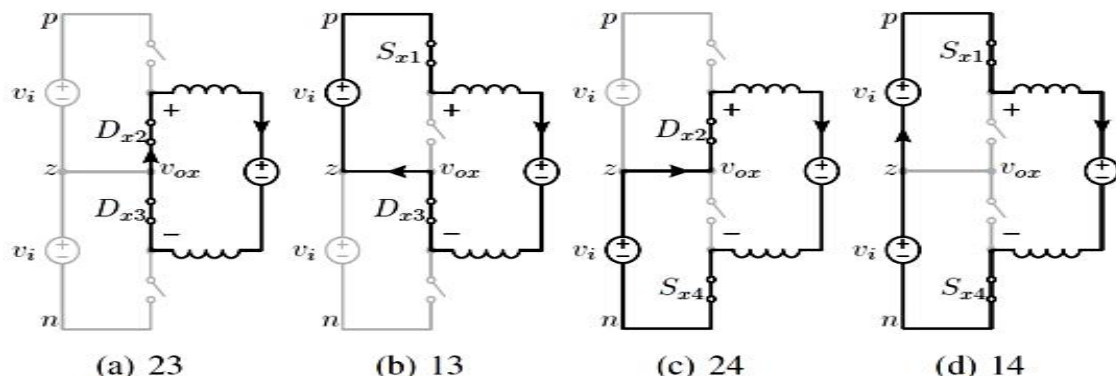


Figure 3. Equivalent circuits of four operating stages.

III. PROPOSED METHODOLOGY

In order to assist the balancing power between the DC buses and to remove the additional balancing circuits, the APBM and PPBM is proposed. Under APBM mode the fast chargers perform the power balance task actively so that the NPC converter can control the grid side currents, which results in better power quality. During this mode of operation the four switching modes of operation is performed as presented in fig. 3. Under balanced power conditions the duty cycles of outer switches $d_{x1}=d_{x4}=d$ i.e. when switches 23 and 14 are turned on. But in the presence of unbalances they must be regulated to different values. When $P_p < P_n$ the dwell time for stage 24 is decreased while time for stage 13 is increased, When $P_p > P_n$ the dwell time for stage 13 is decreased resulting in $d_{x1} < d_{x4}$, the output voltage V_{ox} remains same in all stages but the current i_{np} changes from positive average value to negative average value.

In PPBM principle the virtual disconnection of the neutral point is done making it to work as a two level converter connected to the total DC bus directly. It minimizes the presence of neutral point current and provides balance power operation of the fast chargers. The fast chargers operating in PPBM mode has no unbalanced power between the DC buses as the neutral point current is zero but it cannot balance the dc power actively hence it is called PPBM.

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A. Comprehensive DC Power Balance Management

The comprehensive DC power balance management combines the advantages of both APBM and PPBM. When the imbalanced power is larger than the predefined value then APBM is activated to assist it in balancing power. When the imbalanced power is smaller than the predefined value than PPBM is activated to reduce the fluctuating neutral point current. The transition between APBM and PPBM is triggered by the difference between P_p and P_n .

$$\begin{aligned} \text{PBM} &= \text{APBM}, \text{ when } \Delta P \notin [-P_b, P_b] \\ \text{PBM} &= \text{PPBM}, \text{ when } \Delta P \in [-P_b, P_b] \end{aligned} \quad (1)$$

The control model for the fast charger with comprehensive DC power balance management is shown in fig. 4. The CP (charging profile) provides the reference voltage v_o^* , current i_{o2}^* and the switching signal s_c to control transition between CC and CV charging mode. The lower grey box shows the comprehensive DC power balance management. The balance power is controlled with two PIs, generating control signals. Depending on the power flow direction the balanced control signal will be obtained.

$$\begin{aligned} \Delta d_x &= \min \{d_{x1}, d_{x4}\}, d_{x1}, x_4 \leq 0.5 \\ \Delta d_x &= 1 - \max \{d_{x1}, d_{x4}\}, d_{x1}, x_4 > 0.5 \end{aligned} \quad (2)$$

In the above equation d_{x1} and d_{x4} are the generated duty cycles to turn on and off the particular switches. If the PPBM is chosen the switching signals for the two units must be 180° phase shifted.

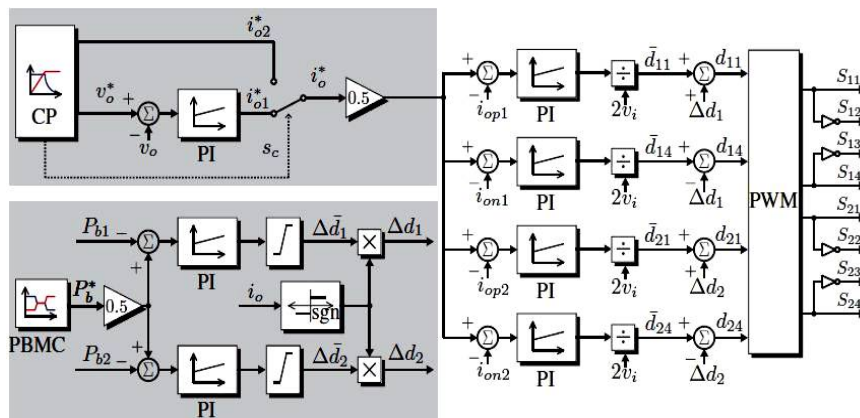


Figure 4 The control model of comprehensive DC power balance management for the fast charger.

IV. SIMULATION OF PROPOSED CIRCUIT AND DISCUSSION OF RESULTS

The proposed fast charger with comprehensive DC power balance management is simulated by using MATLAB/Simulink. 240kW converter is designed as given in the table 1.

Table 1 Simulation Parameters

Parameter	System	Simulation Value
Base voltage	V_b	600 V
Total dc voltage	V_i	1980V
Input capacitance	C_i	0.0678
Output inductance	L_f	0.0115
Output capacitance	C_f	0.022
Switching frequency	f_s	72 pu
Base frequency	f_b	60 Hz
Base power	P_b	1.2 kW



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By using these parameters a comprehensive DC power balance management is simulated as presented in fig. 5. The converter first start operating in CC charging mode, then the four scenarios of the switching is performed with $d \leq 0.5$. Similarly the results can also be validated in CV mode with $d \geq 0.5$. The converter start operating in APBM with $P_b^* = -1pu$, then no PBM, PPBM and again APBM is performed at different intervals. The transition process from CC to CV charging mode is presented in fig. 6. It shows how the duty cycles changes from 0 to 0.5 seconds. . The fig. 6 (b). represents the generated voltage of unit 1 from this we can observe how the voltage fluctuates between 0, v_i and $2v_i$. The converter begins operating in APBM with $P_b^* = -1pu$, from 0 second to 0.17 second. In order to emphasize the features of PPBM, no PBM is performed after the 0.17 second to 0.25 second (under balanced power conditions). PPBM is activated at 0.25 seconds to 0.33 seconds and then the converter is set to operate in APBM with $P_b^* = 1pu$. From 0.33 seconds to 0.5 seconds. Then when the system triggers the control scheme operate under Constant Voltage (CV) charging mode, the same test is simulated once again with $d > 0.5$.

The DC Power Balance Management (PBM) under CC mode ($d \leq 0.5$) is validated through Fig. 6, Fig. 7 and Fig. 8. The total output current reference i_0^* is set to 1pu throughout the test and it can be seen that the total output current i_0 is controlled to its reference i_0^* shown in Fig. 7(a). P_b^* is the reference power which is changed from -1pu to +1pu in order to validate all the operations mode, meanwhile the balance power P_b is regulated to track the reference P_b^* when $d < 0.5$ is shown in Fig. 7(b).

Under PPBM, the total neutral point current i_{np} is zero, hence by decreasing the power and voltage fluctuations at the DC side comparison with no PBM is shown in Fig. 7 (c). From 0 second to 0.15 second $P_b^* = -1$ (where $P_b = P_n - P_p$, here $P_n = 0pu$, $P_p = 1pu$) which represents the imbalance power which is equal to maximum power balancing limit of NPC converter, so that APBM is activated. In order to balance the power ($P_n = P_p$) difference in modulating signal Δd_1 is generated which is also maximum. Finally Δd_1 is added to a duty cycle d_{14} ($d_{14}^* = d + \Delta d_1$) and Δd is subtracted from d_{11} ($d_{11}^* = d - \Delta d_1$).

Duty cycles d_{11}^* and d_{14}^* are lesser than 0.5 ($d \leq 0.5$, CC mode) is shown in the Fig. 8 (a). Difference in duty cycle Δd_1 varies from its minimal value to its maximum in order to generate the maximum balance power as shown in the Fig 8 (b). As the APBM is activated, the power balance control signal Δd_1 is regulated. In order to have a positive average value in the total neutral point current from 0 seconds to 0.17 seconds and a negative average value from 0.33 seconds to 0.5 seconds and when no PBM is performed actively Δd_1 is zero so d_{11} and d_{14} are equal to d_{11}^* and d_{14}^* respectively, as shown in Fig 8 (c).

Currents i_{op1} and i_{on1} are the output of the Unit 1(DC-DC Converter) their magnitude is 0.5pu is shown in Fig. 9 (a). Output currents i_{op2} and i_{on2} are the output of unit 2 (DC-DC Converter) which is equal to 0.5pu as shown in Fig. 9 (b). Magnitude of both unit 1 and unit 2 are equal therefore that the current sharing between the two units is successfully achieved. Each unit has larger output current ripple, leading to the larger total output current ripple. The total output current i_0 is equal to sum of the output currents of both unit 1 and unit 2 is 1pu as shown in Fig. 9 (c).

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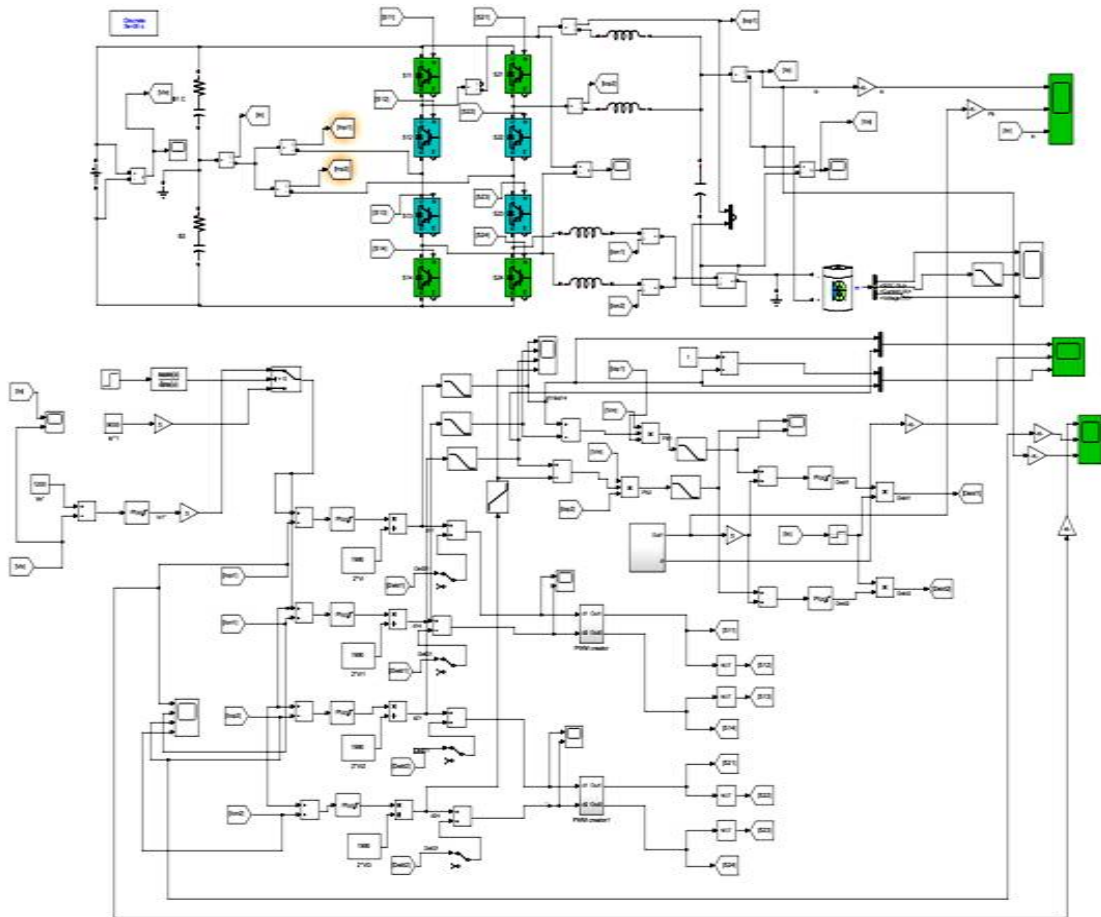


Figure 5. Simulated model of three level DC-DC converter with comprehensive DC power balance management principle.

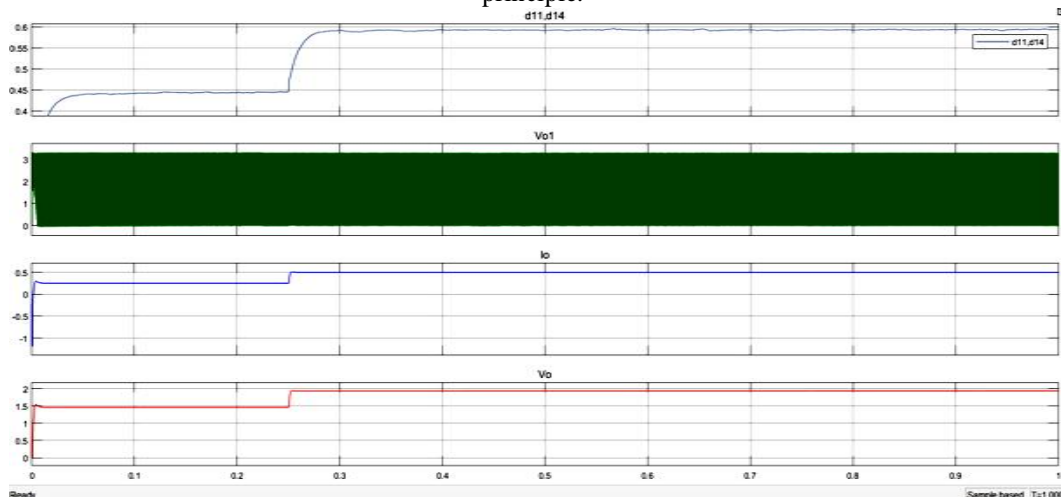


Figure 6. Simulated result for transition from CC to CV mode. (a) Modulation signals d_{11} , d_{14} . (b) Output voltage of unit 1 v_{o1} . (c) Total output current i_o . (d) Output voltage v_o .

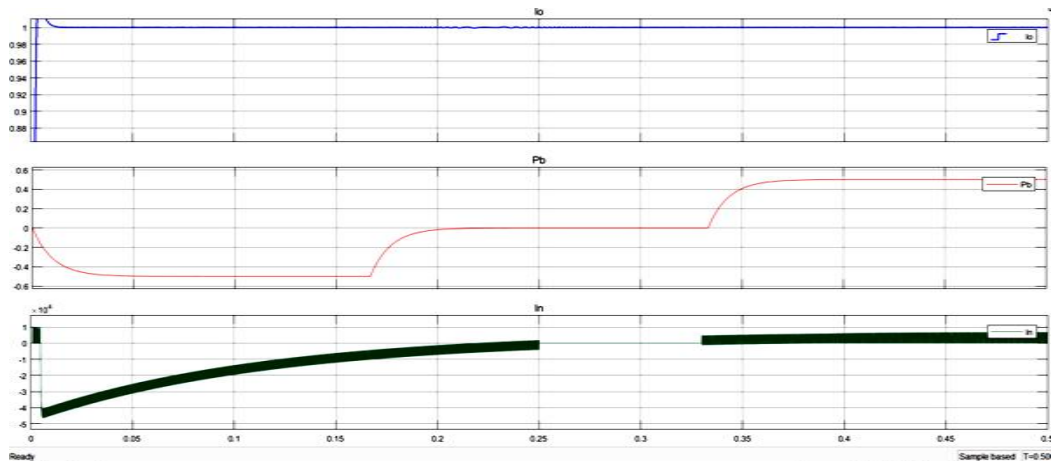


Figure 7. Simulated result of PBM in CC mode for $d \leq 0.5$. (a) Output current i_o , reference current i_o^* . (b) Balance power P_b . (c) Neutral point current i_{np} .

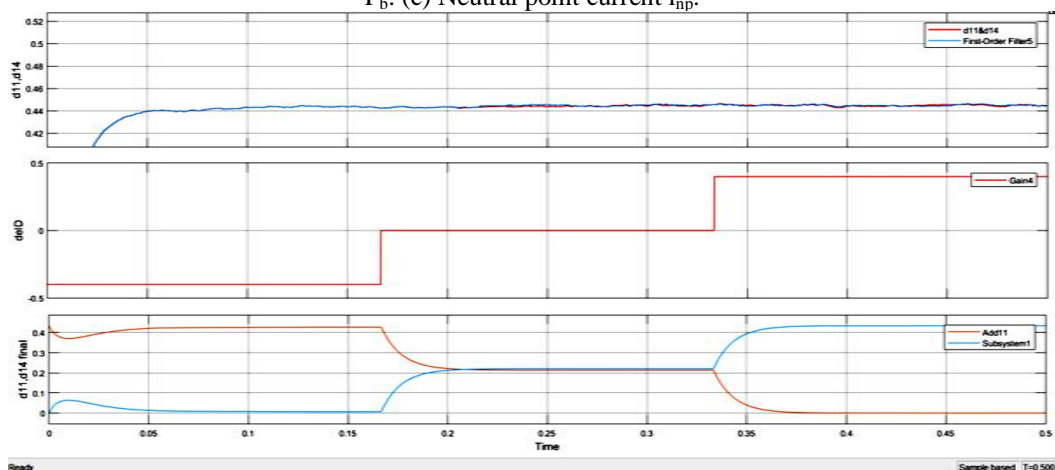


Figure 8. Simulated result of the modulation signals in CC mode, for $d \leq 0.5$. (a) Original modulation signals. (b) Power balance control signal. (c) Final modulation signals d_{11} and d_{14} .

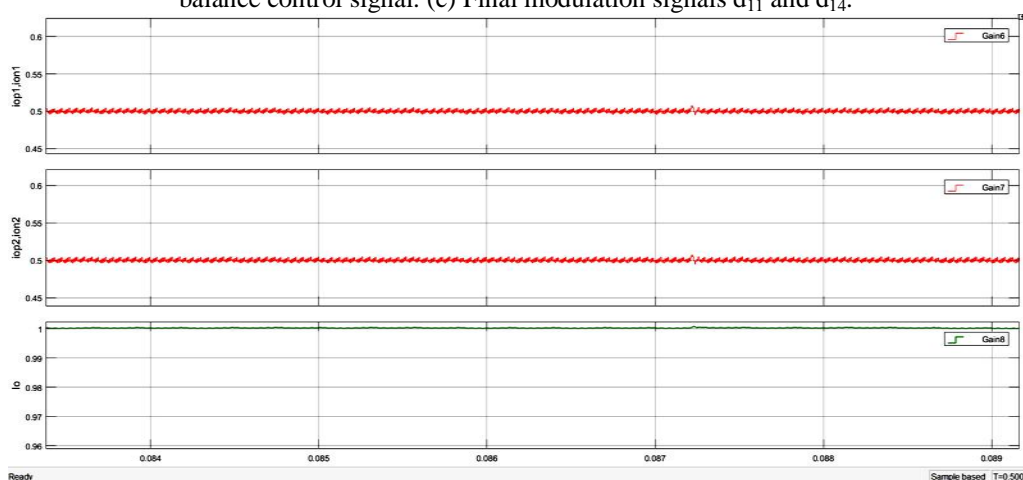


Figure 9. Simulated performances of the output currents in CC mode, for $d \leq 0.5$: (a) Unit 1 output currents i_{op1} and i_{on1} . (b) Unit 2 output currents i_{op2} and i_{on2} . (c) Total output current i_o .



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V. CONCLUSION

The comprehensive DC power balance management principle for the fast charging of electric vehicle is proposed with bipolar DC bus. This fast charger has the dc power balance capability and eliminates the use of additional balancing circuits, need of high frequency transformer. It increases the overall efficiency of the system. This configuration enable the NPC converter to control the grid side fluctuating currents where as the three level DC-DC converter is meant for balancing power. Through simulation results the performance of the proposed fast charger is demonstrated very well in addition to basic function of electric vehicle fast charging.

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