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A DFT Tactic Aimed At Testable Q-Flop Rudiments

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ABSTRACT: In the field of VLSI Design the flip flop elements play an important role in terms of memory management. For registers and memory elements in all the designs either Q flip flop or the D flip flop has its major dominance. Especially the Q-Flop is an alternative memory component for designs that are susceptible to to metastability. This has been noticeably reconnoitered by the former investigation efforts, principally in the schemes of synchronization. But the testing methodologies for these Q flop elements are rarely found and has only few number of support of the insertion of test elements along with it because of its complexity and its perilous nature. The proposed Q flop elements integrate itself to a standard synthesis and scans with automation providing automation solutions in real time. The technique which is built in for testing is one of the approach of DfT. The test results proves the trade offs between the power, area and speed. The circuit design is done using Tanner EDA for computing the design and its code is synthesized for its ability check in Xilinx. The power analysis and area analysis proved to be remarkably better for an automation testing of Q flop elements.

KEYWORDS: Q flop, RTL, FIFO, LSSD, DfT. Metastability.

I.INTRODUCTION

The synchronous standard is the easiest and efficient way of the todays VLSI designers. VLSI design can be done in various levels of abstractions such as gate level, data flow level, behavioral level, switch level. Each level has its uniqueness and will be used by the designers for their prescribed codes. Especially the designers work in the RTL level to omit the delays generating due to the codes. The synchronous design at its best is achieved since it uses global clocking thereby the frequency analysis for the overall design will be helpful. The delay problems arises due to its serial working operation and it can be reduced by adding margins to the clocking system. To achieve this margin in synchronous design, every designer needs to adjust between the parameters of the power, delay, area constraints of VLSI. A perfect tradeoff has to be done by the designer in order to achieve the better result of delay. This tradeoff could be achieved by the RTL design abstraction and synthesis. Many designers prefer for asynchronous paradigm due to this tradeoff problem. One easy way is to use a Globally Asynchronous Locally Synchronous (GALS) [1].

This communication technique will be following the pipelining strategy of any of the types of Synchronous, Asynchronous, and Wave. The synchronous design will be helpful in the concept of pipelining because it uses the protocol of Handshaking. The protocol of handshaking utilizes the duplex way of communication and will be responsible for high safety during the communication between the channels of various frequency domains. Otherwise another way for the approach is the use of wave pipelining were the difference between the maximum and minimum propagation delay will be calculated and it will be utilized for the processing stages of the pipelining. The Q flop element is a register proposed by Rosenberger et al [2] a substitute method for the synchronizers used in GALS. The Q flops behaves same as that of the flip flop and utilizes the same technique of edge triggering. Either positive or negative edge triggering methodology can be utilized for the usage of the Q flop elements. Metastability is a state to persist for an unbounded time in an unstable equilibrium. The state where the elements will be in the forbidden range of low to high or high to low. The Q flop gives solution for the metastability by its internal design feature and will not allow this state to be falling on the output states of the overall block. Thereby the propagation delay can be minimized.

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This metastability free approach aims in integrating the Q flop element to a DfT flow for a scan design model. This could be considered as a EDA tool for verifying the layout designs and make sure that the elemental blocks are functioning in a better way.

II.THE Q FLOP WITH FILTER

The Q flop with metastability filter is depicted in the Fig. 1 [3]. The filter will ensure that the intermediate stages will not arrive at the output states. The uncertainty due to metastability will be available at the output as a variable delay line. The transistor cleans the metastability state by going high only when there is voltage difference between Q and Q'.

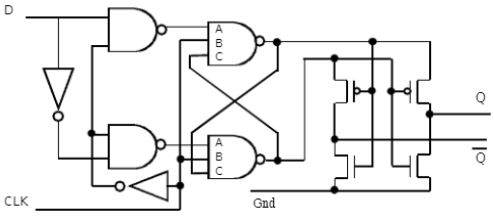

Fig. 1. Q flop with filter

When the CLK input is at low logic 0, then the output of the Q flop will also be at 0. It exhibits a D flip flop behavior at the rising edge of the CLK input. For its register element a pair of cross coupled NAND is used. At logic 1 the output Q will be 0 with nMOS transistor under operation and at logic 0 the output Q will be 1with the help of the pMOS transistor. For Q bar the vice versa operation will be held with the same conditions of logic 1 and logic 0.
The truth table for the above event is depicted in the Fig. 2.

CLK	D	Q	Qbar
0	0	0	0
0	1	0	0
↑	0	0	1
↑	1	1	0

Fig. 2. Truth table

The timing diagram for the operation of the Q flop is shown in the Fig. 3. Where the metastability state will not be arrived at the output. It will be depending on the CLK input 1 and CLK input 0 where the NAND gate design will omit the uncertainty timing at the output.

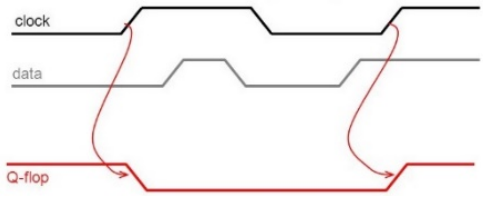

Fig. 3. Timing Diagram of Q flop

The Q flop is divided into two structure having D flip flop as first element and NAND gate as memory element as the second part. diagram for the operation of the Q flop is shown in the Fig. 3. Where the metastability state will not be

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arrived at the output. It will be depending on the CLK input 1 and CLK input 0 where the NAND gate design will omit the uncertainty timing at the output. The split up of the components [5] of rail and NAND gate has better efficiency.

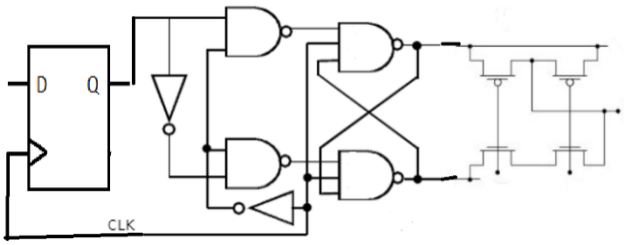

Fig. 4. Q flop proposed structure

The proposed structure for Q flop with register element to eliminate the metastability is shown in the Fig. 4. The filter approach of FIR [4] can also be used as one of the approach for the better design.
The D flip flop used in the architecture can also be replaced with the help of muxed D scan cell for better aligning of the inputs which is based on LSSD [7] test protocol. LSSD is a method which uses separate system and scan clocks to distinguish between normal and test mode. Latches are used in pairs, each has a normal data input, data output and clock for system operation.

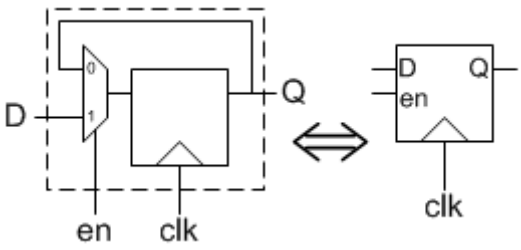

Fig. 5. Muxed D

There will be a violation of reset port when there is too many logic operated with the help of a global clock as we use in the synchronous type of approach. This is removed with the help of the center logic of rail connectivity where it codifies the values to the filter where it avoids the metastability. The rail connectivity techniques are the one which are derived from asynchronous design concepts. Since the proposed idea is going to be a part of automation tool where the testing will be done using a EDA type. The scan chain will play an important role where the number of chain matters for the efficiency of the design. If the flop chain is more automatically the global clock faces a serious issue in clocking the rail connectivity.

III.RESULT AND DISCUSSION

The proposed design of DFT schematic in tanner tool is shown in the Fig. 6. The schematic is drawn and noted for error and its layout is depicted in the Fig. 7. The area for the Q flop is trade off by the usage of the NAND gate as a filter element. The simulation of the design is focused on its area and propagation delay. The propagation delay represents the time required for the output for the changes in its input data. The simulation output shown in the Fig. 8 shows that the rise propagation time gets decreased when it passes on to the 2 input NAND gate and the fall propagation delay will also be similar to that of the rise propagation because the same NAND gate only drives the output. The implemented design also proves to be less power dissipation because it uses only fewer CMOS components. The dynamic power dissipation is low since there is no capacitance effect at the output of the gates. The dynamic power dissipation occurs only when there is a charging and discharging of a capacitor load.

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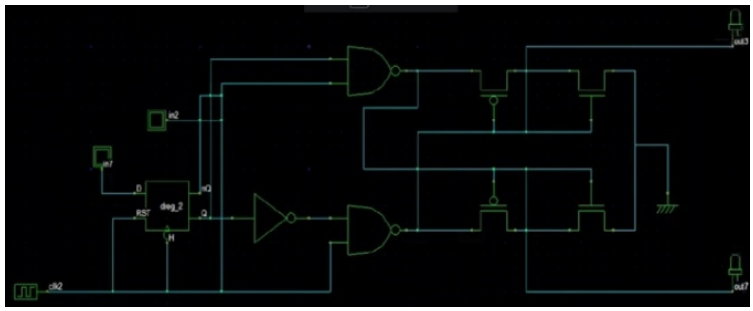

Fig. 6. Q FLOP SCHEMATIC

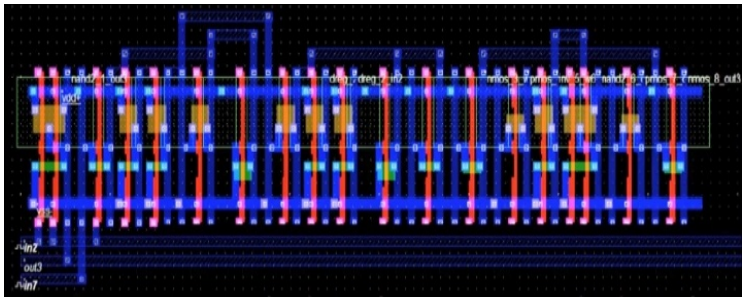

Fig. 7. Q FLOP LAY OUT

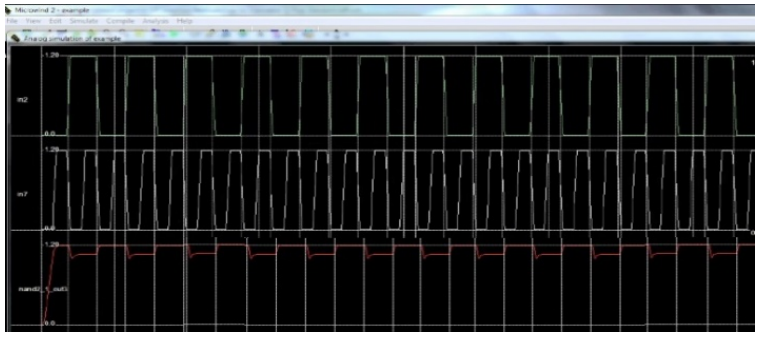

Fig. 8. Q FLOP SIMULATION

VI.CONCLUSION

The proposed methodology integrated the filters with the Q flop registers for the DfT approach. Since it utilized the global clocking the propagation delay got reduced. The area overall got reduced because of fewer CMOS components. Further it can be reduced if we utilize the ratioed circuits like pseudo nMOS concept. The proposed technique helps in better testability for complex circuits since it uses the approach of LSSD. It also ensures the correct circuit behavior of metastability and its logic. The proposed technique can also be developed as a ASIC [6] for better area efficiency.

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