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A Novel Method for Improving the Voltage Quality of Dynamic Loads

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ABSTRACT: This paper deals with improving the voltage quality of sensitive loads from voltage sags using a dynamic voltage restorer (DVR). The higher active power requirement associated with voltage phase jump compensation has caused a substantial rise in size and cost of the dc link energy storage system of DVR. The existing control strategies either mitigate the phase jump or improve the utilization of dc link energy by the following: 1) reducing the amplitude of the injected voltage or 2) optimizing the dc bus energy support. In this paper, an enhanced sag compensation strategy is proposed, which mitigates the phase jump in the load voltage while improving] the overall sag compensation time. An analytical study shows that the proposed method significantly increases the DVR sag support time (more than 50%) compared with the existing phase jump compensation methods. This enhancement can also be seen as a considerable reduction in dc link capacitor size for new installation. The performance of the proposed method is evaluated using simulation study and finally verified experimentally on a scaled laboratory prototype.

KEYWORDS: DVR, Active Power, Phase Jump Compensation

I. INTRODUCTION

In industrial distribution systems, the grid voltage disturbances (voltage sags, swells, flicker, and harmonics) are the most common power quality problems. Sag, being the most frequent voltage disturbance, is typically caused by a fault at the remote bus and is always accompanied by a phase angle jump. The phase jump in the voltage can initiate transient current in the capacitors, transformers, and motor. It can also disturb the operation of commutated converters and may lead to glitch in the performance of thyristor-based loads. It is therefore imperative to protect sensitive loads, especially from the voltage sags with phase jump.

A SCOPE OF THE PROJECT

This paper deals with improving the voltage quality of sensitive loads from voltage sags using a dynamic voltage restorer (DVR)

B EXISTING SYSTEM

The only possible way to mitigate the phase jump is to restore the load voltage to the prefault value. Such an approach is addressed as presag compensation in . However, the phase jump compensation using the presage method requires a significant amount of active power from the dc link capacitor. Thus, this method will require a larger size capacitor or will result

in shorter sag support time. In, an interesting technique is proposed to increase the compensation time while mitigating the voltage phase jump. In this method, once the dc link voltage drops to the threshold limit, the magnitude of the injected voltage is reduced by synchronizing the phase-locked loop (PLL) to the grid voltage. This allows further utilization of the dc link capacitor energy and extends the compensation time by some extent. However, it continues to

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consume the energy in the dc link capacitor throughout the duration of compensation and imposes limitation on compensation time enhancement.

C EXISTING SYSTEMS TECHNIQUE:

The existing control strategies either mitigate the phase jump or improve the utilization of dc link energy by the following: 1) reducing the amplitude of the injected voltage or 2) optimizing the dc bus energy support.

D PROPOSED SYSTEM

This project deals with improving the voltage quality of sensitive loads from voltage sags using a dynamic voltage restorer (DVR). The higher active power requirement associated with voltage phase jump compensation has caused a substantial rise in size and cost of the dc link energy storage system of DVR.

E PROPOSED SYSTEM TECHNIQUE

The work presented in this paper proposes an enhanced sag compensation method to extend the DVR compensation time. It optimizes the gradient of the dc link voltage (dv/dt) by regulating the amount of active power injected by DVR. In the proposed method, the controller restores both phase and amplitude of the load voltage to the presag value and then initiates a transition toward the minimum active power (MAP) mode. The overall operation sequence and implementation of the proposed compensation method is discussed in the following subsections.

F ADVANTAGES OF PROPOSED TECHNIQUE

- Switching losses and harmonics reduced
- High efficiency
- It improves system performance

II. PROJECT DESCRIPTION

To protect sensitive loads from grid voltage sags, custom power devices (such as SVC, D-STATCOM, dynamic voltage restorer (DVR), and UPQC) are being widely used. Among these devices, DVR has emerged as the most cost effective and comprehensive solution. The system configuration of a DVR. It consists of a dc link capacitor (serving as an energy reserve for DVR), a series injection transformer, a six-switch voltage source inverter (VSI), and an *LC* filter for removing switching harmonics from the injected voltage. The primary function of the DVR is to inject a voltage with certain magnitude and phase in series with the upstream source voltage such that the load connected downstream always sees the pure sinusoidal voltage at its terminals.

A MODULE DESCRIPTION

DVR (Dynamic Voltage Restorer) is a static var device that has seen applications in a variety of transmission and distribution systems. It is a series compensation device, which protects sensitive electric load from power quality problems such as voltage sags, swells, unbalance and distortion through power electronic controllers that use voltage source converters (VSC).In normal conditions, the dynamic voltage restorer operates in stand-by mode. However, during disturbances, nominal system voltage will be compared to the voltage variation. This is to get the differential voltage that should be injected by the DVR in order to maintain supply voltage to the load within limits. The amplitude and phase angle of the injected voltages are variable, thereby allowing control of the real and reactive power exchange between the dynamic voltage restorer and the distribution system. The DC input terminal of a DVR is connected to an energy storage device of appropriate capacity. As mentioned, the reactive power exchange between the DVR and the distribution system is internally generated by the DVR without AC passive reactive components. The real power exchanged at the DVR output AC terminals is provided by the DVR input DC terminal by an external energy source or energy storage system.

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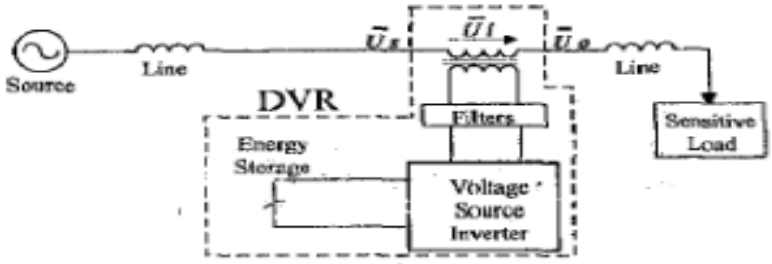
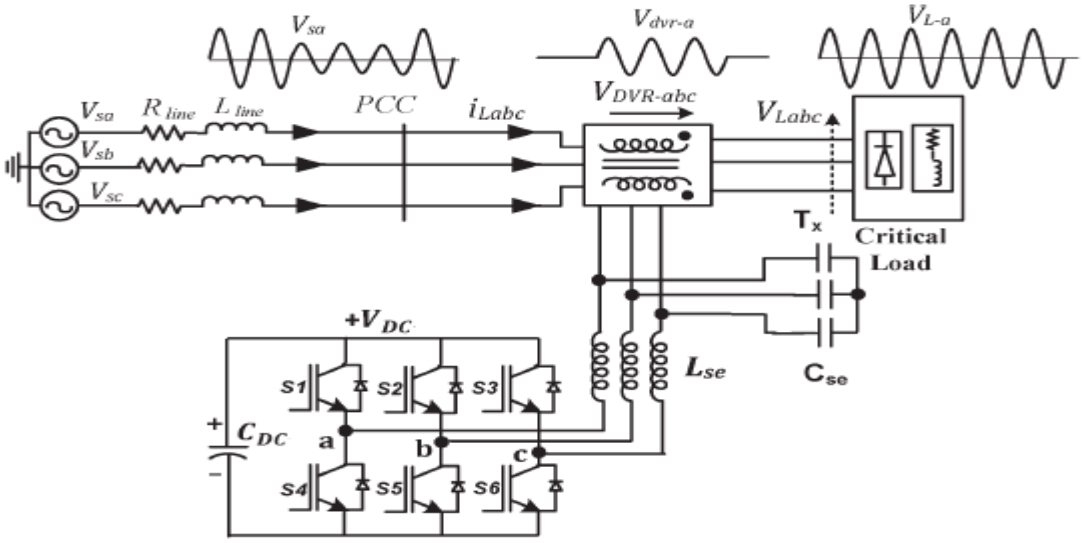


2.1 Block Diagram for Exixting System

Practically, the capability of injection voltage by DVR system is 50% of nominal voltage. This allows DVRs to successfully provide protection against sags to 50% for durations of up to 0.1 seconds. Furthermore, most voltage sags rarely reach less than 50%.
The dynamic voltage restorer is also used to mitigate the damaging effects of voltage swells, voltage unbalance and other waveform distortions.

B CIRCUIT EXPLANATION



2.2 Circuit Diagram for Proposed System

Operation of Proposed Converter

The work presented in this paper proposes an enhanced sag compensation method to extend the DVR compensation time. It optimizes the gradient of the dc link voltage (dv/dt) by regulating the amount of active power injected by DVR. In the proposed method, the controller restores both phase and amplitude of the load voltage to the presag value and then initiates a transition toward the minimum active power (MAP)mode. The overall operation sequence and implementation of the proposed compensation method is discussed in the following subsections.
3 Simulation Results

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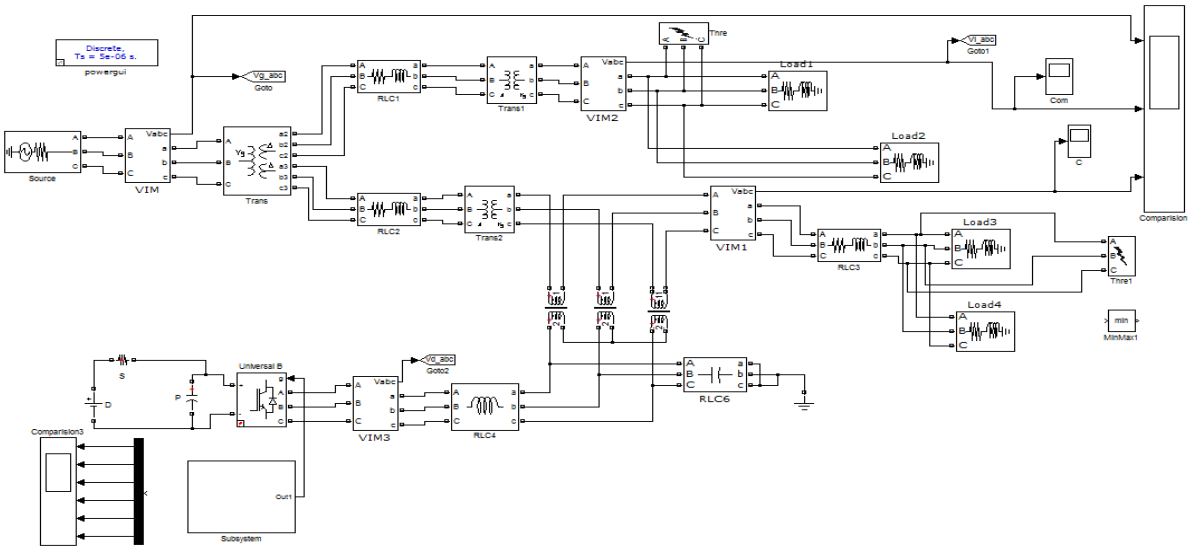
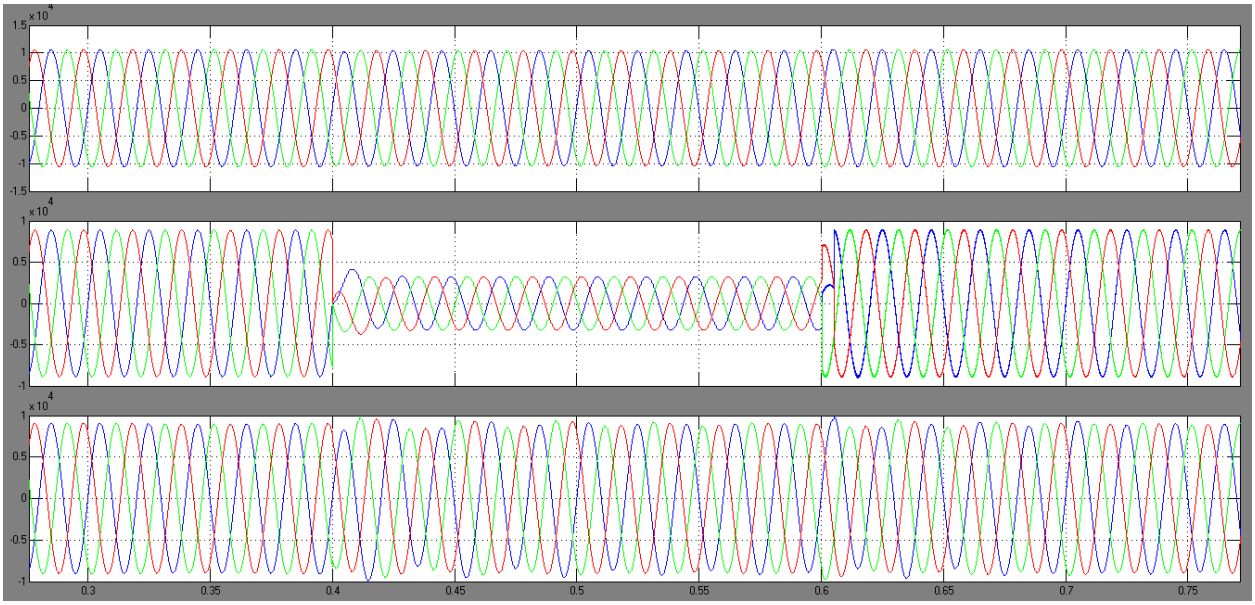


2.3 Simulation Diagram



2.4 Output voltage, Current waveform

III. HARDWARE DESCRIPTION

The hardware system of the proposed converter is implemented using a PIC micro-controller. The software system like Proteus, Mplab, and Micropro is used for the system design for coding the pulses in to the PIC controller. The power supply circuit is designed that will control the PIC and driver circuit to drive the pulses to the MOSFET.

A Microcontroller (sometimes abbreviated µC, uC or MCU) is a small computer on a single integrated circuit containing a processor core, memory, and programmable input/output peripherals. Program memory in the form of NOR flash or OTP ROM is also often included on chip, as well as a typically small amount of RAM. Microcontrollers

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are designed for embedded applications, in contrast to the microprocessors used in personal computers or other general purpose applications.

High-Performance RISC CPU: Only 35 single-word instructions to learn, All single-cycle instructions except for program branches, which are two-cycle, Operating speed: DC – 20 MHz clock input DC – 200 ns instruction cycle, Up to 8K x 14 words of Flash Program Memory, Up to 368 x 8 bytes of Data Memory (RAM), Up to 256 x 8 bytes of EEPROM Data Memory, Pinout compatible to other 28-pin or 40/44-pin PIC16CXXX and PIC16FXXX microcontrollers

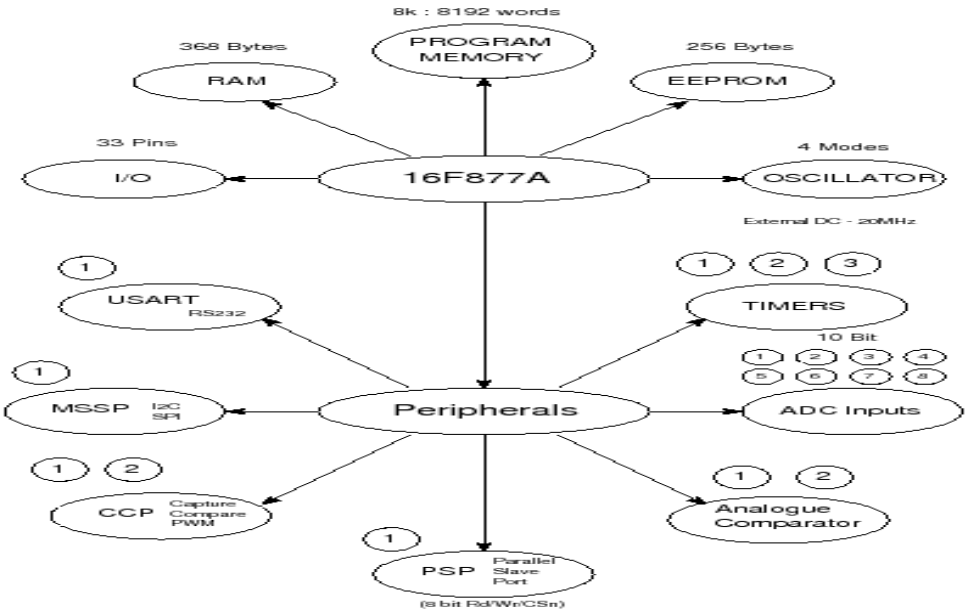

Fig.3.1. Micro-controller Peripherals

Timer0: 8-bit timer/counter with 8-bit pre scalar, Timer1: 16-bit timer/counter with prescaler, can be incremented during Sleep via external crystal/clock, Timer2: 8-bit timer/counter with 8-bit period register, prescaler and postscaler, Two Capture, Compare, PWM modules, Capture is 16-bit max, resolution is 12.5 ns Compare is 16-bit max, resolution is 200 ns, PWM max, resolution is 10-bit Synchronous Serial Port (SSP) with SPI (Master mode) and I2C (Master/Slave), Universal Synchronous Asynchronous Receiver Transmitter (USART/SCI) with 9-bit address detection, Parallel Slave Port (PSP) – 8 bits wide with external RD, WR and CS controls (40/44-pin only), Brown-out detection circuitry for Brown-out Reset (BOR).

CMOS Technology: Low-power, high-speed Flash/EEPROM technology, Fully static design, Wide operating voltage range (2.0V to 5.5V), Commercial and Industrial temperature ranges, Low-power consumption.

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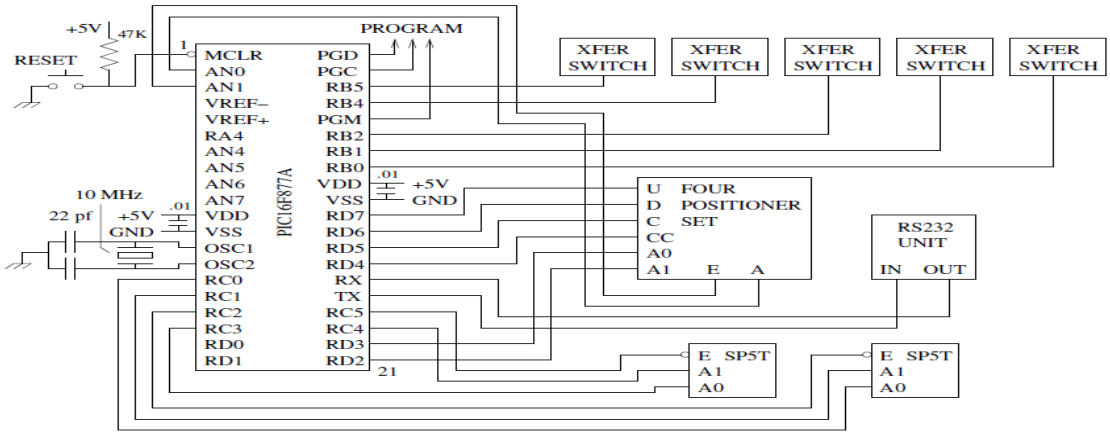

Fig.3.2. Microcontroller PIC16F877A

IV. APPLICATIONS

The dynamic voltage restorer is also used to mitigate the damaging effects of voltage swells, voltage unbalance and other waveform distortions.The application of DVRs would tend to maintain demand even when incipient voltage conditions are present. As a result, this reduces the innate ability to prevent a collapse and increases the chance of cascading interruptions

V FUTURE SCOPE

This converter model will be developed by using matlab simulink soft ware. The efficiency will be improved in future

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