ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 7, Issue 5, May 2018

Design and Simulation of a Standalone Photovoltaic (PV) System with 11 Level Reduced Switch Count Multilevel Inverter

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ABSTRACT: The main objective is to design and simulate a highly compatible standalone photovoltaic (PV) system with 11 level reduced switch count multilevel inverter (MLI) to feed AC load with better power quality. MLI's are becoming eminent because of their high power capability with low harmonic content. Cascaded multilevel inverters are extensively preferred in PV system because it has a distinctive characteristic of employing separate dc sources. The main drawbacks of MLI is its complexity and large number of power devices and passive components. This paper presents topology with reduced no of passive components and power devices for eleven-level inverter. A reduced switch count multilevel inverter is integrated with standalone PV system, which reduces the switching complexity and gate driver circuits without any compromise in the power quality. The PV system with the boost converter assisted by maximum power point tracking (MPPT) algorithm serves as a dc source for each cell of the reduced switch count MLI. To facilitate proper pulse generation and to reduce the harmonic profile multicarrier level shifted pulse width modulation (PWM) is implemented. Simulation results show that total harmonic distortion (THD) of the inverter is less than 4 percent. The proposed system is simulated in MATLAB/Simulink perform.

KEY WORDS:PV Cell, MPPT, Boost converter, Multilevel Inverter, THD

I.INTRODUCTION

In recent past energy demand is highly increased due to Industrialization, Increasing wealth in emerging markets & Globalization. Since the fossil fuels are creating more greenhouse gases, also Global fuel supplies is getting reduced, we go for renewable energy sources. Amidst renewable energy sources photo voltaic power generation is a technology that directly transforms unlimited unpolluted and free solar energy into electric energy. The output power of PV array is dependent on temperature as well as solar radiation or insolation [1]. So with the variation in environmental temperature or insolation, PV power and maximum power point also varies. The non-linear characteristics of PV panel, shading and low insolation do affect the efficiency of a PV array. For tracking of a maximum operating point under a different environmental condition. We use controlled converter with maximum power point tracking algorithm. Ton make it use as standalone it must be converted from DC to AC with highefficiency and less total harmonic distortion. Therefore multilevel inverter can be a good option for this.Recently, multilevel inverter technology has become popular in industry for medium and high voltage applications. Multilevel inverter technology can supplyquality electric power. Multilevel inverter produces staircase output voltage waveform. By increasing number of levels the output voltage waveform approaches near to sine wave improving its quality. As compared to traditional two-level inverter it generates high quality output voltage using low switching frequency with low harmonic distortion. Other merits of this technology are lower switching losses, have more efficiency, and have low voltage stress on power switches, have low

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electromagnetic interference and also low dv/dt stress on load side [1]. Due to these benefits they found wide applications in adjustable speed drives, HVDC, FACTS, wind farms, photovoltaic systems, electric vehicles, etc. Cascaded multilevel inverters are becoming ubiquitous because they have a competent behavior of exploiting individual dc sources and there is no issue in charging the capacitor which is a drawback in flying capacitor topology. For high power applications, the number of levels required is more. The extension of the generalized MLI topology to increase the number of levels will involve more number of switches which in turn increases the complexity of the system with more number of gate driver circuits. The cascaded H bridge MLI with reduced switches is suitably connected with renewable energy mainly Solar PV system.

II.PROPOSED SYSTEM

In this system the PV source with dc-dc converter assisted by maximum power point tracking (MPPT) technique acts as a source for each cell of the reduced switch count MLI. The dc power is pumped to the load using reduced switch count multilevel inverter. The duty cycle of the converter is varied to operate the PV array at its maximum power point (MPP). In this application boost converter is used for interfacing the PV with each cell of the multilevel inverter. Perturb and Observe (P&O) MPPT algorithm is used to track the MPP because it is a reliable MPPT which can be effortlessly executed in both analog and digital environment. Periodic tuning of the system is not required. The P&O method follows and holds the MPP by perturbing, observing and analyzing the power generated from the PV array using iteration. The block diagram of the stand-alone solar PV system is shown in figure1.

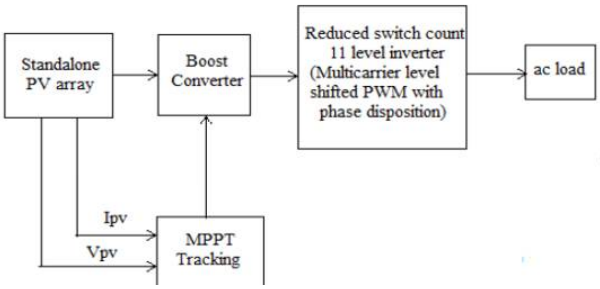

Fig 1 Block Diagram of standalone photovoltaic (PV) system with reduced switch count multilevel inverter (MLI)

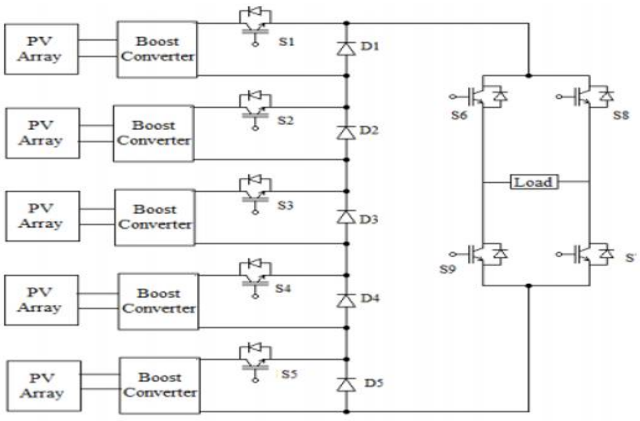

Fig 2Schematic diagram of the proposed system – PV Array with Boost Converter and reduced switch count Cascaded MLI

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III.SOLAR PV ARRAY

The proportional single diode model of a viable PV cell is shown in figure 3. It is also termed as five parameter model (n, Rsh, Rs, Io, Iph).RS is acquainted as with consider the voltagedrops and inward misfortunes in because of stream of current. Rsh takes into record the spillage current to the ground when diode is backward one-sided. 05 Nos. of PV Arrays are connected directly to the input of each Boost converter through MPPT algorithm in the proposed system.

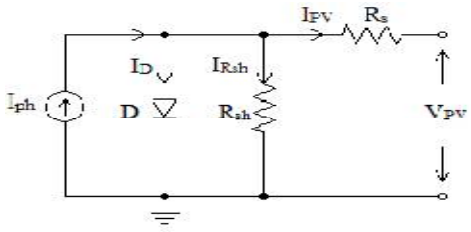

Fig 3 Single diode model of PV

Where,
R_S is series resistance
R_{sh} is parallel resistance
n is ideality factor of diode
I_{ph} is photon current which is directly proportional to solar insolation
ID is diode current

A. PV PANEL SPECIFICATION

DESCRIPTION	RATING
Rated peak power	37.0 W
Voltage at maximum power (V_{mp})	16.56 V
Current at maximum power (I_{mp})	2.25 A
Open circuit voltage (V_{oc})	21.24 V
Short circuit current (I_{sc})	2.5 A
Total number of cells in series	36
Total number of cells in parallel	1

Table 1 PV Panel Specification

The PV output current (I_{pv}) is given by

$$I_{pv} = N_p \times I_{ph} - N_p \times I_o \left[exp\left\{ \frac{q \times (V_{pv} + I_{pv} R_s}{N_s A k T} \right\} - 1 \right]$$

Where,
I_{pv} and V_{pv} are current and voltage of the PV module.
Rs and Rsh are the series and shunt resistance of PV module.
Np and Ns denote the number of cells in parallel and series.
k is the Boltzmann constant (1.3805×10-23J/K).
T is the temperature
A is the ideality factor (1.6).

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q is the charge of an electron(1.6×10-19 C)

B. BOOST CONVERTER

The dc-dc converter acts as a key component of a standalone PV system. Boost converter is used for interfacing the PV with each cell of the multilevel inverter. The duty cycle of the converter is varied to operate the PV array at its maximum power point (MPP). The boosted voltage of the boost converter acts as a source for each cell in reduced switch count MLI.

BOOST CONVERTER DESIGN

Mv = Vo/Vs = 1/(1-D)

$$L_C = \frac{RD(1-D)^2}{2f_S} \quad C_C \geq \frac{V_O \times D}{f_S \times V_r \times R}$$

Where
D = Duty Cycle
Vo = Output Voltage
Vs = Input Voltage
Fs = Switching Frequency
R = Value of resistance
Vr = Output voltage ripple

C. MPPT (MAXIMUM POWER POINT TRACKER)

Climatic change has an impact on temperature and irradiation which has its effect on open circuit voltage and short circuit current of PV. Hence MPPT is used to follow and hold the maximum power even with wide variation in temperature, irradiation and varying load. Power electronic dc-dc converters are assisted by MPPT to follow and hold the maximum power. Buck-Boost converter is employed as dc-dc converter.

D. PERTRUP & OBSERVE ALGORITHM

Perturb and observe (P&O) methodis mostly used out of other method as it is simple and less expensive. This algorithm is based on the sign of slope of P-V curve of solar module. In this algorithm voltage is perturbed and slope (dP/dV) is checked weather it is positive, negative or zero. If the slope is zero, then that point is MPP and if slope is negative then voltage is perturbed in reverse direction else voltage perturbation is continued in same direction until we reach peak point.

E. MLI TOPOLOGY

The boosted voltage of the boost converter acts as a source for each cell in reduced switch count MLI. The reduced switch count multilevel inverter topology is a modification of cascaded half bridge multilevel inverter which utilizes all the advantages of cascaded MLI. To facilitate proper pulse generation pattern for reduced switch count multilevel inverter multicarrier level shifted pulse width modulation (PWM) with phase disposition is implemented. The 11 level inverter topology is shown in Fig. 4.

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Vol. 7, Issue 5, May 2018

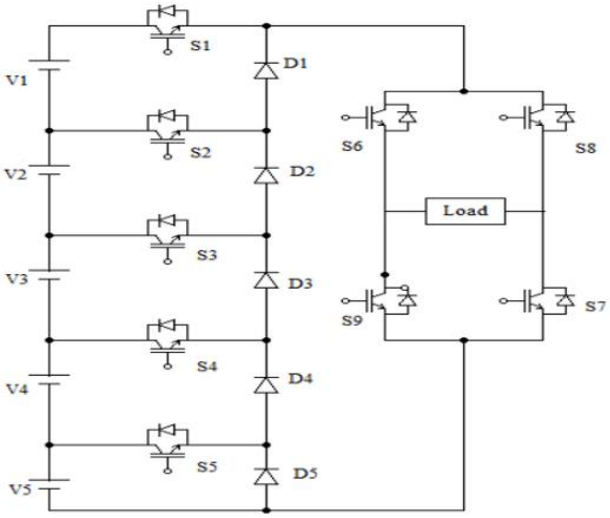

Fig 4Schematic diagram of reduced switch count MLI

F. WORKING

Each cell has its own dc source with a control switch (IGBT) and uncontrolled switch (diode). The symmetrical configuration of the topology is made use for this application. Therefore V1=V2=V3=V4=V3=Vdc which implies the voltage sources in all the cells are equal. The waveform generation is segregated into two parts; level generation part and polarity generation part. The switches S1, S2, S3, S4, and S5 are used in level generation part and they operate at high switching frequency. Switches S6, S7, S8, and S9 in the H Bridge are used in polarity generation part, operating at fundamental switching frequency. Table 2 shows the pattern in which the switches are triggered to produce the desired voltage level and Table 3 shows the switching of full H bridge inverter.

Voltage level	S_1	S_2	S_3	S_4	S_5
0	0	0	0	0	0
V_1	1	0	0	0	0
V_1+V_2	1	1	0	0	0
$V_1+V_2+V_3$	1	1	1	0	0
$V_1+V_2+V_3+V_4$	1	1	1	1	0
$V_1+V_2+V_3+V_4+V_5$	1	1	1	1	1

Table 2 Switching table for redused swith count inverter

Voltage level	S_6	S_7	S_8	S_9
V_{dc}	1	1	0	0
0	0	0	0	0
$-V_{dc}$	0	0	1	1

Table 3 Switching table for H Bridge Inverter

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G. COMPARISON OF PROPOSED 11 LEVEL REDUCED SWITCH COUNT CASCADED MULTI LEVEL INVERTER

SL. NO.	TOPOLOGY	DIODE CLAMPED	FLYING CAPACITOR	CASCADED	**OUR PROPOSED REDUSED SWITHCOUNT MLI**
01	Power Semiconductor Switches	2(m-1)	2(m-1)	2(m-1)	**(m-1)/2 + 4**
		20 nos	20 nos	20 nos	**9 Nos**
02	Clamping Diodes per phase	(m-1)(m-2)	0	0	**5 nos**
		90 nos			
03	DC Bus Capacitors	(m-1)	(m-1)	(m-1)2	**5 PV arrays I/P**
		10 nos	10 nos	5 nos	
04	Balancing Capacitors per phase	0	(m-1)(m-2)/2	0	**0**
			45 nos		
05	Voltage Unbalancing	Average	High	Very Small	**Very Very Small**

Table 4Comparison of proposed 11 level reduced switch count cascaded multi-level inverter.

From the above table it is revealed that the same conventional cascaded 11 step Multilevel Inverter requires 20 switches, whereas our proposed reduced cascaded 11 step Multilevel Inverter requires only 09 switches.

H. PULSE GENERATION (PULSE GENERATION)

The multilevel inverter implements multicarrier level shifted PWM with phase disposition for pulse generation. Thescheme of multicarrier level shifted PWM is shown in Fig. 5.

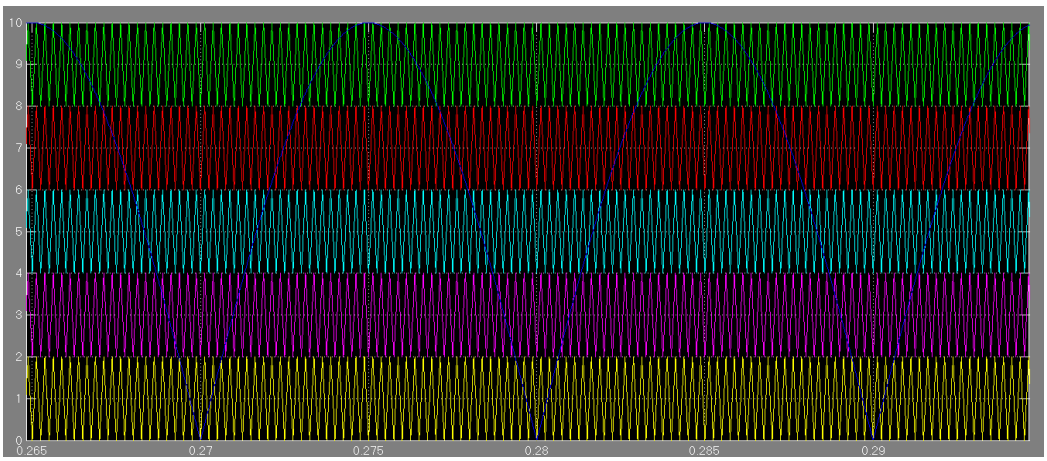

Fig 5 Multicarrier level shifted PWM with phase disposition for pulse generation

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IV.SIMULATION AND RESULTS

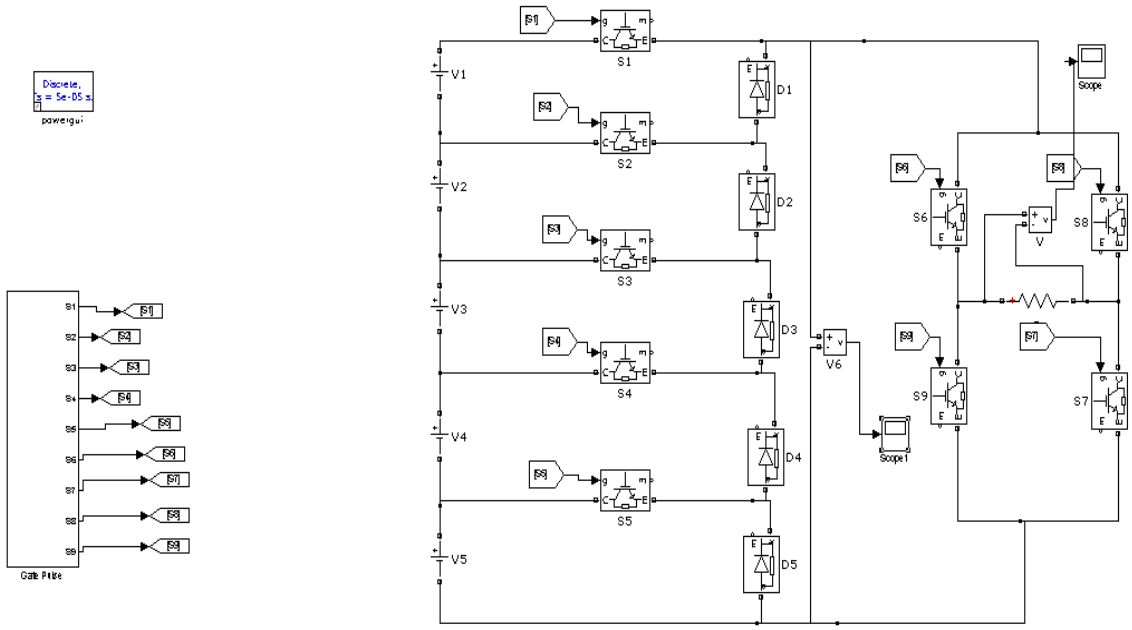

Fig6 Simulation Circuit of 11 Level Reduced Switch Count Cascaded Multi Level Inverter without Filter

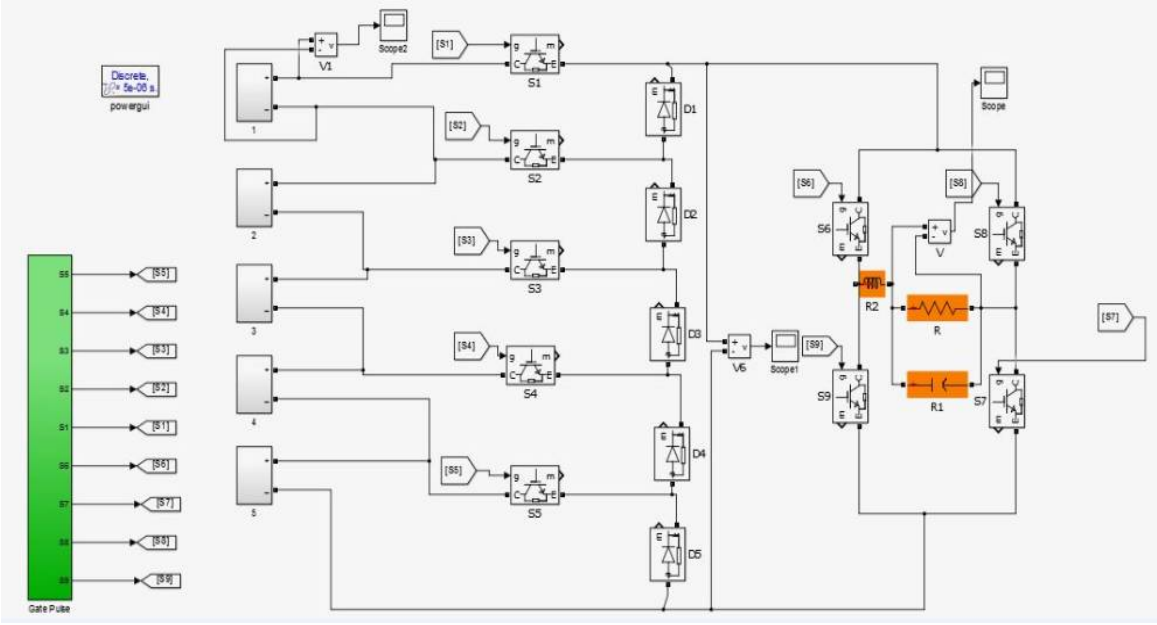

Fig7 Simulation Circuit of 11 Level Reduced Switch Count Cascaded Multi Level Inverter with Filter

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A.OUTPUT VOLTAGE WITHOUT FILTER

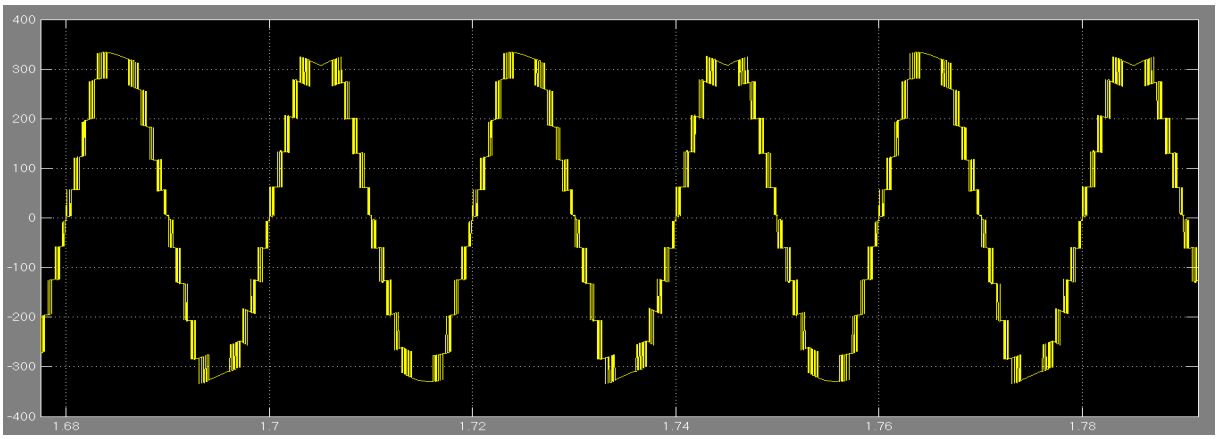

Fig 8 Output Voltage Without Filter

B.THD VALUE WITHOUT FILTER

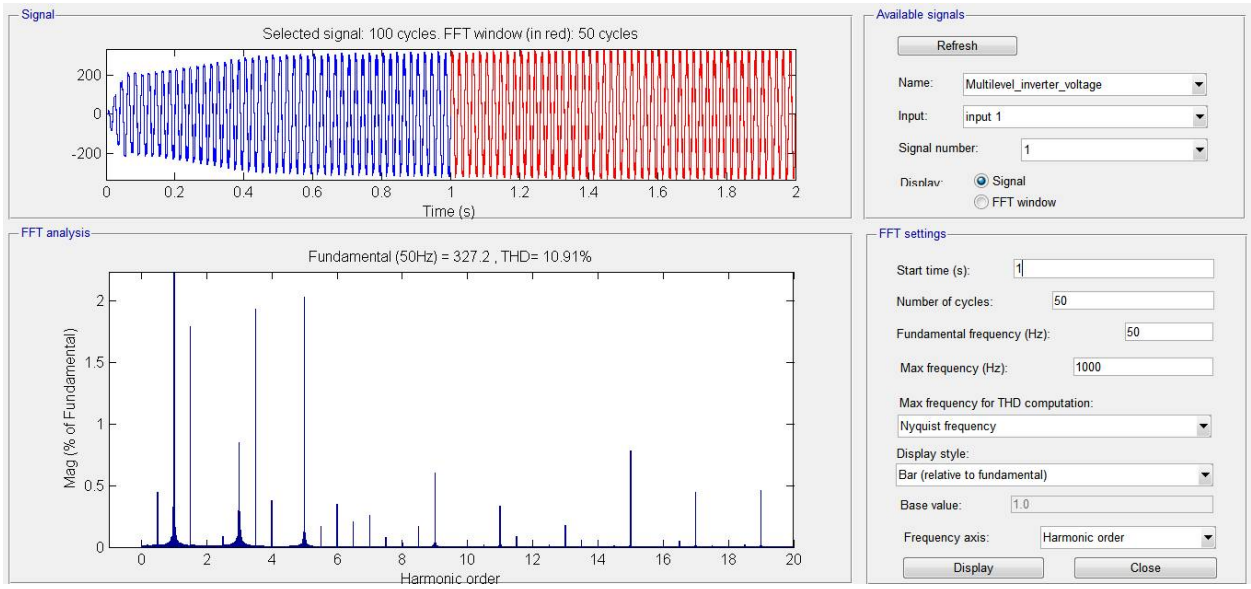

Fig 9THD Value Without Filter

The output voltage of the system without filter is shown inFig. 8 and its THD analysis is shown in Fig. 9. It isobservedthat THD before filter is 10.91%.

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C. OUTPUT VOLTAGE WITH FILTER

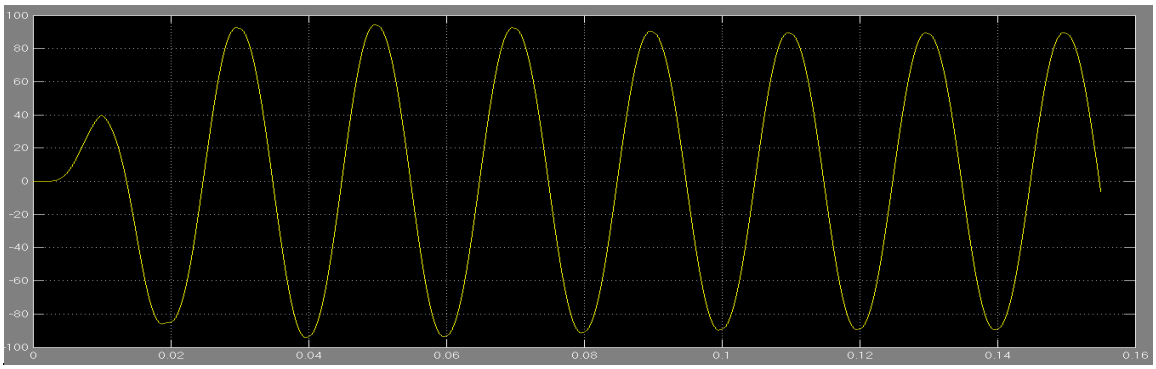

Fig 10Output Voltage with Filter

D.THD VALUE WITH FILTER

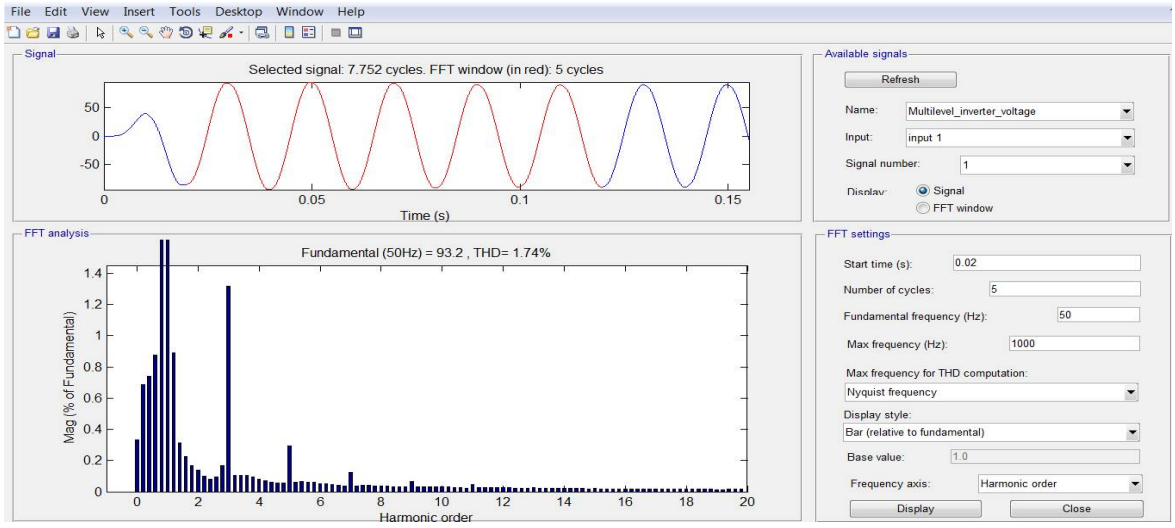

Fig11THD Value with Filter

The system is designed with output LC filter to reduce the harmonics. The sinusoidal output voltage waveform after filter is shown in Fig.10 and the THD analysis is depicted in Fig.11. The THD of the system is observed to be less than 4%.

E.COMPARISON OF THD ANALYSIS

DESCRIPTION	WITHOUT FILTER	WITH FILTER
Reduced switch count multilevel (11 level) inverter	10.91%	1.74%

Table 5Comparison of THD analysis.

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V. CONCLUSION

A standalone photovoltaic system is designed and simulated with a highly compatible reduced switch count multilevel inverter. Multicarrier level shifted pulse width modulation is employed as the control strategy. The boost converter not only assists in MPPT tracking but also steps up the lower voltage from PV to higher voltage for each cell of the inverter. Simulation results show that the THD of the system is less than 4%.

REFERENCES

[1] Aparna Prayag and Sanjay Bodkhe "Novel Basic Block of Multilevel Inverter Using Reduced Number of On-State Switches and Cascaded Circuit Topology" Advances in in Electrical Engineering Volume 2017 (2017), Article ID 5640926, 16 pages.
[2] H.A. Guda, U.O Aliyu., "Design of Standalone for a photovoltaic system in bauchi", International journal of engineering and technology, vol.5, ISSN 2049- 444, No1. Jan.2015.
[3] NatarajanPandiarajan, RamabadranRamaprabha and Ranganathmuthu "Application of circuit model for photovoltaic energy conversion system" International journal of photoenergy, Hindawi Publishing Corporation, vol 2012, 410401.
[4] Md. SifatMorshed, Shoaib Mohammed Ankon, Md.TanzilHoqueChowdhury, Md. AnikurRahman, "Design of a 2 kW Standalone PV system in Bangladesh using PV syst, Homer and solar MAT" in Proc. IEEE, ICGET, 2015, pp.1-6.
[5] Hani Vahedi, Kamal AL-Haddad," Single DC source 7 level CHB inverter with multicarrier level shifted PWM", IECON, pp.004328-004333,2015.
[6] S. Malathy, R. Ramaprabha, "A new single phase multilevel inverter topology with reduced number of switches" in Proc. IEEE, ICEES, 2016, pp.139-144.
[7] M.F.Kangarlu. and E.Babaei, "A generalized cascaded multilevel inverter using series connection of sub multilevel inverters", IEEE Trans. Power Electron., vol.28, no.2, pp-625-636, Feb.2013.
[8] Krishna kumargupta, AlekhRanjan, PallaviBhatnagar, Lalit Kumar Sahu, Shailaendra Jain, "Multilevel inverter topologies with reduced switch count: A review", IEEE Trans. Power Electron., vol.31, no.1.pp 135-151, Jan 2016.
[9] DebashishaJena,VanjariVenkataRamana, "Modelling of Photovoltaic System for uniform and non-uniform irradiance: A critical review", Renewable and sustainable energy reviews 52,Elsevier Ltd, pp.400-417,2015.
[10] K. Praveen Kumar, D.S. Purushothaman, "Implementation of modified sepic converter for standalone PV applications", International journal of advanced research in Electrical Electronics and Instrumentation Engineering, vol.5, Mar 2016.
[11] NagarajaRao. S, Ashok Kumar. D.V, Ch. SaiBabu, "New Multilevel inverter topology with reduced number of switches using advanced modulation strategies", International Conference on Power energy and Control (ICPEC), 2013.
[12] J.Ebrahimi, E. Babaei and G.B. Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components," IEEE Trans. Ind. Electron, vol. 59, no.2, pp.655-667, Feb.2012.
[13] I.Clak, E.Kabalci and R.Bayandir, "Review of multilevel inverter topologies and control schemes", Energy Convers. Manage.,52(@).1114-1128.2011.