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Fault Location with Using Window Least Square Method

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ABSTRACT: DC fault current is contributed by various distributed energy resources in dc distribution systems. The tightly coupled dc distribution systems have relatively low line impedance values. The fault current increases fast because of the low impedance. Some converters in dc distribution systems include fault current limiting function. The controlled fault currents at different locations are very close. Thus, it is important to design a reliable and fast fault detection and location method for dc distribution systems. This paper proposes a novel local measurement-based fault location algorithm for tightly coupled dc distribution systems. The proposed fault location algorithm can estimate the equivalent inductance between a protective device and a fault in less than 1 ms.The performance of the developed protection algorithm was validated by numerical simulation and hardware tests.

KEYWORDS: Impedance, simulation, novel**.**

I. INTRODUCTION

The Emerging power electronic technologies improve the developments of dc power systems. Examples of dc distribution systems include industrial systems, renewable energy collection systems, shipboard power systems, data centers, building systems, etc. DC distribution systems may interface with ac power systems and exchange energy with bulk power systems. When a dc fault occurs, fault current contributions will be from utility grid, distributed generators, distributed capacitor energy storages, active loads, etc. A fault current can be estimated with the equivalent resistance, inductance, and capacitance of a fault path [1], [2]. The circuit impedances in most dc distribution systems are very low in comparison to ac systems. The dc fault current thus rises very rapidly. DC protective devices, such as dc circuit breakers, are required to isolate dc faults in a timely and reliable way. The converter-interfaced energy resources and loads are distributed system wide in dc distribution systems. The short-circuit fault current may reach tens of thousands ofamperes without any protection. Sustained large fault currents in converter-based dc systems are not allowed due to the electrical and physical limits of power electronic switches. When a dc fault occurs, some converters (such as thyristor rectifiers, dc/dc converters, full-bridge multilevel modular converters, and clamp double converters) will limit the fault current to 1.5 times of the nominal current to protect power electronic devices. It becomes difficult to discriminate faults in dc distribution systems once fault currents are limited. Thus, it is a challenge to locate dc faults and coordinate protective devices timely in dc distribution systems. Different fault detection, location, and coordination methods can be used for dc protection [3]–[10]. Recently, impedance- based protection methods were proposed as effective alternative methods to protect dc distribution systems [11]–[13]. The methods use capacitor discharge to locate a fault. An online inductance-based fault location method for dc distribution systems was proposed in [11]. The line inductance between a large capacitor and a fault is estimated using the capacitor voltage and the line current at the initial stage of the capacitor discharging. This method requires a large enough capacitor at the measurement point to locate a fault. An impedance-based fault location apparatus was developed in [12] and [13]. The discharging cur- rent from a capacitor, in the offline apparatus, is injected into an isolated fault segment. The frequency of the capacitor discharging. Current is used to locate the fault. However, this method is not designed for online applications because the capacitor in this apparatus is required to discharge on a de-energized network.

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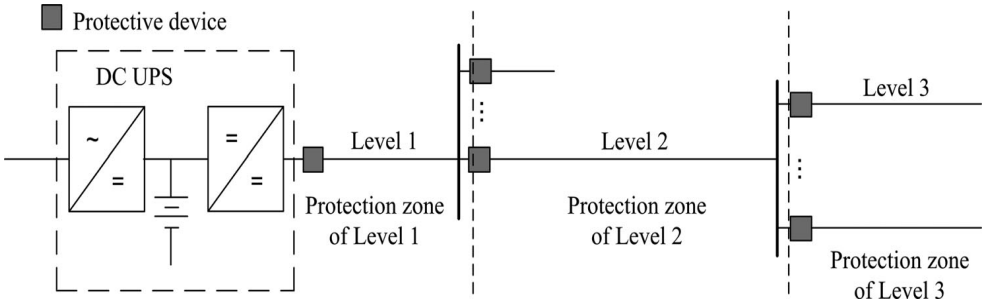

Fig 1.

II. PROBLEM STATEMENT

The one-line-diagram of a dc distribution system is shown in Fig. 1. The system includes a specific ac/dc uninterruptible power supply (UPS), lines, loads, and protective devices (such as circuit breakers). Even though the dc/dc converter in this algorithm has been validated in a hardware- in-the-loop simulation environment [14]. The main contribution of this work is the validation of the novel local measurement- based fault location algorithm in a hardware testbed. The technical work has been previously presented in [15].UPS has a fault current limiter to limit the averaged current from up- stream sources to a predefined low current value, the discharging current of the UPS output capacitor is uncontrollable. The capacitor discharging current is the predominant fault current and is high enough to damage devices or equipment. Due to low impedance values in tightly coupled systems, the fault current can reach its peak value within 1 ms. with this quickly developed dc fault current, it is vital for protective devices to interrupt the fault current timely to avoid any damage to equipment and to minimize the impact of the fault. The total dc protection response time *t* can be estimated by (1). It consists of fault detection time *t*, fault location time communication time and device turning- off time *t*.

$$t = t\text{detection} + l\text{ocation} + c\text{omm.} + t\text{prot.}$$

To avoid the communication delay, local measurement-based protection methods are preferred. Fast fault detection and location becomes an essential requirement for fast protective devices. Each protective device measures local electrical variables. A local controller is embedded with each protective device to implement the fast fault detection and location algorithm. The algorithm differentiates internal faults and external faults for each protection zone. The protection controller sends tripping commands to the protective device. The estimated distance to fault will be used to achieve protection coordination without any communication between protective devices. This method does not require any communication to achieve coordination, and thus, the fault location and isolation time can be minimized. The pro-posed fault location

III. NOVEL DC FAULT LICATION METHOD

When a fault occurs, the dc system experiences a transient period in the first few milliseconds. The proposed method uses the information of theTransient stage to locate the fault. The equivalent inductance from a protective device to a fault is estimate using local signals. The reason to use the inductance instead of the resistance is that the fault resistance is normally unknown. However the unknown fault resistance may notaffect the inductance calculation result. When a fault occurs as shown in Fig. 1, the fault current limiting (FCL) function in the UPS takes action. In practical applications, due to the communication delay and the FCL control delay, the fault currents from upstream resources

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normally are uncontrolled for a few milliseconds before limited to a constant value. The transient voltage, current, and *di*/*dt*signals are measured at each protective device. The measured signals are used to

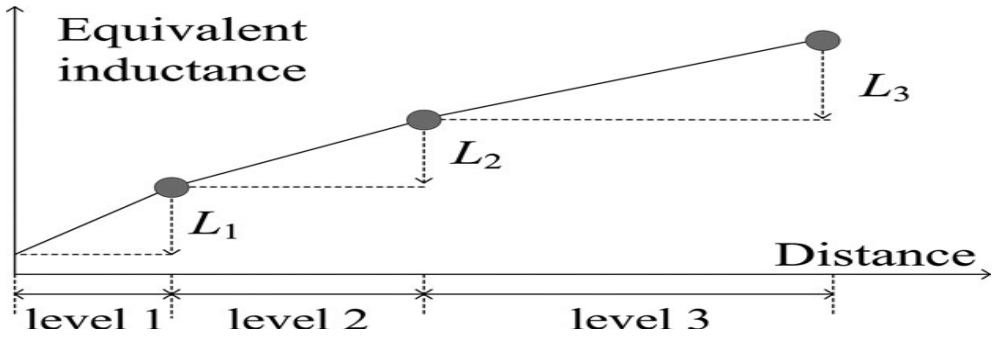

Fig.2 Equivalent inductances in levels 1–3.

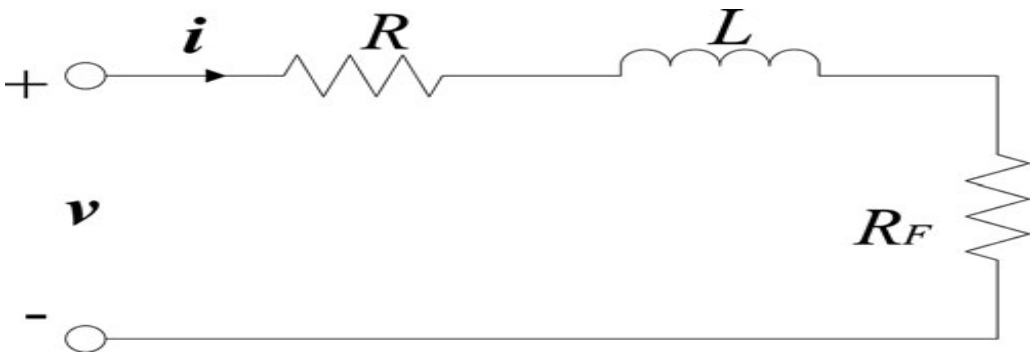

Fig.3 Equivalent circuit used in the equivalent inductance estimation.

Estimate the equivalent fault inductance between the local protective device and the fault. The inductance distribution in levels 1–3 of the system is illustrated in Fig. 2. L_1, L_2, and L_3 represent the equivalent inductances of levels 1–3. If the estimated inductance is less than the known line inductance, the fault is considered as an internal fault. The local protective device will open to isolate the faulted segments and the healthy part will go back to normal operation.To estimate the equivalent inductance between a protective device and a fault, an equivalent electric circuit is used.
as shown in Fig. 3. Circuit parameters L and R represent the equivalent inductance and resistance between the protective device and the fault. $R_F$is the fault resistance. The state-space equation of the circuit is expressed as

$$V = L\frac{di}{dt} + (R + R_F)i$$

The voltage, current, and d*i*/d*t* are sampled at various time steps. (R + R_F) and L are estimated from the data samples. At multiple time instants using the least-squares method. The relationship of the sampled data is shown in Fig.6 Where, N is the sampling index. The sampling rate can be chosen as 20–100 μs depending on the transient behavior of the system. Using the least-squares method, the unknown parameters are estimated as to improve the estimationaccuracy, an online moving- window least-squares method [16] is implemented to identify the equivalent inductance. The inductance estimation

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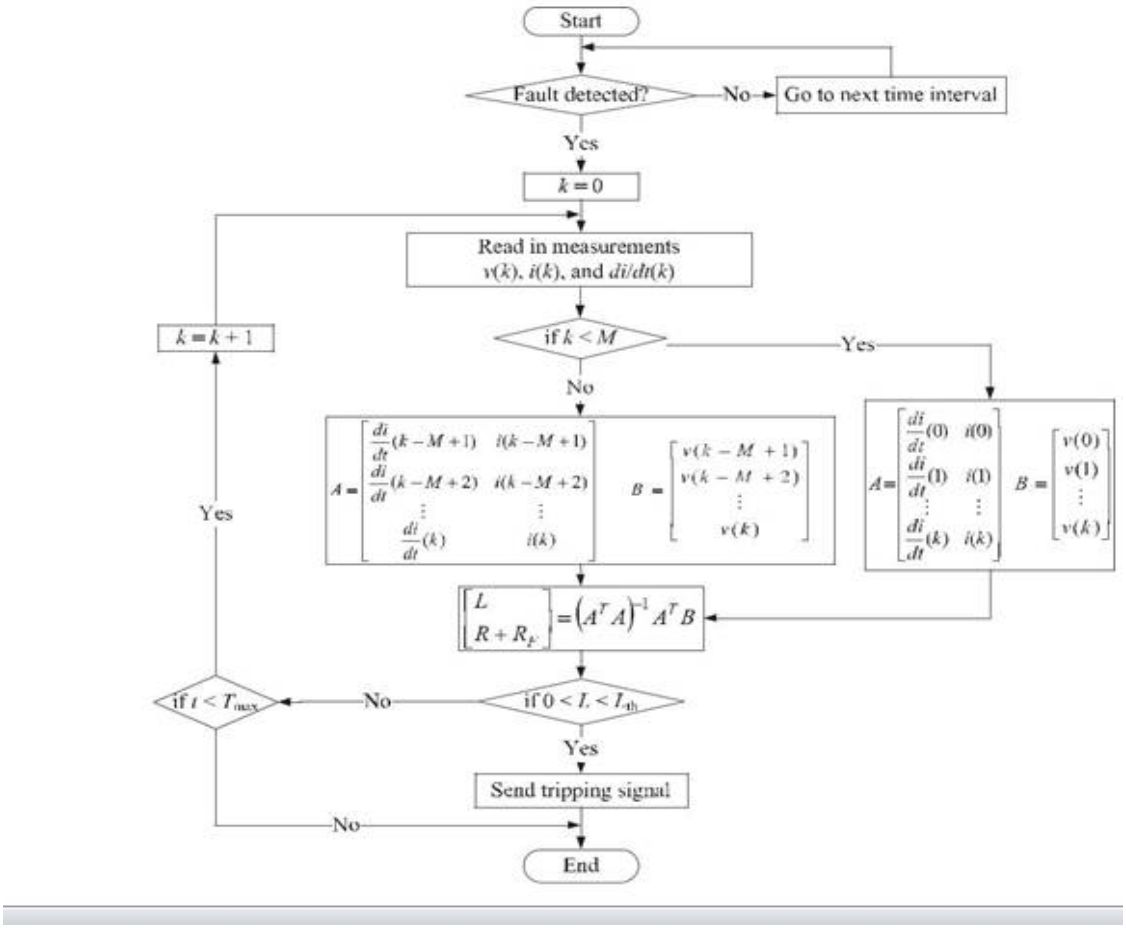

Fig .4 Flowchart of the proposed fault location algorithm

flowchart is shown in Fig. 4. Once a fault is detected by over current and/or under voltage, the fault location routine is activated.

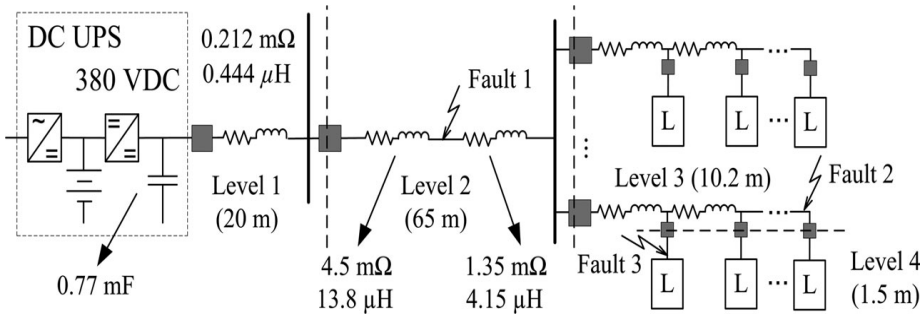

Fig.5 Simulation diagram of an LVDC distribution system

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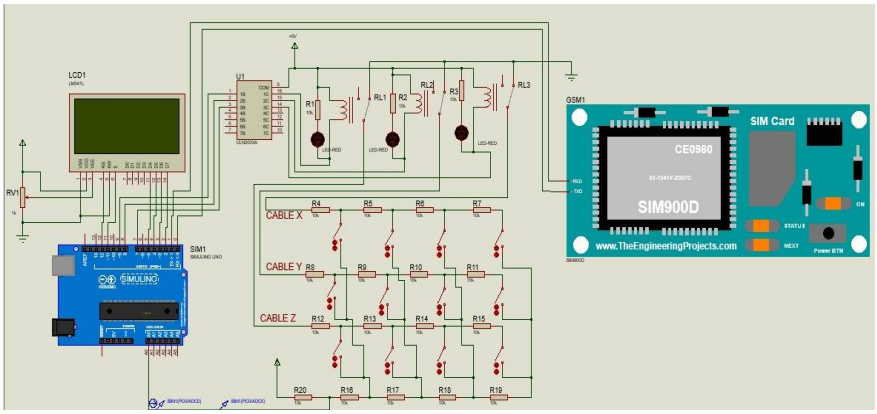

Fig.6 Hardware setup

The measured voltage, current, and d*i*/d*t* signals at different time instants are used to estimate the equivalent inductance. If data samples are less than *M* (*M* is the size of the moving window of the least square method), all the data are used in the inductance samples are less than *M* (*M* is the size of the moving window of the least square method), all the data are used in the inductance.

IV.NUMERICAL SIMULATION

In this section, numerical simulation is used to validate the proposed fault location algorithm. A low voltage dc (LVDC) distribution system is simulated in MATLAB/Sim Power System with a step size of 5 μs. The simulated LVDC system is shown in Fig. 5. The UPS rating is 100 kW and the output voltage is 380 V dc. The converter in the UPS has a fault current limiter. Once

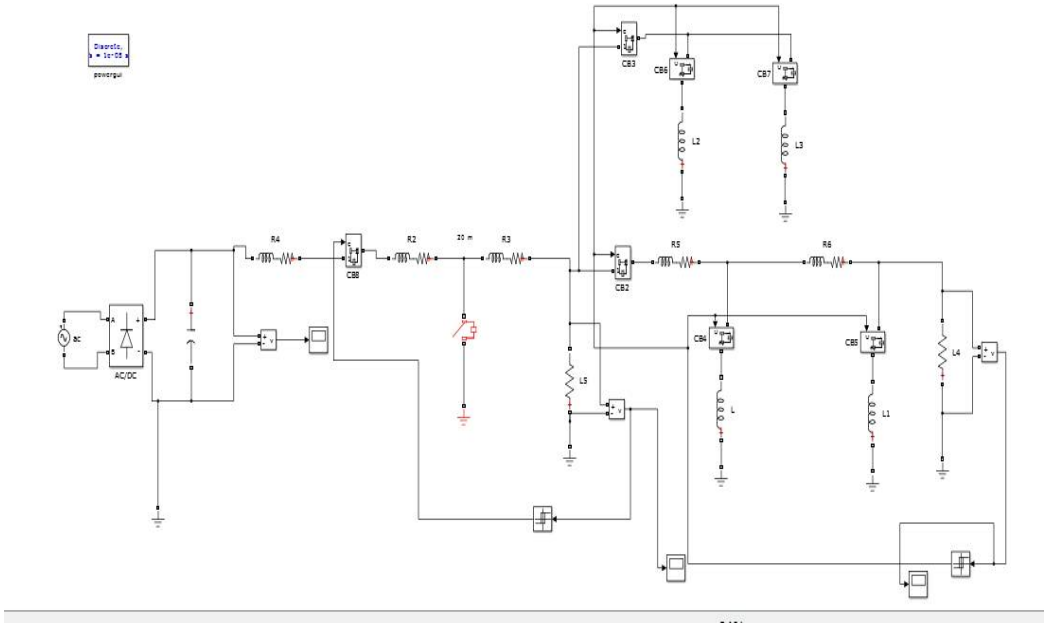

Fig.7simulation setup

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Fault occurs; the converter limits the fault current to 1.5 times of the nominal current in 600 μs. In the system, each level 2 feeder supplies power to four level 3 feeders and each level 3 feeder supplies power to eight constant resistive loads. The equivalent inductance of level 3 feeder is 4.8 μH. The inductance from level 4 breaker to load is 0.432 μH.the fault.Fault 3 is at the downstream of a level 4 breaker. The estimated inductance at the level 3 breaker is shown in Fig. 8.In order to differentiate the levels 3 and 4 faults, a zonal boundary inductor with 2.5 μH is inserted right before each level 4 breaker. Due to the inserted inductor, the estimated inductance at the level 3.and 4 faults, a zonal boundary inductor with 2.5 μH is inserted right before each level 4 breaker. Due to the inserted inductor, the estimated inductance at the level 3.

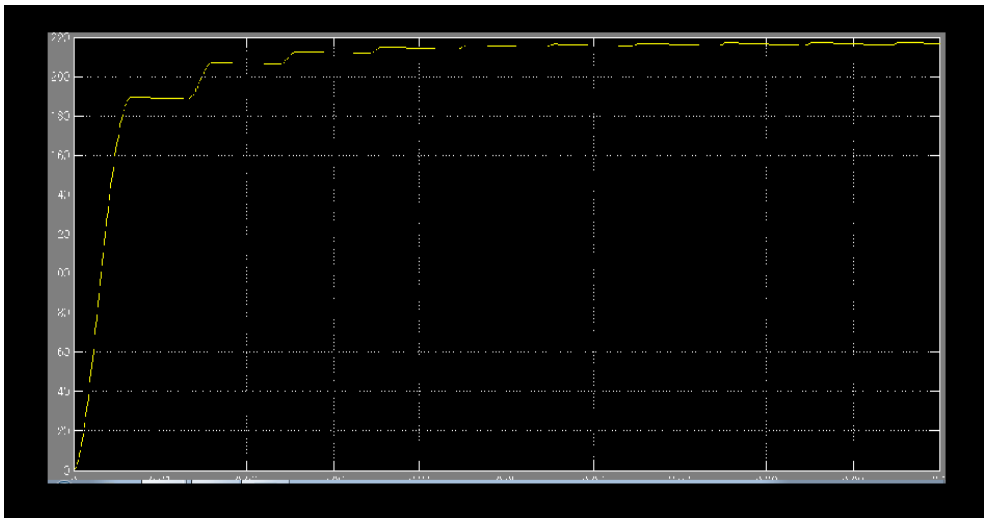

Fig.8Input signal voltage

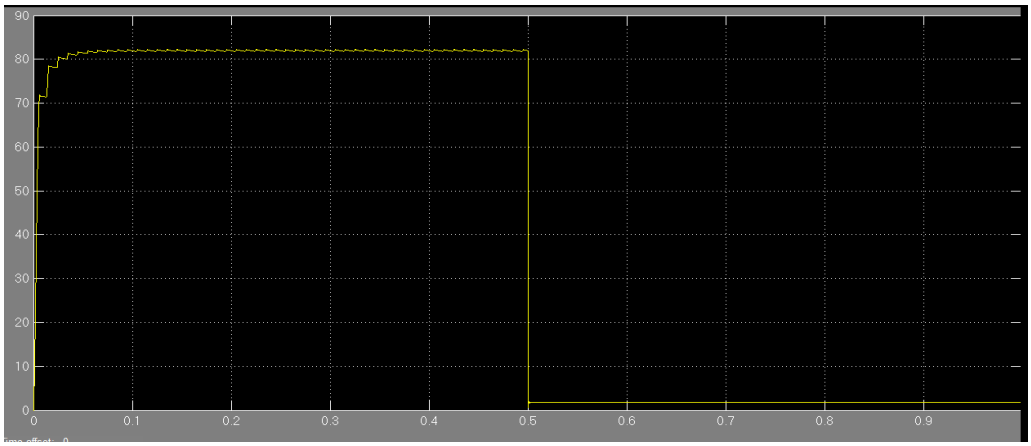

Fig.9Fault signal voltage

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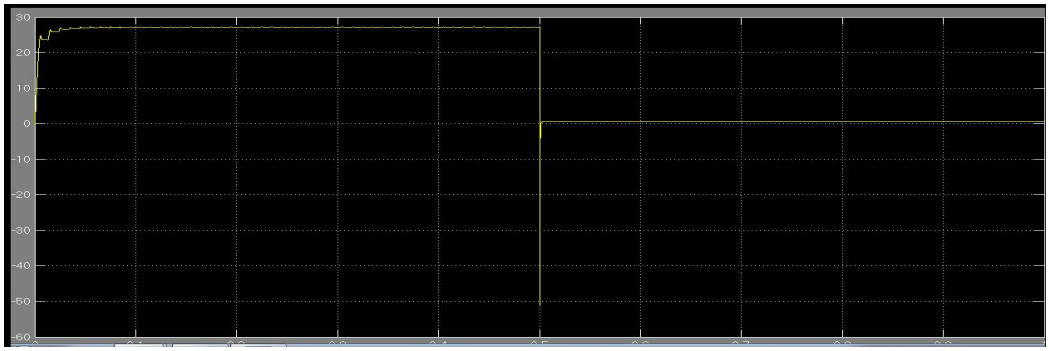

Fig.10 Output signalvoltage

Breaker is above the upper threshold of level 3 and within the tripping zone of level 4, so the level 3 breaker keeps closed and the level 4 breaker is selected to isolate the fault.The numerical simulation results verify that the fault location algorithm can accurately locate faults in the dc distribution system. The fault is detected and located within 1 ms.the inserted zonal boundary inductors provide sufficient discriminations at special conditions and ensure the selectivity of the proposed inductance-based fault location method.

V. HARDWARE VALIDATION

In this section, the hardware validation of the developed inductance-based dc protection scheme is discussed. The di-agram of the scaled-down hardware testing circuit is shown in Fig. 9. The scaled-down hardware test system is illustrated

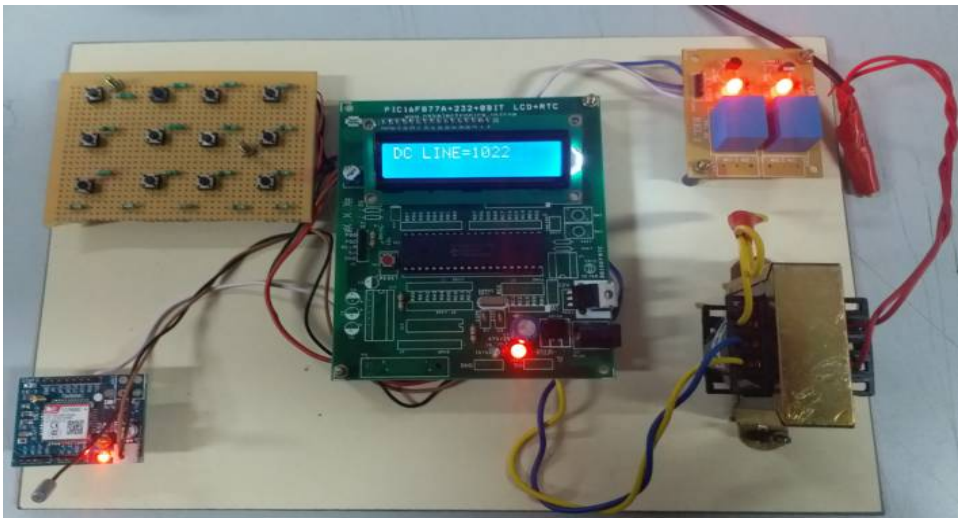

Fig.11 HARDWARE KIT

At the end of the line, an ABB Emax dc breaker [17] is wired to isolate faults. The Emax breaker is normally open and is closed to create a short-circuit fault artificially. If a fault is identified as an internal fault, a tripping signal is generated to open the circuit breaker. The testing system includes a 7.07 mF capacitor, a 6 μH inductor and a line, which is emulated usinga6 or 12 μH inductor. The detailed converter circuit is not included in the testing circuit. This is because the dc fault current is mainly contributed by the output capacitor of the converter. Thus, only the filter capacitor and system equivalent inductors are included in the hardware testing circuit. The capacitor is charged to 12 V

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dc before each the implementation of the developed protection algorithm on the board is shown in Fig. 11. One PRU sequentially reads in data from the analog input channels. The data sampling period is 7 μs. The voltage, current, and $di/dt$are read in sequentially, so the total time to get all samples at one data point is 21 μs. The data are then stored in the processor memory. Once a fault is detected, the fault location routine is activated to locate the fault. The main program uses the most recent ten data points to determine if there is a fault. A control command is sent out andthe program is reinitiated. If there is no fault, the main program goes to the next cycle.A 200 A dc hall-effect sensor [19] is placed at the starting point of the line to measure the dc current. The voltage is also measured at the same point. The $di/dt$is calculated using an analog circuit with input and output filters. The current, voltage, and di/dtsignals are scaled down to the range of 0–1.8 V using linear analog circuits and can be directly taken by the A/D converters on the board. The scaled-down signals then are converted back to their original values in the software program. Once a fault is detected due to high current or low voltage, the fault location routine is activated to locate the fault. If the estimated fault inductance is less than a predefined threshold, a tripping signal will be sent The test results indicate that the inductance estimation error is always less than 20% and the total fault detection and location time is less than or equal to 0.65 ms.

VI.CONCLUSION AND FUTURE WORK

In this paper, a fast fault detection and location algorithm for tightly coupled distribution systems is proposed. The proposed method detects and locates a fault based on local measurements without any communication between protective devices at different locations. The developed algorithm was implemented on a microcontroller board, which can be used as a control unit for protective devices. The fault detection and location algorithm was validated by numerical simulation and hardware tests. The simulation and testing results indicate that the protection algorithm can locate faults in dc distribution systems with fast speed, specifically less than 1 ms, and enough accuracy.Future work focuses on the inductance-based fault location for general dc distribution networks with long cables as well as mixed cables with different characteristics. In addition, a digital di/dtcalculation method will be developed to further improve the fault location accuracy

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