ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Website: www.ijareeie.com

Vol. 6, Issue 11, November 2017

FMO/Manchester Encoding VLSI Architecture using Transmission Gates by SOL's Technique for DSRC Applications

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ABSTRACT: The dedicated short-range communication (DSRC) is an emerging technique to push the intelligent transportation system into our daily life. The DSRC standards generally adopt FM0 and Manchester codes to reach dc-balance, enhancing the signal reliability. Nevertheless, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture for both (Fmo/Manchester). In this thesis, the similarity-oriented logic simplification (SOLS) technique is proposed to overcome this limitation.. The maximum operation frequency is 2 GHz and 900 MHz for Manchester and FM0 encodings, respectively. The power consumption is 1.58 mW at 2 GHz for Manchester encoding and 1.14 mW at 900 MHz for FM0 encoding. The core circuit area is 65.98 × 30.43 μm2. The encoding capability of this thesis can fully support the DSRC standards of America, Europe, and Japan. This thesis not only develops a fully reused VLSI architecture, but also exhibits an efficient performance compared with the existing works.

I.INTRODUCTION

The committed short range correspondence is a convention for maybe a couple way medium range correspondence. The DSRC can be quickly arranged into two classifications: car to-car and car to roadside. In car to-car, the DSRC empowers the message sending and broadcasting among vehicle. The vehicle to-roadside concentrates on the savvy transportation benefit, for example, electronic toll accumulation (ETC).

The DSRC architecture having the transceiver. The following Fig1.1 shows the DSRC transceiver.

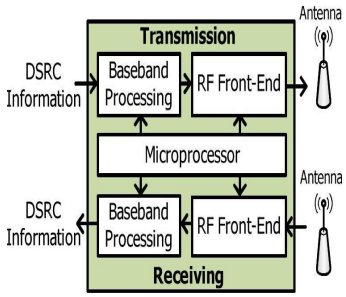

Figure.1 System architecture of DSRC transceiver

The handset having the baseband preparing, RF front end and chip. The chip is utilized to exchange the direction to the baseband handling and RF front end. The RF front end is utilized to transmit and get the remote signs utilizing the reception apparatus. The baseband preparing is in charge of regulation, mistake remedy, encoding and synchronization.The transmitted flag comprises of the discretionary double grouping; it is exceptionally hard to get the

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Vol. 6, Issue 11, November 2017

dc-adjust. The FM0 and Manchester are give the transmitted flag and after that the dc-adjust. The (SOLS) closeness arranged rationale rearrangements having the two strategies: zone minimized retiming and adjust rationale operation sharing. The region smaller retiming used to diminish the transistor tallies and LUT's. The adjust rationale operation sharing is utilized to consolidate the FM0 and Manchester encoding.The DSRC standards have been established by several organizations in different countries. These DSRC standards of America, Europe, and Japan are shown in Table. The data rate individually targets at 500 kb/s, 4 Mb/s, and 27 Mb/s with carrier frequency of 5.8 and 5.9 GHz. The regulation techniques join sufficiency move keying, stage move keying, and orthogonal recurrence division multiplexing. For the most part, the waveform of transmitted flag is relied upon to have zero-mean for vigor issue, and this is additionally alluded to as dc-adjust. The transmitted flag comprises of self-assertive parallel succession, which is hard to get dc-adjust. The motivations behind FM0 and Manchester codes can give the transmitted flag dc-adjust. Both FM0 and Manchester codes are generally received in encoding for downlink. The VLSI models of FM0 and Manchester encoders are checked on as takes after. The framework engineering of DSRC handset is appeared in Fig.1. The upper and base parts are devoted for transmission and accepting, individually. This handset is ordered into three essential modules: microchip, baseband handling, and RF front-end.The microprocessor interprets instructions from media access control to schedule the tasks of baseband processing and RF front-end. The baseband processing is responsible for modulation, error correction, clock synchronization, and encoding. The RF front-end transmits and receives the wireless signal through the antenna.

REVIEW OF VLSI ARCHITECTURES FOR FM0 ENCODER AND MANCHESTER ENCODER

In this task utilizes another Manchester code generator composed at transistor level. This generator utilizes 32 transistors and has an indistinguishable many-sided quality from a standard D flip-slump. It is proposed to be utilized as a part of a complex optical correspondence framework. The primary advantage of this outline is to utilize a time flag running at an indistinguishable recurrence from the information. Yield changes on the rising edge and falling edge of the clock. Facilitate a nMOS transistor is utilized to build the recurrence of operation up to 5 GHz and a rapid VLSI engineering completely reused with Manchester and Miller encodings for radio recurrence distinguishing proof (RFID) applications. This outline is acknowledged in 0.35-µm CMOS innovation and the greatest operation recurrence is 200 MHz. The Manchester encoding design for ultrahigh recurrence (UHF) RFID label emulator is likewise utilized as a part of this venture. This equipment engineering is directed from the limited state machine (FSM) of Manchester code, and is acknowledged into field-programmable door cluster (FPGA) prototyping framework. The most extreme operation recurrence of this outline is around 256 MHz. The comparable outline strategy is additionally connected to exclusively build FM0 and Miller encoders likewise for UHF RFID Tag emulator. Its greatest operation recurrence is around 192 MHz Also a recurrence move keying (FSK) adjustment and demodulation with Manchester codec in equipment acknowledgment is finished.

II.PROPOSED SYSTEM

FM0 ENCODING

FM0 is otherwise called Biphase space encoding. A change is available on each piece and an extra progress may happen amidst the bit. Here the information rate is twice. Adequate clock data can be recouped from the information stream with the goal that a different clock isn't required. Along these lines, for transmission, the quantity of wires is limited. Rationale 0 speaks to the change in the focal point of the bit. Rationale 1 speaks to there is no progress from the focal point of bit. This encoding information contains adequate data to recuperate a clock from the information. It needs to achieve the DC adjust and upgrade flag unwavering quality. It is utilized to diminish clamor and transmission control. Fig 2.3 demonstrates the codeword structure of FM0
The FM0 having the accompanying three guidelines.

- If X is the rationale 0, the FM0 code has the progress between the An and B when clock occasion happens.
- If X is the rationale 1, there is no change is permitted between the An and B.
- The change is designated among each FM0 code regardless of what the X is toward the finish of each clock beat.

Figure.2 Codeword structure of FM0.

The wave form is given below the by following the above rules three. The FM0 having the clock and then the x. The clock and then the cycle having the cycle in each transaction.

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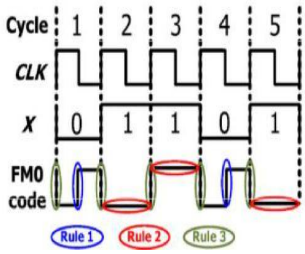

Figure.3 FM0 encoding

A FM0 coding illustration is appeared in Fig. At cycle 1, the X is rationale 0; subsequently, a progress happens on its FM0 code, as indicated by run 1. For straightforwardness, this change is at first set from rationale 0 to - 1. As indicated by run 3, a progress is assigned among each FM0 code, and accordingly the rationale 1 is changed to rationale 0 in the start of cycle 2. At that point, as per govern 2, this rationale level is hold with no progress in whole cycle 2 for the X of rationale 1.Thus, the FM0 code of each cycle can be inferred with these three guidelines specified before.

MANCHESTER ENCODING

Manchester encoding is likewise called stage encoding. It can be utilized for a higher working recurrence. Manchester encoding is an extremely basic strategy and is likely the most ordinarily utilized. The signs can be transmitted serially. In Manchester encoding the normal power is dependably the same, regardless of what information is transmitted. Contrasted with all other encoding strategies, Manchester code takes after a calculation to encode the information. It generally delivers a progress at the focal point of the bit. It contains adequate data to recoup a clock. So if the information rate is twice, adequate clock data can be recuperated from the information stream with the goal that different timekeepers are not required. Subsequently, the electrical association utilizing Manchester code is effectively a galvanic partner isolator (it is the standard of detaching practical areas of electric frameworks to counteract current stream) utilizing a system isolator for straightforward balanced segregation change. In this manner, while transmitting the information, the quantity of wires is limited, which is utilized to decrease the clamor and transmission control.
Rationale "1" speaks to the progress from HIGH to LOW. Rationale "0" speaks to the change from LOW to HIGH. To get a fast, give a synchronized information source as the principal clock beat for input information. While transmitting the information, it is an advanced encoding in which information transmission bits are spoken to by changes starting with one rationale then onto the next rationale. The length of each piece is set as default, and it expends the signs as self-timing. The heading of the progress chooses the condition of the bit. It is here and there important to have a change amidst a bit with the goal that the progress got toward the starting time frame is ignored.

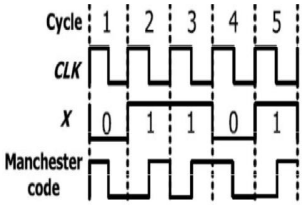

Figure.4 Manchester encoding

The Manchester encoding is realized with the XOR operation for using the CLOCK and X as shown in Figure.6. The clock always has a transition within the one cycle.
The Manchester code is derived from

$$X \oplus CLK \qquad \text{----------(1)}$$

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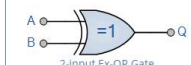
The truth table and symbol for XOR gate is shown

Symbol	Truth Table		
 2-input Ex-OR Gate	B	A	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	0
Boolean Expression Q = A ⊕ B	A OR B but NOT BOTH gives Q		

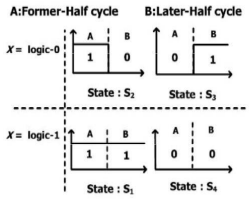
The truth table above shows that the output of an Exclusive-OR gate ONLY goes "HIGH" when both of its two input terminals are at "DIFFERENT" logic levels with respect to each other. If these two inputs, A and B are both at logic level "1" or both at logic level "0" the output is a "0" making the gate an "odd but not the even gate". This ability of the Exclusive-OR gate to compare two logic levels and produce an output value dependent upon the input condition is very useful in computational logic circuits as it gives us the following Boolean expression of:

$Q = (A \oplus B) = A.B + A.B$

The logic function implemented by a 2-input Ex-OR is given as either: "A OR B but NOT both" will give an output at Q. In general, an Ex-OR gate will give an output value of logic "1" ONLY when there are an **ODD** number of 1's on the inputs to the gate, if the two numbers are equal, the output is "0".

FLOW
STATE CODE PRINCIPLE FOR FM0

The FM0 code starts with the FSM principle. The FSM of FM0 code classified into four states. The four states as shown in the below Fig and its state diagram is shown in Fig.



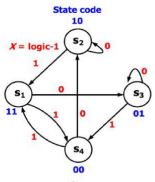


Figure.5 FSM of FM0 Figure.6 State diagram for FSM

Suppose the initial state is S1, and its state code is 11 for A and B, respectively.

- If the X is logic-0, the state-transition must follow both rules for FM01 and 3.
- The only one next-state that can satisfy both rules for the X of logic-0 is S3.
- If the X is logic-1, the state-transition must follow both rules for FM0 2 and 3.
- The only one next-state that can satisfy both rules for the X of logic-1 is S4.

Thus, the state-transition of each state can be completely constructed.

The FSM of FM0 can also conduct the transition table of each state A (t) and B (t) represent the discrete-time state code of current-state at time instant t.

Their previous-states are denoted as the A(t − 1)and the B(t − 1), respectively.

With the transition table in Table 3.1, the Boolean functions of A (t) and B (t) are given as

$$\mathbf{A(t) = B(t-1)} \quad \text{----------(2)}$$

$$\mathbf{B(t) = X \oplus B(t-1)} \quad \text{----------(3)}$$

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With both A(t) and B(t), the Boolean function of FM0 code is denoted as

CLK A(t) + ~ CLK B(t) ----------(4)

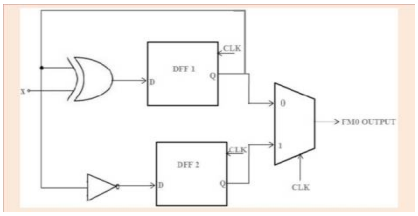

Figure.7 .Block diagram for FM0

The block diagram in Fig3.2 has an XOR gate, DFF, inverter, and MUX. For example, the XOR gate has one input as feedback that is 0, and another input as 1. This XOR output is given to DFF1, and it also has a CLK signal with an output of 1. Another DFF2 has an input as 1 and CLK. The output is 1. Both DFF outputs are given to MUX, and also it has a CLK with it that produces the output based on selection lines. If the selection line is 0, it produces the output as DFF1 as FM0 output. Otherwise, the selection line is 0 and produces an output as DFF2 or FM0 output.

STATE CODE PRINCIPLE FOR MANCHESTER

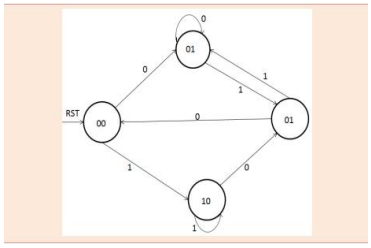

Figure.8 .State Diagram for Manchester

Table 1 For state machine diagram of Manchester encoder

Reset	Input	Current State	Next State
1	-	-	00
0	0	00	01
0	1	00	10
0	0	01	01
0	1	01	11
0	0	10	11
0	1	10	10
0	0	11	00
0	1	11	01

The four states available are 00, 01, 10, and 11 as shown in Fig 3.3. There is also RST. A transition was obtained based on 1 and 0. Based on the Table 3.2, in the initial state, reset is 1, and then the next state will be 00. After that reset it will always be 0. When the input is 0 and the current state is 00, the next state is 01. If the input is 1 and the current state is 00, the next state is 10. When the input is 0, and the current state is 01, the next state is 01. And if the input is 1, and the current state is 01, next state is 11. When the input is 0, and the current state is 10, the next state is 11. If the input is 1, and the current state is 10, the next state is 10. When the input is 0, and the current state is 11, and the next state will be 00. Finally, if the input is 1, and the current state is 11, the next state is 01.

ADVANTAGES FOR MANCHESTER ENCODING

The main advantage is that the signal synchronizes itself, minimizes the error rate, and optimizes the reliability. The drawbacks to this encoding are that more bits are needed to transmit in the Manchester encoding signal than the original signal, and it needs more bandwidth.

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DESIGN OF FMO/MANCHESTER

The hardware architecture of the fm0/Manchester code. The top part is denoted the fm0 code and then the bottom part is denoted as the Manchester code. In FM0 code the DFFA and DFFB are used to store the state code of the FM0 code and also mux_1 and not gate is used in the FM0 code.

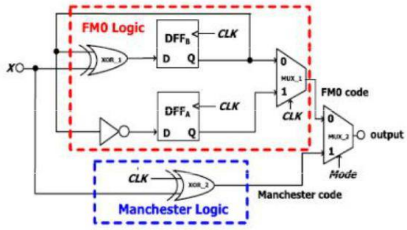

Figure.9 .Hardware architecture of FM0 and Manchester

- When the mode=0 it is for the FM0 code.
- The Manchester code is developed only using the XOR gate and when the mode=1 is for the Manchester code.

The component is defined as the hardware to perform a specific logic function, such as AND, OR, NOT, and flip-flop. The active components in the above Table 4.1 means the components are work in the both FM0 and Manchester code no matter what encoding method is adopted. The total components means the number of the components are present in the whole circuit.

The HUR rate is calculated by following formula

$$HUR = \frac{\text{Active Components}}{\text{Total Components}} \times 100\%$$

For both the encoding methods the total components is 7.For the FM0 code the total component is 7 and then the active component is 6.In Manchester code the total component is 7 the active components are 2 used without SOLS.
For FM0 encoding, the active components are 6, and its HUR is 85.71%. For Manchester encoding, the active components are 2, comprising XOR−2 and MUX−2, and its HUR is as low as 28.57%. On average, this hardware architecture has a poor HUR of 57.14%, and almost half of total components are wasted.In proposed work reduce the total components from 7 to 6 and. In this paper two multiplexer is used in proposed work reduce two multiplexer from one multiplexer, when reduce the multiplexer the total components are reduced the area and then the power consumption also reduced.

LIMITATION ANALYSIS ON HARDWARE UTILIZATION OF FM0 ENCODER AND MANCHESTER ENCODER

- This hardware architecture has a poor HUR of 57.14%, and almost half of total components are wasted.
- The coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture.
- The number of LUT's required here are 5 and so the power required for implementing this encoding architecture is also high.

The purpose of SOLS technique is to design a fully reused VLSI architecture for FM0 and Manchester encodings.
The SOLS technique is classified into two parts

- Area compact retiming
- Balance logic operation sharing

Each part is individually described as follows. Finally, the performance evaluation of the SOLS technique is given.

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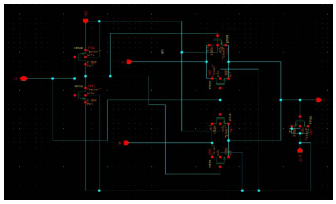
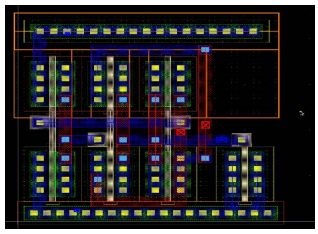
III. RESULTS

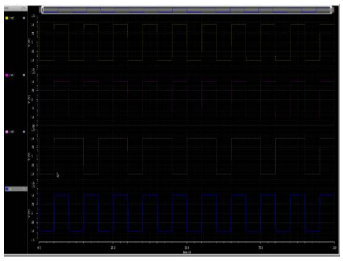
MUX-CLOCK-SCHEMATICS



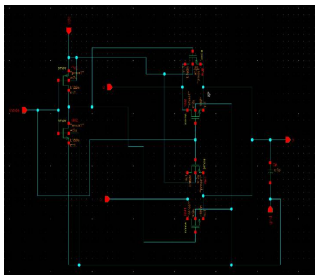
MUX-CLOCK-LAYOUT



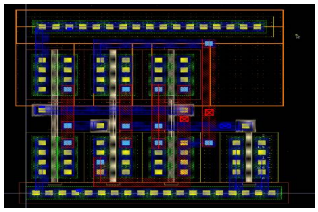
MUX-CLOCK-OUTPUT WAVE FORMS



MUX-MODE-SCHEMATIC



MUX-MODE-LAYOUT



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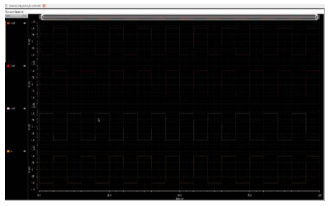
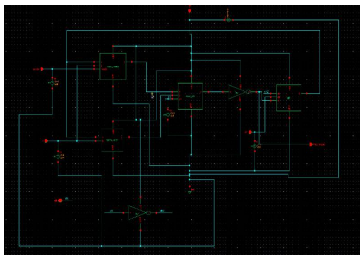
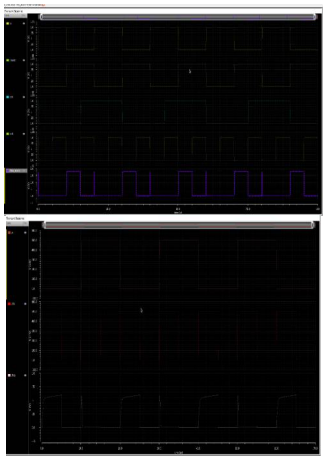
MUX-MODE-OUTPUT WAVE FORMS



FMO/MANCHESTER SCHEMATIC



FMO/MANCHESTER WAVE FORMS



IV.CONCLUSION

The coding-decent variety amongst FM0 and Manchester encodings causes the confinement on equipment use of VLSI engineering outline. A confinement examination on equipment usage of FM0 and Manchester encodings is talked about in detail. In this thesis, the completely reused VLSI engineering utilizing SOLS procedure for both FM0 and Manchester encodings is proposed. The SOLS system kills the confinement on equipment usage by two center strategies: area compact retiming and adjust rationale operation sharing. The region conservative retiming moves the equipment asset to decrease 22 transistors. The adjust rationale operation sharing proficiently joins FM0 and Manchester encodings with the indistinguishable rationale parts. The encoding capacity of this thesis can completely bolster the DSRC norms of America, Europe, and Japan. This paper builds up a completely reused VLSI engineering, as well as displays an aggressive execution contrasted and the current works.

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V.FEATURE SCOPE

Nonetheless, the coding-assorted variety between both truly constrains the possibility to plan a VLSI design that can be completely reused with each other. This paper proposes a VLSI engineering configuration utilizing comparability arranged rationale rearrangements (SOLS) procedure. The SOLS comprises of two center techniques: territory conservative retiming and adjust rationale operation sharing. The region minimal retiming moves the equipment asset to diminish 22 transistors. The adjust rationale operation sharing effectively joins FM0 and Manchester encodings with the completely reused equipment design. With SOLS system, this paper builds a completely reused VLSI engineering of Manchester and FM0 encodings for DSRC applications. The analysis comes about uncover that this plan accomplishes a proficient execution contrasted and modern works.

REFERENCES

[1] F. Ahmed-Zaid, F. Bai, S. Bai, C. Basnayake, B. Bellur, S. Brovold, et al., "Vehicle wellbeing interchanges—Applications (VSC-A) last report," U.S. Dept. Trans., Nat. Parkway Traffic Safety Admin., Washington, DC, USA, Rep. Spot HS 810 591, Sep. 2011.
[2] J. B. Kenney, "Committed short-run interchanges (DSRC) measures in the United States," Proc. IEEE, vol. 99, no. 7, pp. 1162– 1182, Jul. 2011.
[3] J. Daniel, V. Taliwal, A. Meier, W. Holfelder, and R. Herrtwich, "Outline of 5.9 GHz DSRC-based vehicular wellbeing correspondence," IEEE Wireless Commun. Mag., vol. 13, no. 5, pp. 36– 43, Oct. 2006.
[4] P. Benabes, A. Gauthier, and J. Oksman, "A Manchester code generator running at 1 GHz," in Proc. IEEE, Int. Conf. Electron., Circuits Syst., vol. 3. Dec. 2003, pp. 1156– 1159.
[5] A. Karagounis, A. Polyzos, B. Kotsos, and N. Assimakis, "A 90nm Manchester code generator with CMOS switches running at 2.4 GHz and 5 GHz," in Proc. sixteenth Int. Conf. Syst., Signals Image Process., Jun. 2009, pp. 1– 4.
[6] Y.- C. Hung, M.- M. Kuo, C.- K. Tung, and S.- H. Shieh, "Rapid CMOS chip outline for Manchester and Miller encoder," in Proc. Intell. Inf. Concealing Multimedia Signal Process., Sep. 2009, pp. 538– 541.
[7] M. A. Khan, M. Sharma, and P. R. Brahmanandha, "FSM based Manchester encoder for UHF RFID label emulator," in Proc. Int. Conf. Comput., Commun. Netw., Dec. 2008, pp. 1– 6.
[8] M. A. Khan, M. Sharma, and P. R. Brahmanandha, "FSM based FM0 and Miller encoder for UHF RFID label emulator," in Proc. IEEE Adv. Comput. Conf., Mar. 2009, pp. 1317– 1322.
[9] J.- H. Deng, F.- C. Hsiao, and Y.- H. Lin, "Top down plan of joint MODEM and CODEC discovery plans for DSRC coded-FSK frameworks over high versatility blurring stations," in Proc. Adv. Commun. Technol. Jan. 2013, pp. 98– 103.
[10] I.- M. Liu, T.- H. Liu, H. Zhou, and A. Aziz, "Synchronous PTL cradle addition and estimating for limiting Elmore delay," in Proc. Int. Workshop Logic Synth., May 1998, pp. 162– 168.
[11] H. Zhou and A. Aziz, "Support minimization in pass transistor rationale," IEEE Trans. Comput. Supported Des. Integr. Circuits Syst., vol. 20, no. 5, pp. 693– 697, May 2001.
[12] N. H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective, second ed., Upper Saddle River, NJ, USA: Pearson Educ. Ltd., 1993, pp. 98– 103.

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