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A Symmetric Multilevel Voltage Source Inverter with Reduced Number of Switches

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ABSTRACT: Multilevel inverters are preferred over conventional inverters as the quality of output voltage improves with the number of voltage steps at the output. In addition, low switching losses, low voltage stress on the switches, high efficiency and better electromagnetic interference are the advantages of multilevel inverters. But the cost, circuit size so installation space, complexity of control scheme and reliability are dependent on number of circuit devices used. Thus the number of circuit devices used in the multilevel inverter has to be reduced. To achieve this, a modified symmetric multilevel voltage source inverter is proposed to generate fifteen levels of voltage using a lower number of circuit devices including power semiconductor switches and gate driver circuits. That is conventional cascaded H-bridge multilevel inverter can be replaced with the suggested symmetric multilevel inverter with reduced switches which is cost effective and has simple control scheme. Simulation for the suggested topology has been carried out using MATLAB-simulink software and the output voltage with fifteen levels has been obtained. The simulation results thus obtained confirms the superiority of the proposed topology over the existing topologies.

KEYWORDS: Multilevel Inverters (MLI), Symmetric Multilevel Inverter, Reduction of Switches.

I.INTRODUCTION

Multilevel inverters are emerging as a viable alternative for most of the applications because of their higher output power quality, lower total harmonic distortion, higher amplitude of the fundamental component, higher efficiency, lower switching losses, and lower *dv/dt*. These advantages are the reason for the transition from the conventional two-level inverter to multilevel structures. They include an array of power semiconductors and dc voltage sources, the output of which generate voltages with stepped waveforms. Three broad classification of multilevel inverters are Diode clamped MLI, Flying Capacitor MLI and Cascaded H-bridge(CHB) MLI. The Cascaded H bridge inverter can be divided into two groups from viewpoint of values of the DC voltage sources: the symmetric and the asymmetric topology. In the symmetric topology, the values of all the DC voltage sources are equal. This characteristic gives the topology good modularity. However the number of switching devices rapidly increases by increasing the number of output voltage level. In order to increase the number of output voltage level, the value of DC voltage sources are selected to be different, these topologies are called asymmetric.

The Cascaded H-Bridge multilevel inverter has been industrially employed in several application fields such as pump, fans, compressors etc. In addition, they have been recently proposed for other applications like photovoltaic power-conversation system and wind power conversion. In this paper a new configuration of symmetric multilevel inverter is suggested which can generate more number of levels using lower number of circuit components compared with the conventional CHB inverter. Lower circuit component reduces power losses and voltage drops. The simulation results and its comparison with the conventional CHB inverter demonstrate its benefits.

II. SYMMETRIC TOPOLOGY

Fig. 1 depicts the overall view of the proposed symmetric multilevel inverter. The proposed topology is composed of n-isolated dc voltage sources. Among different topologies of cascaded multilevel inverter the presented work deals with the symmetric MVSI which means the value of DC voltage sources selected are same. The quality of the output voltage may deteriorate due to the inequality of dc voltage sources and as a result of inequality of voltage levels.

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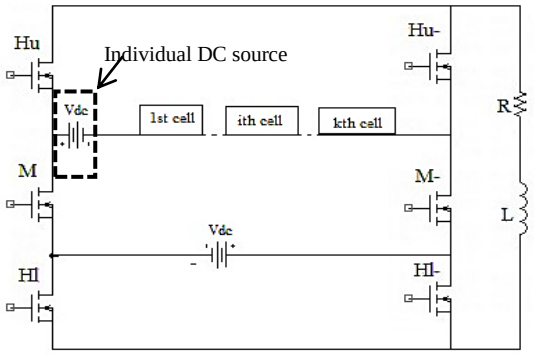

Fig 1. Overall view of symmetric multilevel voltage source inverter.

The proposed inverter is constituted of k cells that is basic units, as shown in Fig. 1. The basic unit of the suggested MLI is expressed in Fig. 2. Three dc voltage sources and four power switches are the elements of the basic cell. Each power switch consists of a metal oxide semiconductor field effect transistor. The equivalent circuits for the basic cell of the suggested MLI with the modes of working to generate various voltage levels are illustrated in Fig. 3(a)–(d). As mentioned in the figure, the operation of "not turning on the switches at the same time" can prevent a short circuit. Hence, switches (S1 with S1') and (S2 with S2') are controlled in a complementary manner. The output of each basic unit is four levels that consist of three positive and zero values. Various switching states of the basic cell of the suggested topology, for each output voltage step, are represented in Table I. Table I shows that the relevant switch is turned on, and 0 points out the off-state. A provided output phase voltage is synthesized by individual voltages of dc sources. The reason for calling the proposed topology symmetric topology is the same value of (Vdc) for all dc voltage sources .The basic unit of proposed symmetric multilevel inverter can be given as follows.

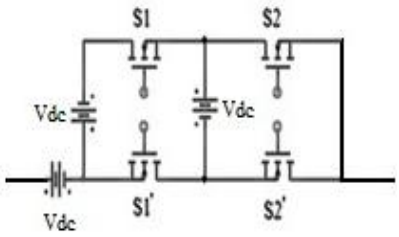

Fig 2.Circuit diagram of the basic unit of the suggested Topology.

If m represents the number of levels, then the number of DC voltage sources required are given by,

$$n = \frac{m-1}{2} \quad (1)$$

Then the basic unit in this configuration determines the number of output levels to be generated. Hence the number of basic units used gains importance here. If k represents number of basic units used, then the expression for k is given as,

$$k = \frac{n-1}{3} \quad (2)$$

where n is the number of DC voltage sources.

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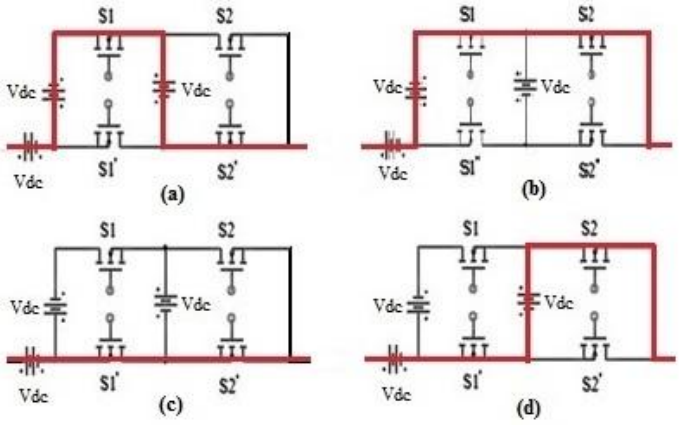

Fig. 3. Equivalent circuits of modes of operation of basic unit for (a) 3Vdc, (b) 2Vdc, (c) Vdc, and (d) zero level.

TABLE 1

Switching states of basic unit of suggested symmetric mli

MODES	S1	S2	Vo
1	1	0	+3Vdc
2	1	1	+2Vdc
3	0	0	+Vdc
4	0	1	0

The next important parameter to be decided is the total number of switches to be used in the suggested inverter which is given as,

$N_{switch} = \frac{4n+10}{3}$, with individual DC source

$N_{switch} = \frac{4n+14}{3}$, without individual DC source (3)

Number of driver circuits required to give pulses to the switches are given as

$$N_{Driver} = N_{switch} \quad (4)$$

The power loss in any inverter can be studied under two types:

i.Conduction losses: this results due to the equivalent resistance and the on-state voltage drop of switches.

ii.Switching losses: practical switches suffer from switching losses due to their non-ideality.

Losses across the MOSFET switches can be calculated using the following equation.

$$P_T(t) = [V_T + R_T i^{\beta}(t)]i(t) \quad (5)$$

V_T and R_T are the on state voltage and internal resistance of MOSFET respectively. β is the constant dependent on MOSFET characteristics. Thus the general characteristics of the suggested symmetric multilevel inverter is discussed.

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III. SIMULATION AND RESULTS

The simulation for eleven level and fifteen level inverters based on the suggested symmetric topology is made by using MATLAB-Simulink.

Eleven level Inverter

The circuit diagram of the eleven level symmetric multilevel inverter is shown in figure 4 with ten switches and five DC voltage sources. The input DC voltage source V_{dc}=7.5 Volt. Five DC voltage sources are used and are of same magnitude 7.5 volt, since this is symmetric topology. The Simulink block of the eleven level symmetric inverter is shown below.

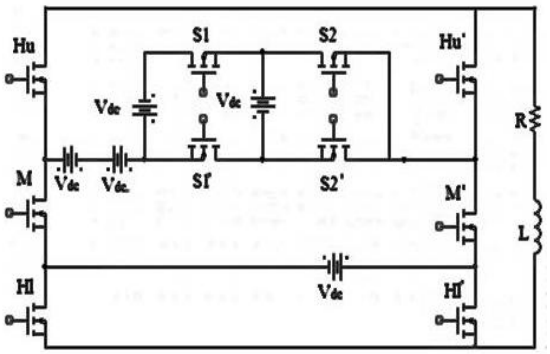

Fig 4. Circuit diagram of eleven level inverter

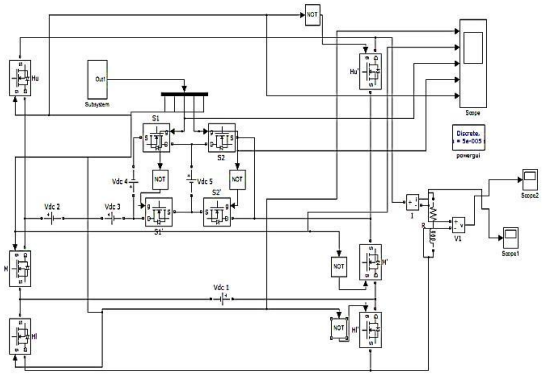

Fig 5. Simulink block of eleven level inverter

TABLE II

Switching States of eleven level inverter

Voltage/ Switches	H_l	M	S_1	S_2	H_u
5Vdc	1	0	1	0	1
4Vdc	1	0	1	1	1
3Vdc	0	0	1	1	1
2Vdc	0	0	0	0	1
1Vdc	1	0	-	-	0
0Vdc	0	0	-	-	0
-Vdc	1	1	0	0	0
-2Vdc	0	1	1	0	0
-3Vdc	1	1	1	1	0
-4Vdc	0	1	1	1	0
-5Vdc	0	1	1	0	0

The output of the eleven level symmetric inverter is observed under three categories. They are output voltage, output current and the Total Harmonic Distortion.

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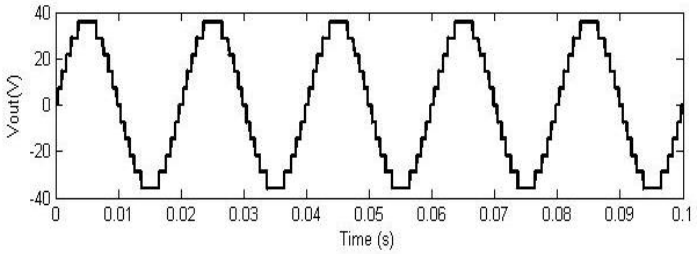

Fig 6. Simulated Output Voltage Of Eleven Level Symmetric Inverter

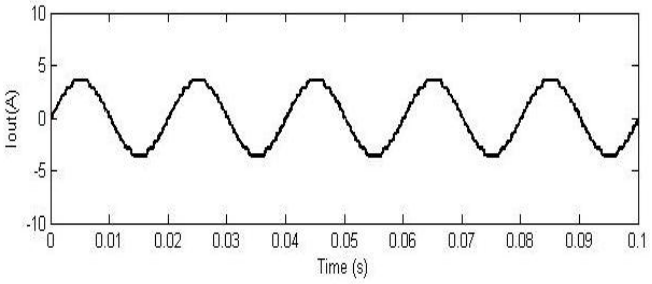

Fig 7. Simulated output current Of Eleven Level Symmetric Inverter

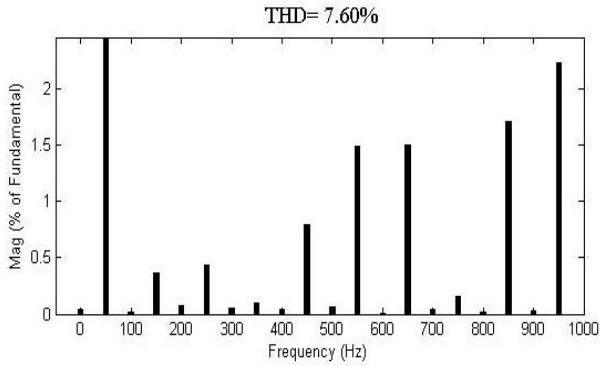

Fig 8. Total Harmonic Distortion Of Eleven level Symmetric Inverter

The above figure 7 represents the Total Harmonic Distortion of the eleven-level symmetric inverter. The THD level obtained is 7.60% which is considerably high and can reduce the quality of sinusoidal output voltage. Hence the reduction of THD is made further with the increasing in output levels of the symmetric multilevel inverter.

FIFTEEN LEVEL INVERTER

In general, the symmetric topology of inverters cannot synthesize as many voltage levels when compared to asymmetric topologies. But the modularity, easy realization, reduced cost and simple control scheme of symmetric topologies makes it more reliable. The inverter presented here will be equipped with all the advantages of the symmetric topology and also existing eleven level symmetric inverter is extended to fifteen levels. The circuit diagram of the proposed fifteen-level symmetric inverter is shown in the figure 8. The circuit of suggested multilevel inverter consists of modified H-bridge with switches H_u, M, H_l, its complementary switches H_u', M', H_l', the basic unit in the middle with switches S_1, S_2, , S_3, , S_4 and its complementary switches S_1', S_2', S_3', S_4'. All these switches are used to bypass the DC voltage sources V_{dc} as shown in the circuit diagram.

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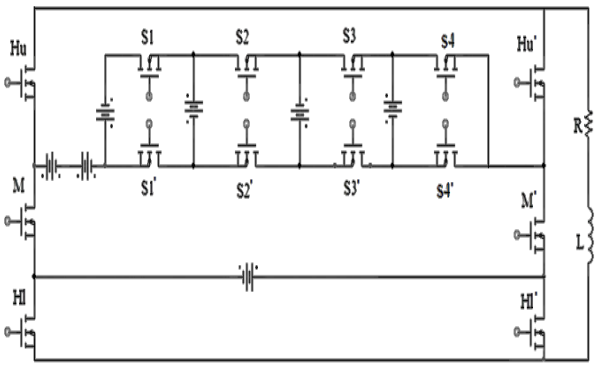

Fig 8. Circuit Diagram Of The Fifteen Level Inverter

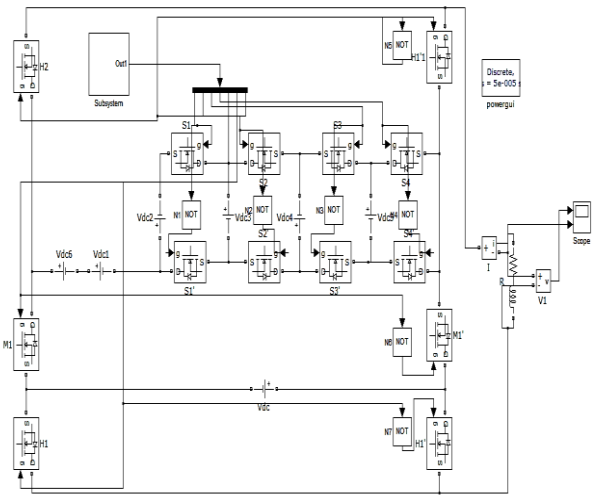

Fig 9. Simulink Model Of fifteen level inverter.

The switching pattern of the fifteen level inverter is mentioned in the following table. The switches are turned on and off based on this switching table. The Simulink model of the fifteen level symmetric multilevel inverter is shown in figure 9. The input DC voltage source V_{dc}=7 Volt. Seven DC voltage sources are used and are of same magnitude 7 volt, since this is symmetric topology. The pulses are generated at the fundamental frequency of 50 Hz for all the switches.

TABLE III

Switching States of fifteen level inverter

Voltage/ Switches	Hu	S1	S2	S3	S4	M	H1
7Vdc	1	1	0	1	0	0	1
6Vdc	1	0	0	1	1	0	1
5Vdc	1	1	0	0	0	0	1
4Vdc	1	1	1	1	1	0	1
3Vdc	0	1	1	1	1	1	1
2Vdc	0	0	0	0	0	1	1
Vdc	0	-	-	-	-	0	1
0Vdc	0	-	-	-	-	0	0
-Vdc	1	-	-	-	-	1	0
-2Vdc	1	0	0	0	0	0	0
-3Vdc	1	1	1	1	1	0	0
-4Vdc	0	1	1	1	1	1	0
-5Vdc	0	1	0	0	0	1	0
-6Vdc	0	1	0	1	1	1	0
-7Vdc	0	1	0	1	0	1	0

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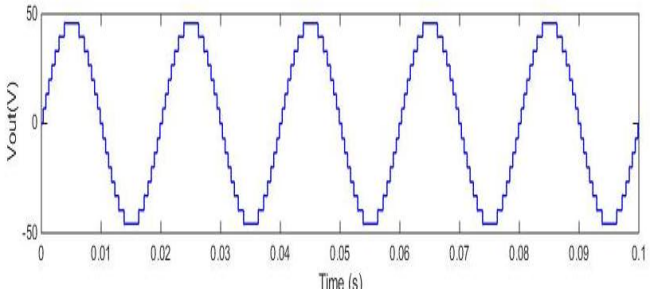

Fig 10. Simulated Output Voltage Of Fifteen Level Symmetric Inverter

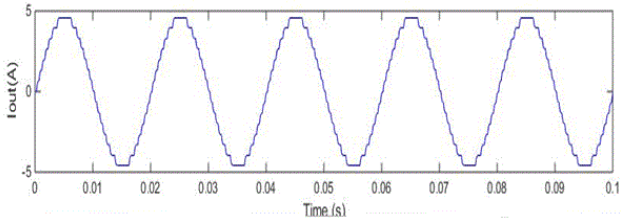

Fig 11. Simulated Output Current Of Fifteen Level Symmetric Inverter

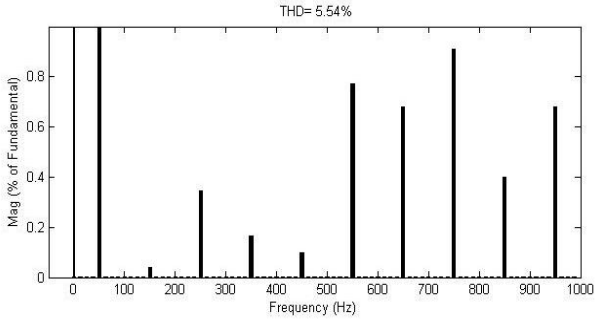

Fig 12.Total Harmonic Distortion of Symmetric Fifteen-Level Inverter

The above figure 12 represents the Total Harmonic Distortion of the fifteen-level symmetric inverter. The THD level obtained is 5.54% which is considerably low than the eleven level symmetric inverter and can increase the quality of sinusoidal output voltage.

IV.COMPARISON WITH CONVENTIONAL CHB

The simulation results of the eleven and fifteen level symmetric inverter is compared with the conventional cascaded H-bridge inverter in terms of number of switches and total harmonic distortion.

TABLE IV

Comparison table of THD content in suggested fifteen level inverter with conventional CHB

Levels	THD in conventional CHB	THD in suggested inverter
Eleven level	11.50[10]	7.60
Fifteen level	10.15[11]	5.54

TABLE V

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Comparison table of number of switches in suggested fifteen level inverter with conventional CHB

Levels	Number of switches in conventional CHB	Number of switches in suggested inverter
General form	4n	$\frac{4n+14}{3}$
Eleven level	20	10
Fifteen level	28	14

V.CONCLUSION

A modified symmetric fifteen level multilevel inverter has been developed and simulated using MATLAB. The proposed symmetric fifteen level multilevel inverter is found to have less number of devices required in application point of view considering its reduction in cost, installation space and circuit difficulties. The proposed topology uses simple modulation method for getting the high quality of output voltage. This makes the control method simple and the suggested symmetric voltage source inverter can be realised easily with the simple control scheme itself. The THD of existing symmetric eleven level multilevel inverter is 7.60%. The THD of proposed symmetric fifteen level multilevel inverter is 5.54%. On comparing the THD of the existing system with that of proposed system the THD of later is low. The future work focuses on implementing the symmetric multilevel inverter with increase in the number of levels produced from minimum number of switching devices in an experimental prototype.

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