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A Methodology for Improvement of Domino Logic Based Circuits for Electronic Applications

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ABSTRACT- Domino logic is used in high speed techniques for the digital circuit and requires less area in large circuits as compare to static CMOS circuits which uses n-channel MOSFET (NMOS) only. Research work in the domain of improvements in the design of Nano-fabrication based devices is an area which has received much attention in the last two decades. A key parameter in such developed works is the reduction in the power requirement and the improvement of the delay time. In this paper, a new methodology for improvement of Domino Logic Based OR Gate has been proposed. The proposed domino logic based circuit has less speed-power product and when compared to previous reported literature the presented methodology in this design work gives 74% reduction in power requirement and 31% reduction in the delay time. Complete circuit is simulated using Tanner EDA tool, using library IBM 90 nm technology having a supply of 1 Volt per simulation studies.

KEYWORDS: Dynamic logic gates, Domino Logic, Simulation study, Tanner EDA , Power, Delay time, Power Delay Product (PDP).

I.INTRODUCTION

The area reduction and high performance advantages have made dynamic logic circuits a main implementation option for high performance circuits such as high speed microprocessors. This performance advantage comes at the cost of high power dissipation. Mostly domino logic finds its application in high speed in digital circuits as it requires less area in large circuit compared to static CMOS. Applications such as dynamic memories and microprocessor [1]-[3] have observed the application of domino logic for the aforementioned advantages. Construction of the domino logic involves the addition of an inverter at the output of the dynamic gate. The basic domino logic circuit based on the OR gate is shown in fig 1.

Working of this circuit is as follows. When the clock is low (CLK = 0), PMOS transistor Mp is turn ON and NMOS transistor Mn is OFF, dynamic node charge to V_{dd} (Supply voltage), and circuit is pre-charge state which causes the output to be equal to zero. When clock is high, such that the PMOS transistor Mp is OFF and NMOS transistor Mn is turn ON, there exist two condition of output depend to input of pull down network. Condition (1): When input of pull down network IN1 and IN2 are high, charge store at dynamic node will be discharge through ground, so that output is equal to 1. And in the second condition when the input of the pull down network is low, the dynamic node should be maintained high so that the output is equal to zero.

Thecurrent research work reported in this paper is used to present a new methodology for system designing of domino logic circuit scheme in order to improve the power, delay and the power-delay product. Organization of the paper is as follows. Section II presentsa brief background work related to domino logic, while the problem related to domino logic is covered in section III. Section IV presents the new proposed domino logic circuit scheme and simulation results and comparisons are discussed in section V. The paper concludes with the findings of the research work in the conclusion reported in Section VI.

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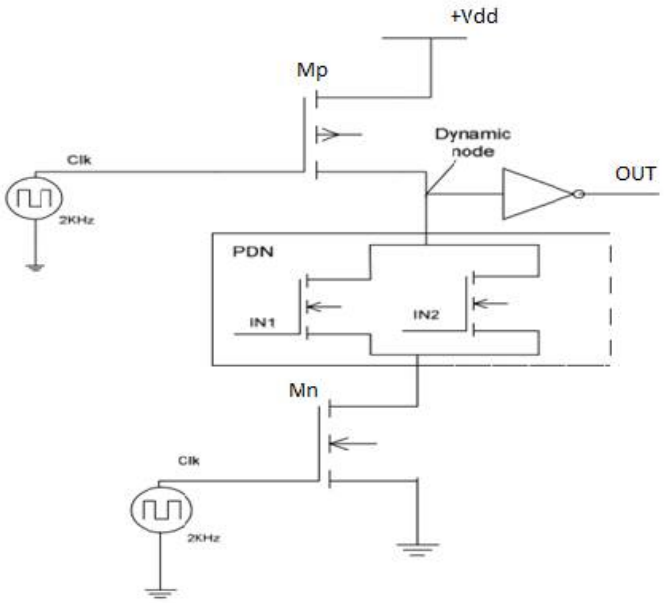

Fig.1 Footer domino logic circuit

II.LITERATURE REVIEW/RELATED BACKGROUND WORK

Domino logic circuitsexperience two major issues when clock is high and both input of pull down network are zero i.e. in the evaluation phase. The problems are the charge sharing and charge redistribution at the dynamic node (as shown in fig.1) and the presence of noise impulses at the input of NMOS pull down network which increases the gate to source voltage resulting in the increase of the charging current at the dynamic node[4].To address this issue at the NMOS transistor under the condition of pull down network where there is charge storage resulting in a capacitance at dynamic node, researchers have suggested use of PMOS keeper circuits in footer domino logic. This is achieved by the use of a PMOS keeper at the dynamic node of the circuit as shown in Fig 2.

Under this condition the working of Footer domino logic with keeper is as follows-
When clock is high transistor Mp is OFF and keeper transistor Mp1 is ON. This results in the charge formation at dynamic node due to the V_{dd} supply voltage and circuit is operational in the pre-charge state so that output is equal to zero. With the help of the keeper in the modified circuit arrangement, the charge is maintained in the dynamic node, which will result in a zero output of the circuit. The basic aim of adding keeper circuit is to provide the device with the ability to store charge at dynamic node during evaluation phase, when inputs of pull down network are equals to zero.Here the keeper circuit can be said to have worked as afeedback path. However, when a noise voltage signal occurs at input of pull down network, the keeper cannot maintain the voltage level of the dynamic node. This is because with presence of noise the NMOS transistor of the pull down network will have an increase in voltage with subsequent increase in the sub-threshold current. This is due to the exponential relation between sub-threshold leakage current and voltage Vgs. Therefore when noise impulse occurs at gate input of pull down network, which results in the increase in Vgs and dynamic node gets discharged [5]. To improve the performance of the circuits due to the noise, researchers have used varioustechniques, but there are inherent issues regarding the size or area of the circuitry, the powerand delay related issues [6]-[7]. Keeper circuits are used to eliminate the sub-threshold leakage current at dynamic node, when clock is high and both input of pull down are zerofor the operation in the evolution phase, the keeper PMOS prevents the charge to be stored in at the dynamic node[8,9].During this phase, when input of the pull down network is equals to one, charge stored at dynamic node will leak away through footer transistor Mn. This will be

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due to thenoise impulses at the input of NMOS pull down network which increases the gate to source voltage. To address this problem further improvement in domino logic circuit has been proposed by Shiksha et.al. [10] by using current mirror circuits which are arranged in stacks.

The domino logic circuit as proposed by Shiksha et.al. [10] is shown in Fig.3. In this circuit current mirror circuits are used in stack in place of footer transistor. If any noise signal occurs at M1 it will be leaked to the ground via M4 and M5(which act as current mirrors). Transistors M3 and M4 also forms current mirror, due to both current mirror circuits gate to source voltage of NMOS pull down network decreases rapidly. This effect is called as stacking effect[12]. The purpose of M4 and M5 used in the domino logic circuit is to create stacking effect, due to which voltage drop across M2 reduces [11,12].The presence of current mirrors in this modified circuit causes increase in the delay. To overcome this problem, size (W/L ratio) of PDN should be increased. Because of stacking effect circuit dissipates power and becomes less noise robust. In [10]the circuit will experience voltage drop in the evaluation phase due to stacked current mirrors. Due to negative Vgs, there will be exponential reduction in sub-threshold current in the circuit. In order to improve the power-delay product, the size of the PMOS transistor should be made at least four times that of NMOS transistor in inverter circuit at the output node. This power delay product can be varied using the transistors M6 and M7. Purpose of transistor Mp3 is to provide strong V_{dd} to the lower PMOS Mp2. This is needed because PMOS transistors are used to provide strong ON (or 1)logic to the circuits.

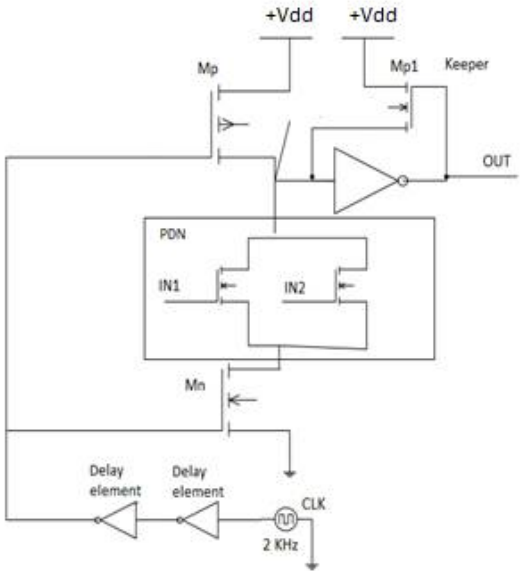

Fig. 2. Footer domino logic circuit with keeper

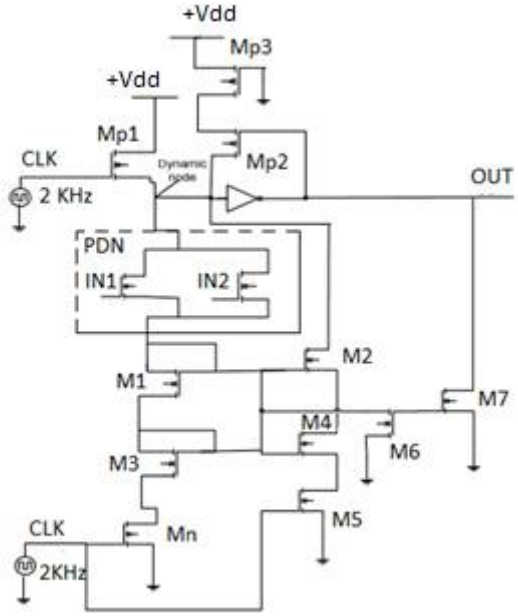

Fig. 3. Domino logic circuit as proposed by Shiksha et.al.[10]

III.CONTRIBUTION OF THE PRESENTED WORK

Domino logic circuit as proposed by Shiksha *et.al.* [10] gives best value of power-delay product when the size of the transistors M6 and M7 is 500nm.This is due to the fact that on increasing size of transistors, the resistance and time constant of the device is reduced, therefore delay of the circuit is reduced. However due to the addition of these transistors the circuit becomes more complex, draws more power and increases the delay time. In order to improve the circuit developed in [10], this paper presents a novel domino logic scheme as shown in Fig.4. Theproposed design shares the same working principle as that of the domino logic circuit presented in [10]. Improvement of the circuit performance in terms of power reduction and reduction in the delay period is achieved by providing a direct path for discharge of pull down network.For direct discharge path we remove the current mirror transistor M3 and M4 and use

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transistor M1 & Mn in place of transistor M1, M4, M5 for one discharge path, while substituting transistor M1, M3, Mn for other discharge path by using transistor M2 and Mn as shown in fig 4. For direct discharge path we use only one footer transistor Mn in place of footer transistor Mn and M5. For variation of power delay product of the circuit we use one transistor Mn instead of transistor M6 and M7. Thus this scheme removes the transistor M6 and M7 altogether from the circuit which further reduce power, delay and ultimately PDP of proposed circuit. When compared with the results of the scheme in [10] the proposed domino logic as reported in this paper givesbetter results for reduced power and delay.

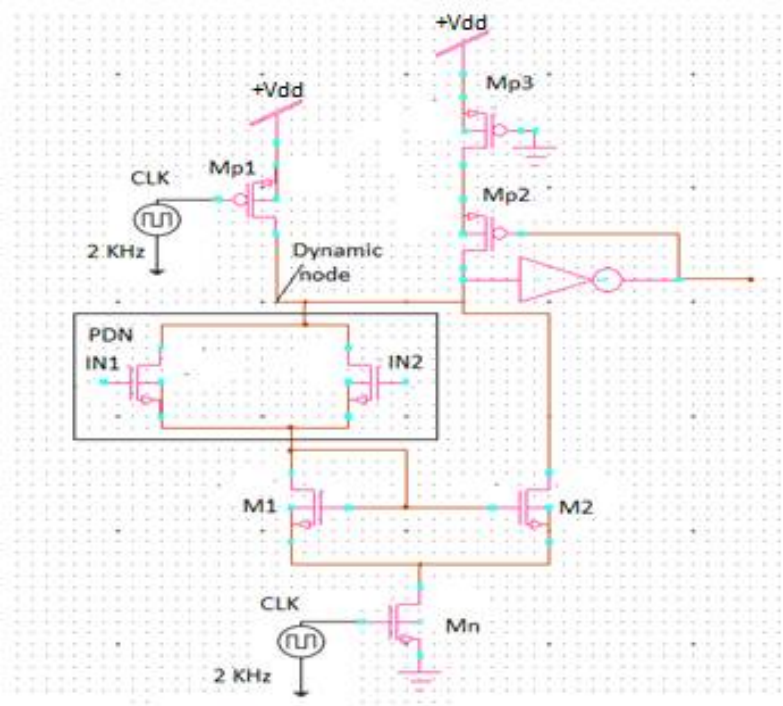

Fig.4 Proposed domino logic circuit

IV. SIMULATION OF DOMINO LOGIC BASED CIRCUITS

For the design of the domino logic based circuits, TANNER EDA software platform has been used (IBM 90nm technology file) for simulation purpose. Tanner EDA is a suite of tools which allow you to enter schematics, perform SPICE simulations, do physical design (i.e. Chip layout), and perform design rule checks (DRC) and layout versus schematic (LVS) checks of analog, mixed-signal, RF and MEMS ICs.The system modelling has been carried out using the features of the software involving the feature of S-Edit which helps to capture schematic blocks, T-Spice feature enables the user to perform the simulation of the designed circuit and W-Edit feature of the software to generate the waveforms of logic operations and power consumption of the design. Details of the features of the software and its usage can be found in ref.[13].

V. RESULTS &DISCUSSION

Results of the simulated models for the domino logic based circuits in ref [10] and the proposed model in this research work are presented here. The comparison of the two circuits is based on the performance parameters of power, delay and PDP for simulation study carried out. The findings are presented in table I. The results indicate that the performance of the proposed methodology is better. In terms of power consumption, there is improvement in this value by 74%, while the delay time is improved by 30% and the PDP is improved by 80%.

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Table I. Comparison of performance between proposed circuit and ref.[10]

Design parameter	Domino logic circuit as proposed by Shiksha et.al. [10]	Proposed domino logic	Percentage reduction in designed parameter
Supply Voltage(V)	1 V	1 V	1 V
Power(uW)	335.05	87.037	74%
Delay(ns)	172.88	120.88	30%
PDP(10^{-18} j)	57.922	10.521	81.83

To test the performance of the methodology proposed, simulation studies were carried out using different values of supply voltage. The results indicate that the proposed model is able to give significant improvement in the performance parameters even on changing the supply voltage. This is reported in table II.

The impact of the variation of the size of the NMOS transistor on the power delay product is a key parameter when dealing with domino logic based circuits. To test the consistency in its performance, the width of the NMOS was varied between 180 nm to 480 nm with a variation of size of 60 nm in each step. The results of the PDP for the proposed circuit and earlier work are shown in fig. 5. The results indicate that the performance of the proposed methodology outweighs earlier reported work on domino logic based circuits.

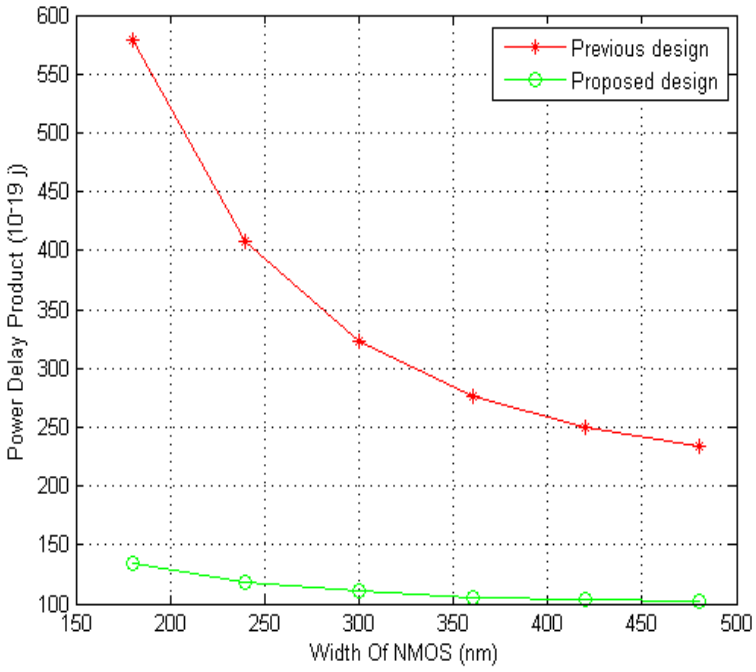

Fig. 9: Variation in Power Delay Product (PDP)with the width Of NMOS transistor for current model and ref.[10]

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Table II. Comparison of performance between proposed wort and ref.[10] for different supply voltages

Supply Voltage	1V		0.9V		0.8V		0.7V		0.6V	
Design Parameter	Work in ref [10]	Proposed Work	Work in ref [10]	Proposed Work	Work in ref [10]	Proposed Work	Work in ref [10]	Proposed Work	Work in ref [10]	Proposed Work
Power (nw)	335.05	87.037	121.61	68.566	179.77	53.461	73.665	40.819	72.933	30.256
Delay (ps)	172.88	120.88	245.59	173.22	441.19	302.20	867.73	628.76	2046.9	1338.4
PDP (10^{-18} j)	57.922	10.521	29.867	11.877	79.312	16.156	63.921	25.666	149.28	40.495

VI.CONCLUSION

In recent times the decreasing technology trends demand circuitry which consume less power and gives less delay Domino logic is very useful scheme used in digital circuit for to fulfil the requirement of reduction of power and. In this research work a proposed methodology has been presented for domino logic based circuits for use in digital and electronic applications. Tanner EDA tool was used to simulate the proposed design using IBM 90nm technology. The proposed design is compared with previous reported works and it has been observed form the simulated study that the presented methodology consumes less power, less delay which results in the reduction of the PDP of the circuit as well. Successful implementation of the proposed methodology has potential of use it in design of full adder circuits,multiplexer, and similar applications.

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