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Design of Low Power High Speed Dynamic Comparator

N.Gowtham Kumar[1], B.Srinivas[2]

PG Student [VLSI], Dept. of ECE, MVGR College of Engineering (A), Vizianagaram, Andhra Pradesh, India[1]

Assistant Professor, Dept. of ECE, MVGR College of Engineering (A), Vizianagaram , Andhra Pradesh, India[2]

ABSTRACT:In this paper, a high-speed low-power two-stage dynamic latched comparator is proposed. In this proposed circuit the first stage power consumption is lessen by limiting the pre-amplifier's voltage swing to Vdd/2 At the evaluation phase, voltage swing constraint provides a vigorous drive which improves comparison speed.. It is shown that in the proposed dynamic latched comparator have less dissipated power and time delay. The proposed dynamic latched comparator reduced the power and delay compared to conventional CMOS comparators. Finally the comparator mentor graphics simulation at the 130nm gives significant improvement in the power and delay.

KEYWORDS: Two stage dynamic comparator, window detector, low power applications.

I.INTRODUCTION

All After Op Amp comparators are mostly used electronic component because they play an important role in ADC's. Comparators are also called as 1-bit A/D convertor. In past Static comparators are used but they are low speed and a large amount of power consumption, due these drawbacks this type of comparator are not applicable for the portable devices. The drawbacks of the static comparator are overcome using dynamic comparator. Initially come up with single-stage dynamic comparators, to increase speed and to reduce the power consumption. But these comparators are suffers with kick back noises which is caused due to the capacitive path formed between output and input. Two-stage dynamic latched comparators are introduced, the drawback of the one-stage dynamic comparator are overcome. To attain the given offset the two-stage dynamic comparator's transistor at the input side are chosen large. There will be larger parasitic capacitance at the output terminal of the first stage of comparator because of using large transistor at input. Due to this power consumption influences offset, as power consumption reduces offset increases. There are number of techniques have been proposed to reduce power dissipation and increase speed. Advantages and disadvantages of each technique are explained below.

A conventional two-stage dynamic comparator [13] is high speed, but to achieve low offset voltage transistor size is increase as a result the power consumption is increase. So this conventional two-stage comparator is not suitable for low power applications.

In [7] a two stage comparator which works only with one clock phase. In this low offset voltage is achieved by using time domain tuned offset cancelation technique is deployed. Smaller transistors are used due to low offset voltage, so the power consumption will reduce. But speed of the comparator is limited due these techniques.

In [6] also two-stage dynamic comparators with different structure which have higher speed but larger power consumption. Power dissipation is large for all these comparators. The proposed two-stage dynamic comparator structure has less stacking and faster latching.

The paper is systemized as follows. Section 2 explores about the dynamic-latch comparator, new dynamic comparator architecture and its operation is described in Section 3. Section 4 discusses the architecture of window detector. Simulation results and conclusion are provided in Section 5 and Section 6 respectively.

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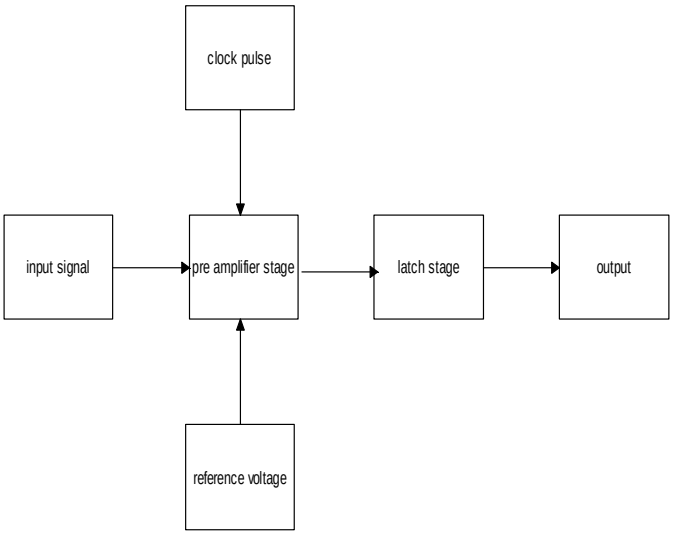

Fig. 1 block diagram of dynamic latched comparator.

II.CLASSIFICATION OF COMPARATOR

Comparators are classified into various types. Those are described below.

A. Static Latched Comparators

The first classification is static latched comparator. An example of static latched comparator is shown in below figure 2. The common characteristics of the static latched comparator are summarized as

- By the two class-A cross coupled inverters ($M_{3a}/M_{4a}$and M_{3b}/M_{4b}) regeneration process is done. But the regeneration process is slow due to current limited operation by the class A cross coupled inverter. Because of the consumption is purely static, power efficiency is poor.
- A differential pair which acts as preamplifier, the output current of this preamplifier is mirrored or injected in the regenerative nodes through the cascade transistor. Kickback noise reduced by this isolation. But it introduces two poles at intermediate node and regeneration nodes respectively.

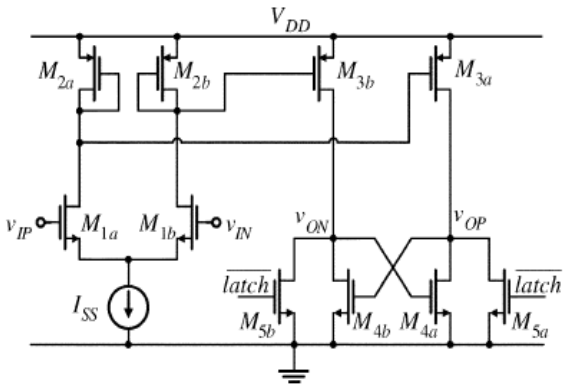

Fig. 2 Static latched comparator

In practical, these latched comparators are not used due to the process of regeneration is slow and static power.Even though a low kickback noise is presented.

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B. Class-AB latched comparators

Second type is Class-AB latched comparator, speed limitation problem of above latched comparator is achieved by this type of comparator. Example of Class-AB latched comparator is shown in figure 3. Common characteristics are as follows.

- Cross coupled CMOS inverters will do regeneration process. The output nodes are charged faster by momentarily increase of current during the regeneration process.
- There will be one pole exists in this type of comparator because there is no isolation between input differential pair drains and regeneration nodes, so it reacts quickly to the input variations. However kick back noise is increases due to the rail to rail signals at nodes which are coupled to inputs.

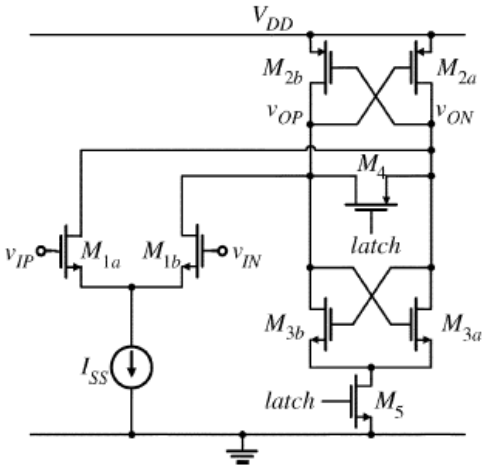

Fig. 3 Class AB latched comparator

Even though it is fast and power efficientwhen compared to static comparator, it not used because more kick back noise isthe drawback of these comparators.

C. Dynamic comparators

Class AB latched comparator is more power efficient, still it uses supply current during reset phase.Dynamic comparators are also called as clocked comparators.A regenerative feedback is used in dynamic comparators to achieve low power, high speed, full output swing and high gain. Power is consumed during the evaluation phase.Speed of the dynamic comparators is very high and the power dissipation is low.

III.TWO STAGE DYNAMIC COMPARATORS

The dynamic comparator[2] shown in figure4 is a conventional one, when the clock is set high M18, M8, M11,M12 AND M14 are turned on, and M5-M10 pmos transistor are turned off. M17 is connected to one of the input pair, it conducts a constant current which intentionally create a additional offset voltage. This conventional comparator is high speed but it stable only under small disturbances.

Another type of comparator [1] is shown in figure5. It consists of two stages: preamplifier stage and latch stage. Before to start comparison, the comparator state is reset to discharge the output node of preamplifier and latch stage to ground and VDD respectively. In next phase the evaluation phase clock to 0 and clockbar to 1 to start comparison. The output of the preamplifier increases, when the output voltage of preamplifier stage is approach the gate voltage of input NMOS transistor of latch, the latch stage of the comparator is activated. To control offset, the input transistors' size are increased. But large size transistor increases the power consumption. Due to this comparator is not suitable of low power high resolution applications.

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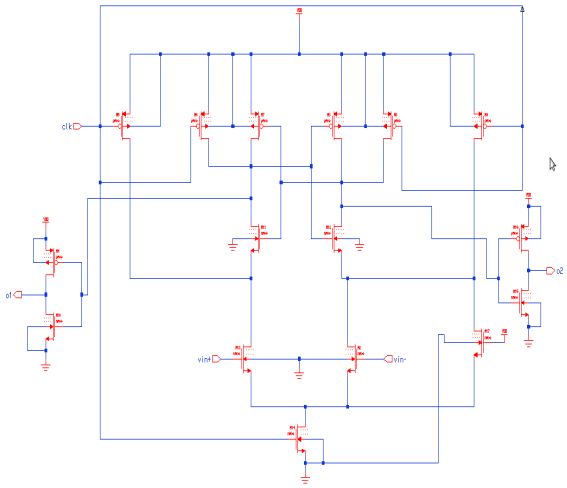

Fig. 4conventional dynamic comparator

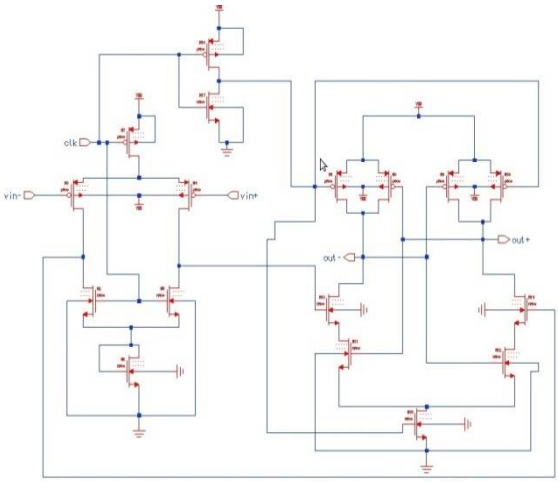

Fig. 5 comparator 2

IV.PROPOSED COMPARATOR

The proposed comparator is shown in figure6. This comparator can be operated at lower voltage because this circuit has less stacking. Independent on common mode voltage, the M12 transistor conducts larger current, which provide speed to comparator. Initially, the comparator state is reset. During the resetphase clk = 0 the output node voltage of preamp are discharged to vdd\2. M1, M8 transistor will turn on, and output discharges to ground(0).

After reset phase clk is vdd, the first stage output voltage starts growing gradually. Magnitude of input differential voltage affects the growth rate of output voltage of first stage. When it reaches threshold voltage of the NMOS transistors' (M7, M8), the latch stage is activated. An additional shield is formed between input and output by the cross coupled transistor. This provides less kickback noise.Output waveform and layout of the comparator are shown in below figure 7 figure 8 respectively.

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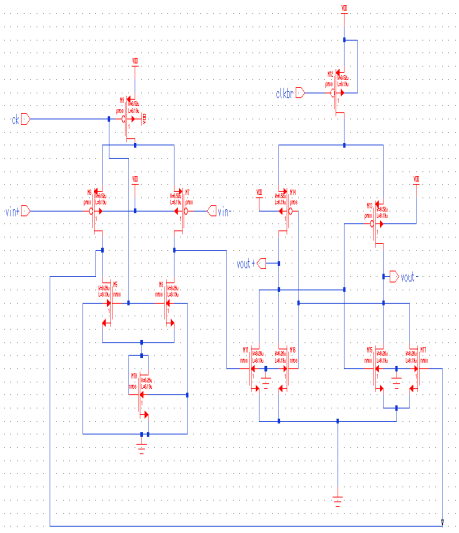

Fig. 6 proposed dynamic comparator

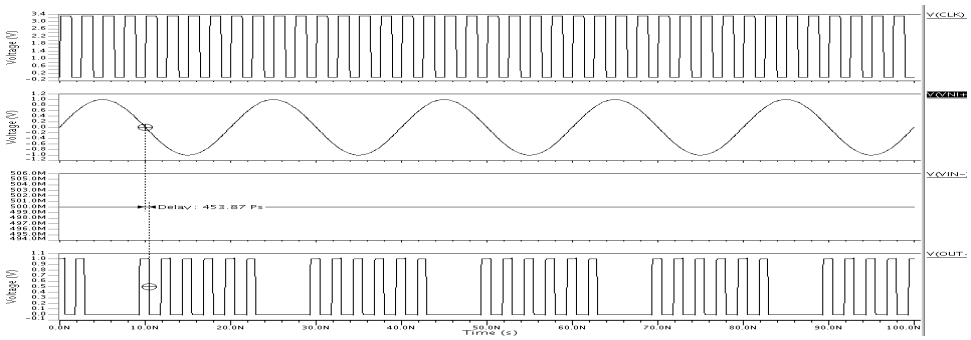

Fig. 7 waveform of the proposed comparator

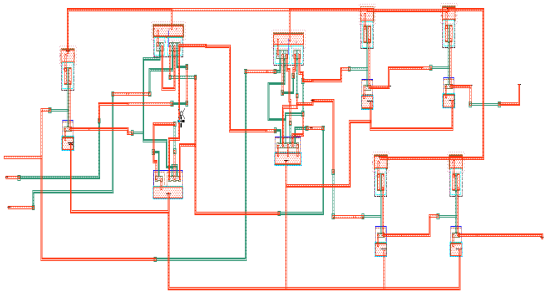

Fig.8 layout of proposed comparator

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V.APPLICATION

Window Detector:

Window detector is also called as window comparator or dual edge limit detector. It has two precise reference voltages, an upper limit and a lower limit. If vin is the input voltage, v1 is upper limit and v2 is lower limit, whenever the vin is between the v1 and v2 output will obtain. Window detector consists of two comparators, output of the two comparator are connected to two inputs AND gate.

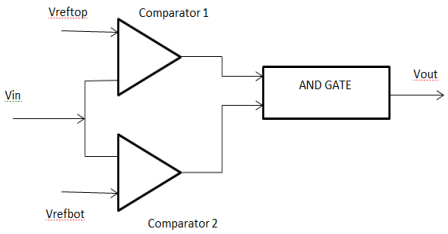

Fig. 9 block diagram of window detector

Window detector is employed in a varity of applications. Window detector is used as input stage for low power SAR ADC in biomedical applications, industrial alarms, level sensor. The waveform of window detector is shown below whenever the input is lies between the two limit the output will follow the clock.

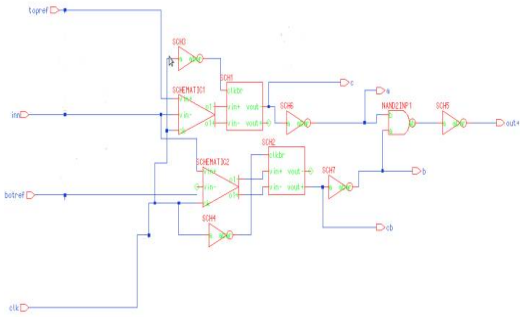

Fig. 10 schematic of the window detector

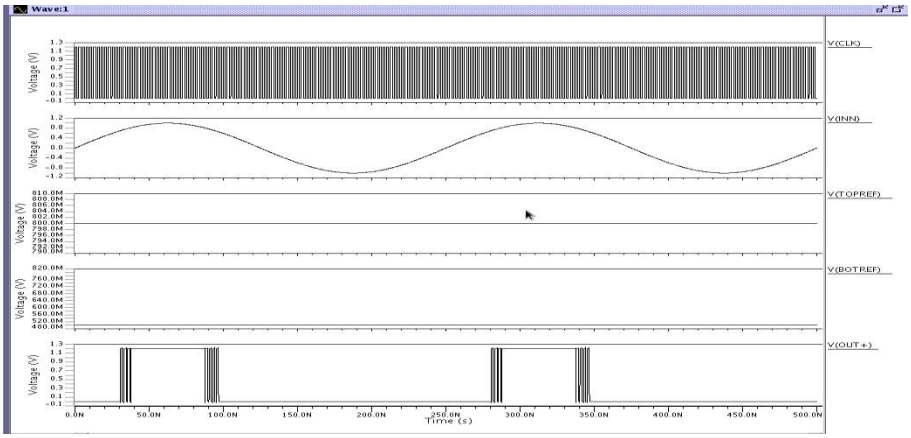

Fig. 11 waveform of window detector

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In output wave form of the window detector is shown in the figure 11. We can observe that the output follows the clock when the input wave form is between the top reference value and bottom reference value. Figure 12 shown below is the layout of the window detector.

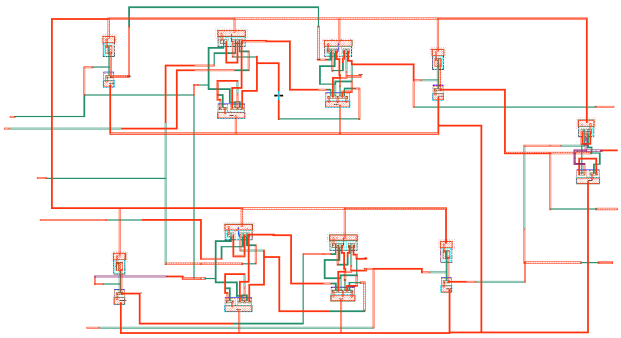

Fig. 12 layout of window detector

VI.SIMULATION RESULTS

The proposed comparator 130nm CMOS dynamic latch comparator and existing dynamic latch comparators are design and simulated in mentor graphics with 1V supply. Comparing the proposed and other comparators are tabulated below table1. Table 2 summarizes the performance of the window detector implemented using proposed comparator.

Table 1: comparison table of proposed comparator with other comparator.

Specification	**Comparator -1**	**Comparator -2**	**Proposed comparator**
Technology	130nm	130nm	130nm
Supply voltage	1V	1V	1V
Number of transistors	16	15	13
Delay	5.2974ns	948.85ps	453.2ps
Power dissipation	1.8497nw	4.9153nw	1.7995n

Table 2: performance of window detector.

Specification	**Window detector**
Technology	130nm
Supply voltage	1V
Delay	30.6ns
Power dissipation	8.874nwatts

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VII.CONCLUSION

In this work, a two stage dynamic comparator has been proposed for low swing application. From the simulation results it has power dissipation of 1.7995nwatts and delay of 453.2ps The simulated results imply that proposed comparator achieves low power consumption and less delay. The performance of window detector is also increased by using the proposed comparator.

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