



# **An Adjustable Speed Control of BLDC Motor Using Bridgeless Buck–Boost Converter with Fuzzy Logic Controller**

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**ABSTRACT:** This paper presents a bridgeless (BL) buck–boost converter-fed brushless direct current (BLDC) motor drive as a cost-effective solution for low-power applications. An approach of speed control of the BLDC motor by controlling the dc link voltage of the voltage source inverter (VSI) is used with a single voltage sensor. This will make the VSI operation at fundamental switching by means of electronic communication of BLCD motor with reduced switching losses. A BL configuration of the buck–boost converter is proposed which offers the elimination of diode bridge rectifier thus reducing the conduction losses those are associated with it. The performance of proposed drive is evaluated over a wide range of speed control and varying supply voltages and MATLAB/Simulink environment is used to simulate the proposed drive.

**KEYWORDS:** Bridgeless (BL) buck–boost converter, brushless direct current (BLDC) motor, discontinuous inductor current mode (DICM), power factor corrected (PFC), power quality

## **I.INTRODUCTION**

The major constrains in the development of low-power motor drives for household applications such as fans, water pumps, blowers, mixers, etc are EFFICIENCY and COST. The use of the brushless direct current (BLDC) motor in these applications is becoming very common due to wide range of features which includes high efficiency, high flux density per unit volume, low maintenance requirements, and low electromagnetic-interference problems. These BLDC motors are not only limited to household applications, but also suitable for other applications such as medical equipment, HVAC, transportation, motion control, and many industrial tools. In recent years, energy efficiency has become an important aspect of designing any electrical drive system due to the scarcity of the energy resources. The selection of a motor for a particular drive application is the foremost task and it's depends on variety of parameters such as high efficiency, compact size and good performance over a wide range of speed control.

A BLDC motor contains three phase windings on the stator and permanent magnets on the rotor. The BLDC motor is also known as an electronically commutated motor because an electronic commutation based on rotor position is used rather than a mechanical commutation which has disadvantages like sparking and wear and tear of brushes and commutator assembly.

The prominent feature which makes Brushless DC Motors different from conventional DC motor is the substitution of electrical commutation system with the mechanical self-commutating analogy. To implement the electronic commutation for a three phase BLDC motor, a three-phase full-bridge inverter consisting of six electronic switches is required. At this stage, having an electronic commuted BLDC motor, it becomes easers to take control of the motor characteristics.

Basically, two usual applicable methods namely Pulse Width Modulation (PWM) and Space Vector Modulation (SVM) are used to control the motor. In this paper, the PWM method is applied to modulate a control reference signal on a high frequency triangular waveform in order to modify the average voltages given to the motor. Brushless direct current motors (BLDC) are rapidly gaining popularity due to the absence of brushes in BLDC motor as the name implies and investigating electronic commutation systems rather than mechanical analogy. In addition, they have high efficiency, reliability and require very less maintenance. Furthermore, BLDC motors have several advantages over the

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conventional brushed DC motors such as higher torque-weight ratio, high dynamic response and better speed vs. torque characteristics.

BLDC motors are nowadays used in every sector of market, especially in the areas of appliances production, aeronautics, medicine, consumer and industrial automations. The BLDC motors are kind of permanent magnet synchronous motors (PMSM), which are driven by commutated direct current (DC) voltage.

Power quality problems have become important issues to be considered due to the recommended limits of harmonics in supply current by various international power quality standards such as the International Electro technical Commission (IEC). A BLDC motor when fed by a diode bridge rectifier (DBR) with a high value of dc link capacitor draws peaky current which can lead to a THD of supply current of the order of 65% and power factor as low as 0.8. Hence, a DBR followed by a power factor corrected (PFC) converter is utilized for improving the power quality at ac mains.

## II. LITERATURE SURVEY

Several research papers are proposed and published on BLDC motors some of them are as follows:

A buck–boost converter feeding a BLDC motor based on the concept of constant dc link voltage and PWM-VSI for speed control which has high switching losses is proposed by Singh and Singh.

Gopalathnam and Toliyat proposed a single-ended primary-inductance converter (SEPIC)-based BLDC motor drive, it is a higher number of current and voltage sensors but it has higher losses in VSI due to PWM switching which restricts its applicability in low-cost application.

Singh and Singh have proposed a Cuk converter-fed BLDC motor drive with the concept of variable dc link voltage which reduces the switching losses in VSI due to the fundamental switching frequency operation for the electronic commutation of the BLDC motor and it also the speed by controlling the voltage at the dc bus of VSI.

A CCM operation of the Cuk converter has been utilized, it requires three sensors but it has low cost and low power rating. For further improvement in efficiency, bridgeless (BL) converters are used which allow the elimination of DBR in the front end.

A buck–boost converter configuration is best suited among various BL converter topologies for applications requiring a wide range of dc link voltage control (i.e., bucking and boosting mode). Jang and Jovanovic and Huber *et al.* have presented BL buck and boost converters, respectively.

These can provide the voltage buck or voltage boost which limits the operating range of dc link voltage control.

Wei *et al.* have proposed a BL buck–boost converter which uses three switches which is not a cost-effective solution.

A new family of BL SEPIC and Cuk converters has been reported in the literature but requires a large number of components and has losses associated with it.

This paper presents a BL buck–boost converter-fed BLDC motor drive with variable dc link voltage of VSI for controlling the speed. Here speed is controlled by varying DC link voltage of VSI and by using PI controller it operates in Discontinuous inductor current mode to improve powerfactor at ac mains.

## III. PROPOSED BRIDGELESS BUCK BOOST CONVERTER FED BLDC MOTOR DRIVE

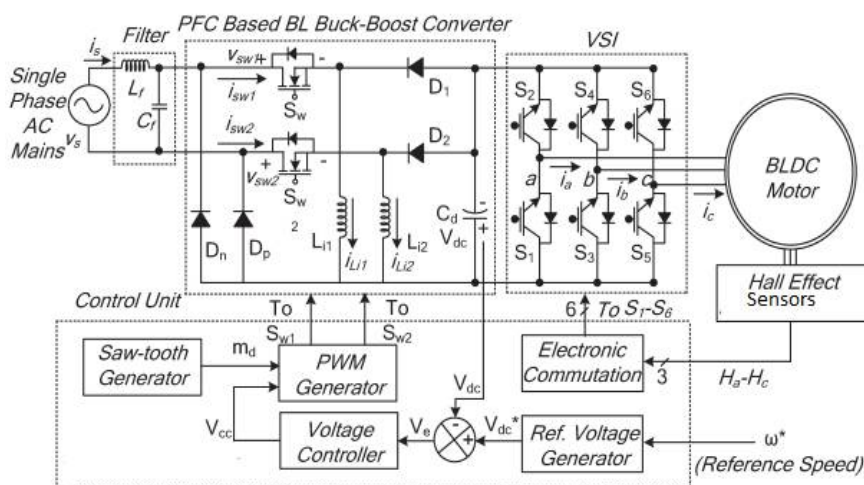


Fig 1. Block diagram of proposed system

Fig.1 shows the proposed concept of **BL buck–boost converter** based VSI fed BLDC motor drive. It generally operates in discontinuous inductor current mode(DCIM) for Power factor correction. Speed control is done by using Brushes buck-boost converter. This drive is used for wide ranger of speed control with improved power quality at Ac mains.

## OPERATION:

### Operating principle of Bridgeless buck–boost converter:

The operation of the PFC BL buck–boost converter is classified into two parts which include the operation during the positive and negative half cycles of supply voltage and during the complete switching cycle.

#### a) Operation During Positive and Negative Half Cycles of Supply Voltage:

During the positive half cycle of the supply voltage, switch  $S_{w1}$ , inductor  $L_{i1}$ , and diodes  $D_1$  and  $D_p$  are operated to transfer energy to dc link capacitor  $C_d$  as shown in Fig. 2(a)–(c). Similarly, for the negative half cycle of the supply voltage, switch  $S_{w2}$ , inductor  $L_{i2}$ , and diodes  $D_2$  and  $D_n$  conduct as shown in Fig. 3(a)–(c). In the DICM operation of the BL buck–boost converter, the current in inductor  $L_i$  becomes discontinuous for a certain duration in a switching period Fig. 2(d) shows the waveforms of different parameters during the positive and negative half cycles of supply voltage.

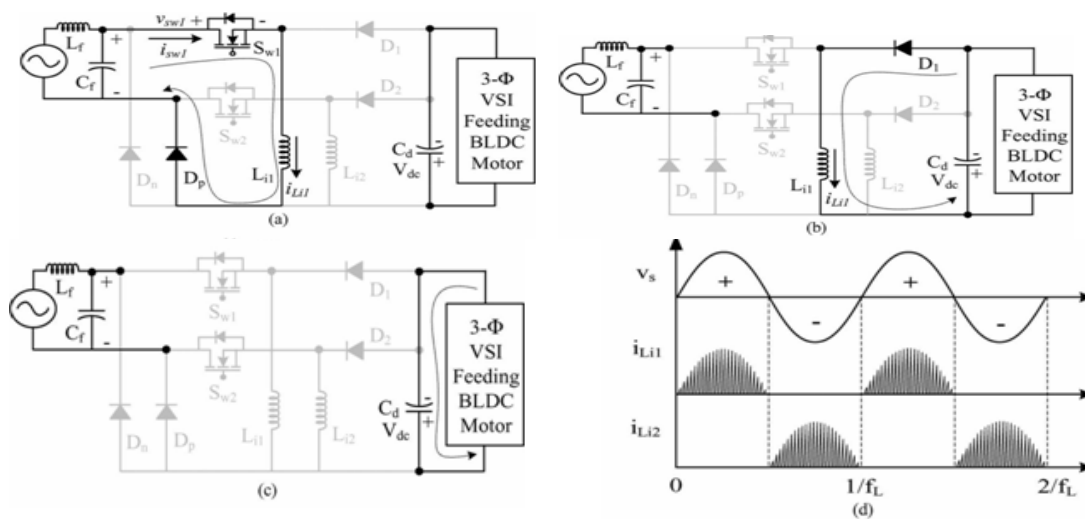


Fig.2 Operation of the proposed converter in different modes (a)–(c) for a positive half cycle of supply voltage and (d) the associated waveforms. (a) Mode I. (b) Mode II. (c) Mode III. (d) Waveforms for positive and negative half cycles of supply voltage.

#### b) Operation during Complete Switching Cycle

Three modes of operation during a complete switching cycle are discussed for the positive half cycle of supply voltage as shown hereinafter.

**Mode I:** In this mode, switch  $S_{w1}$  conducts to charge the inductor  $L_{i1}$ ; hence, an inductor current  $i_{L_{i1}}$  increases in this mode as shown in Fig. 2(a). Diode  $D_p$  completes the input side circuitry, whereas the dc link capacitor  $C_d$  is discharged by the VSI-fed BLDC motor as shown in Fig. 3(d).

**Mode II:** As shown in Fig. 2(b), in this mode of operation, switch  $S_{w1}$  is turned off, and the stored energy in inductor  $L_{i1}$  is transferred to dc link capacitor  $C_d$  until the inductor is completely discharged. The current in inductor  $L_{i1}$  reduces and reaches zero as shown in Fig. 3(d).

**Mode III:** In this mode, inductor  $L_{i1}$  enters discontinuous conduction, i.e., no energy is left in the inductor; hence, current  $i_{L_{i1}}$  becomes zero for the rest of the switching period. As shown in Fig. 2(c), none of the switch or diode is conducting in this mode, and dc link capacitor  $C_d$  supplies energy to the load; hence, voltage  $V_{dc}$  across dc link capacitor  $C_d$  starts decreasing. The operation is repeated when switch  $S_{w1}$  is turned on again after a complete switching

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cycle. Similarly, for the negative half cycle of the supply voltage, switch  $S_{w2}$ , inductor  $L_{i2}$ , and diodes  $D_n$  and  $D_2$  operate for voltage control and PFC operation.

## IV DESIGN F BL BUCK–BOOST CONVERTER:

A PFC BL buck–boost converter is designed to operate in DICM such that the current in inductors  $L_{i1}$  and  $L_{i2}$  becomes discontinuous in a switching period.

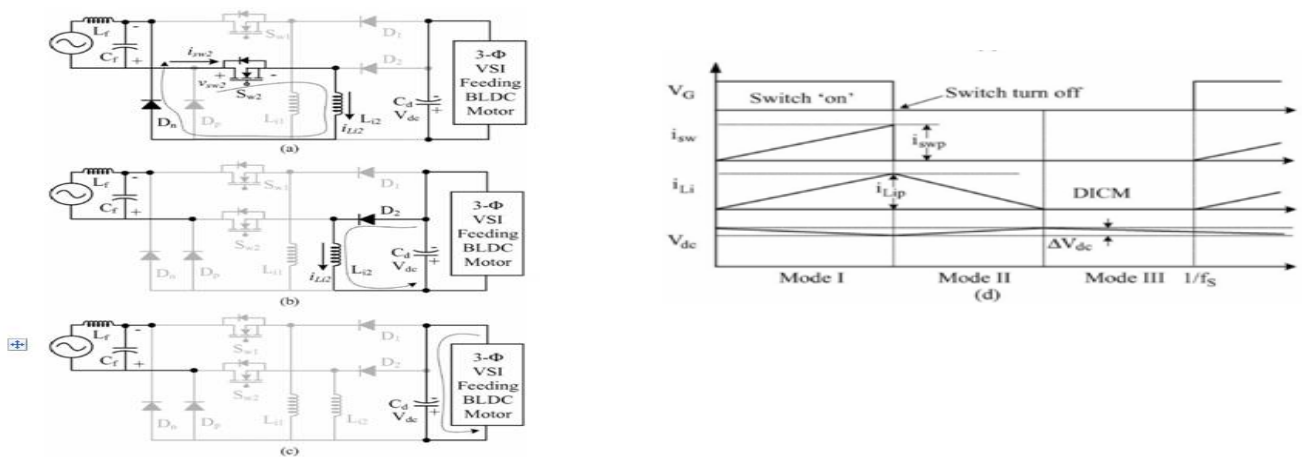


Figure.3 Operation of the proposed converter in different modes (a)–(c) for a negative half cycle of supply voltage and (d) the associated waveforms.(a) Mode I. (b) Mode II. (c) Mode III. (d) Waveforms during complete switching cycle.

For a supply voltage of 220V(RMS value),the Dc voltage appears at the input side is nearly 198V

$$V_{in} = \frac{2\sqrt{2}V_s}{\pi} \quad (1)$$

For a Buck-Boost converter the duty ratio is

$$d = \frac{V_{dc}}{V_{dc} + V_{in}} \quad (2)$$

Generally this converter is designed for DC Voltage limits of 50 volts to 100 volts only with an average value of 100v.so the minimum and maximum values of duty ratio are 0.2016,0.5025 respectively.

### A.Design of input inductors( $L_{i1},L_{i2}$ )

For a BUCK-BOOST converter to operate in critical conduction mode  $L_{i1} = \frac{R(1-d)^2}{2f_s}$  (3)

Where R is equivalent total resistance,d is Duty ratio, $f_s$  is switching frequency.

The  $L_{i1}$  is calculated at minimum d value it means for minimum operating voltage of 50v and minimum power of 90w

### B. Design of dc link capacitor( $c_d$ )

The design of the dc link capacitor is governed by the amount of the second-order harmonic (lowest) current flowing in the capacitor and is derived as follows.  $C_d = \frac{I_d}{2\omega\Delta V_{dc}}$  (7)

Now, the value of the dc link capacitor is calculated for the designed value  $V_{dc}$  des with permitted ripple in the dc link

voltage ( $\Delta V_{dc}$ ) taken as 3% as  $C_d = \frac{I_d}{2\omega\Delta V_{dc}} = \frac{P_0/V_{dc}}{2\omega\Delta V_{dc}}$  (8)

Hence, the nearest possible value of dc link capacitor  $C_d$  is selected as 2200  $\mu F$ .



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## C.Design of Input Filter ( $L_f$ and $C_f$ ):

A second-order low-pass LC filter is used at the input side to absorb the higher order harmonics such that it is not reflected in the supply current. The maximum value of filter capacitance is given as  $C_{max} = \frac{I_{peak}}{\omega_L V_{peak} \tan \phi}$  (9)

Where  $I_{peak}$ ,  $V_{peak}$ ,  $\omega_L$ , represent the peak value of supply current, peak value of supply voltage, line frequency in radians per second, and displacement angle between the supply voltage and supply current, respectively. Hence, a value of  $C_f$  is taken as 330 nF. Now, the value of inductor  $L_f$  is calculated as follows. The value of the filter inductor is designed by considering the source impedance ( $L_s$ ) of 4%–5% of the base impedance. Hence, the additional value of inductance required is given as

$$L_f = L_{req} + L_s = \frac{1}{4\pi^2 f_c^2 C_f} = L_{req} + 0.04 \left( \frac{1}{\omega_L} \right) \left( \frac{V_s^2}{P_0} \right) \quad (10)$$

where  $f_c$  is the cutoff frequency  $f_l < f_c < f_{sw}$

Hence, a value of  $f_c$  is taken as  $f_{sw}/10$ . Finally, a low-pass filter with inductor and capacitor of 1.6 mH and 330 nF is selected for this particular application.

## V. CONTROL OF BL BUCK–BOOST CONVERTER-FED BLDC MOTOR DRIVE

The control of the PFC BL buck–boost converter-fed BLDC motor drive is classified into two parts as follows.

### a) Control of Front-End PFC Converter:

#### Voltage Follower Approach:

The control of the front-end PFC converter generates the PWM pulses for the PFC converter switches ( $Sw_1$  and  $Sw_2$ ) for dc link voltage control with PFC operation at ac mains. A single voltage control loop (voltage follower approach) is utilized for the PFC BL buck–boost converter operating in DICM. A reference dc link voltage ( $V_{dc}^*$ ) is generated as

$$V_{dc}^* = k_v w^* \quad (11)$$

Where  $k_v$ ,  $w^*$  are the motor's voltage constant and the reference speed, respectively.

The voltage error signal ( $V_e$ ) is generated by comparing the reference dc link voltage ( $V_{dc}^*$ ) with the sensed dc link voltage ( $V_{dc}$ ) as

$$V_e(k) = V_{dc}^*(k) - V_{dc}(k) \quad (12)$$

Where  $k$  represents the  $k$ th sampling instant. This error voltage signal ( $V_e$ ) is given to the voltage proportional–integral (PI) controller to generate a controlled output voltage ( $V_{cc}$ ) as

$$V_{cc}(k) = V_{cc}(k-1) + k_p \{V_e(k) - V_e(k-1)\} + k_i V_e(k) \quad (13)$$

where  $k_p$  and  $k_i$  are the proportional and integral gains of the voltage PI control.

Finally, the output of the voltage controller is compared with a high frequency saw tooth signal ( $m_d$ ) to generate the

PWM pulses as For  $v_s > 0$ ; { if  $m_d < v_{cc}$  then  $s_{w1}$ ='ON' and if  $m_d \geq v_{cc}$  then  $s_{w1}$ ='OFF' }

For  $v_s < 0$ ; { if  $m_d < v_{cc}$  then  $s_{w2}$ ='ON' and if  $m_d \geq v_{cc}$  then  $s_{w2}$ ='OFF' }

where  $Sw_1$  and  $Sw_2$  represent the switching signals to the switches of the converter

### b) Control of BLDC Motor: Electronic Commutation:

An electronic commutation of the BLDC motor includes the proper switching of VSI in such that symmetrical dc current is drawn from the dc link capacitor for 120° and placed symmetrically at the center of each phase. A Hall effect position sensor is used to sense the rotor position on a span of 60°, which is required for the electronic commutation of

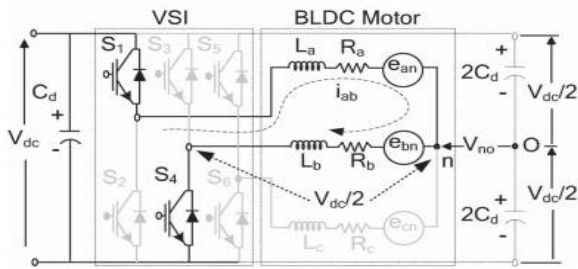
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the BLDC motor. The conduction states of two switches (s1 and s4). A line current  $i_{ab}$  is drawn from the dc link capacitor whose magnitude depends on the applied dc link voltage.



$\Theta^\circ$	Hall Signals			Switching States					
	$H_a$	$H_b$	$H_c$	$S_1$	$S_2$	$S_3$	$S_4$	$S_5$	$S_6$
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-180	0	1	1	0	0	1	0	0	1
180-240	1	0	0	0	0	0	1	1	0
240-300	1	0	1	1	0	0	1	0	0
300-360	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

Table 1: switching states for achieving electronic commutation of BLDC motor based on hall-effect position signals

## VI. SIMULINK CIRCUIT AND RESULTS

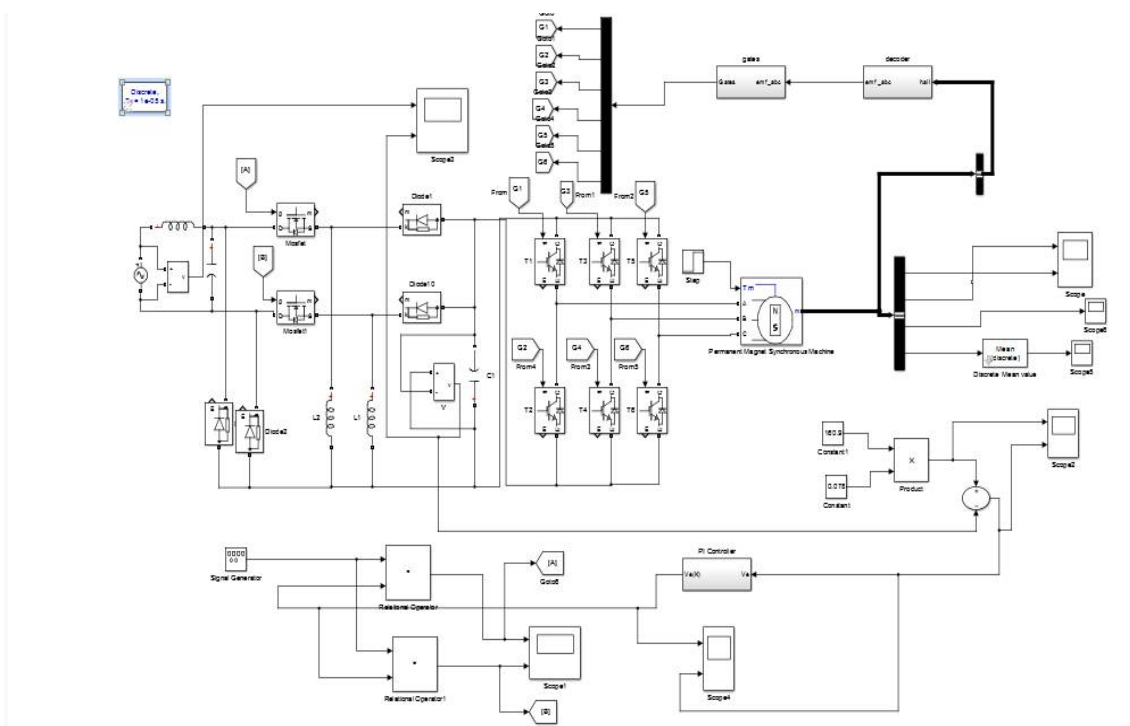


Fig 4: Simulink Circuit of Proposed system

**a) SUB CIRCUIT (DECODER):**

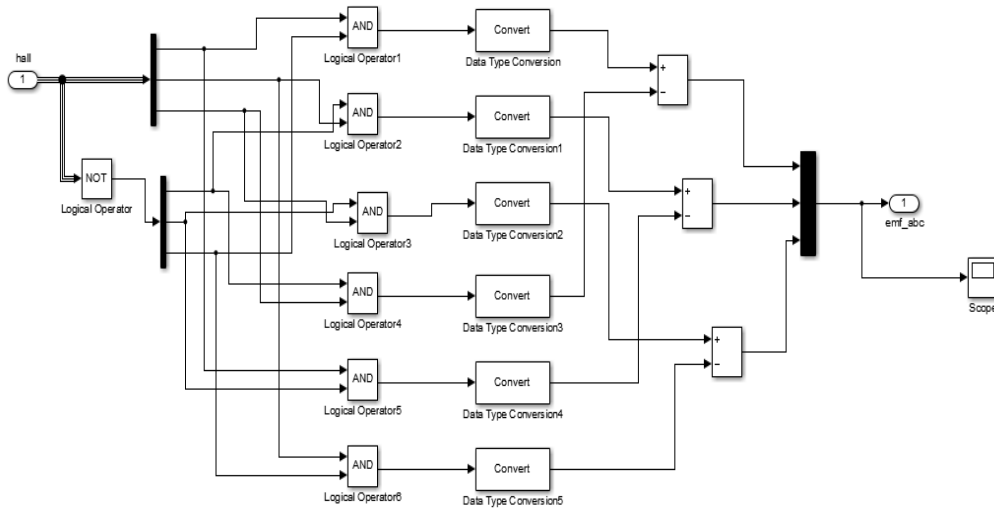


Fig 5: Simulink circuit of decoder

**b. SUB CIRCUIT (GATES):**

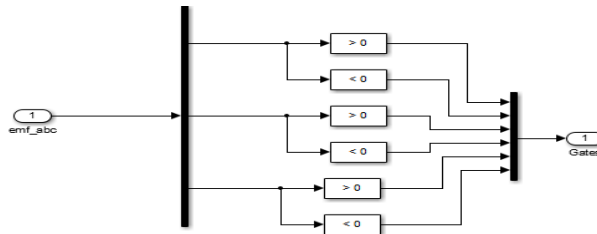
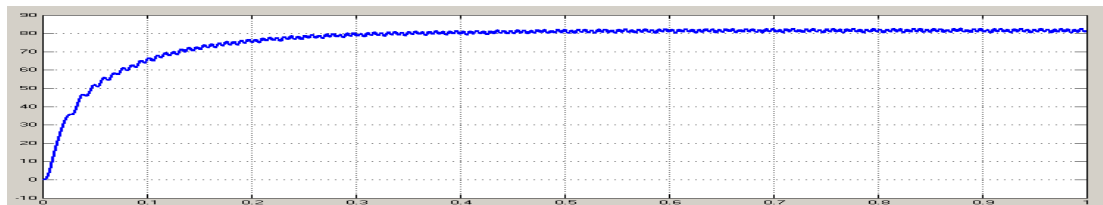


Fig 6: Simulink circuit of Gates block

**RESULTS:**

**Speed Vs time:**



**DC link Voltage Vs time:**

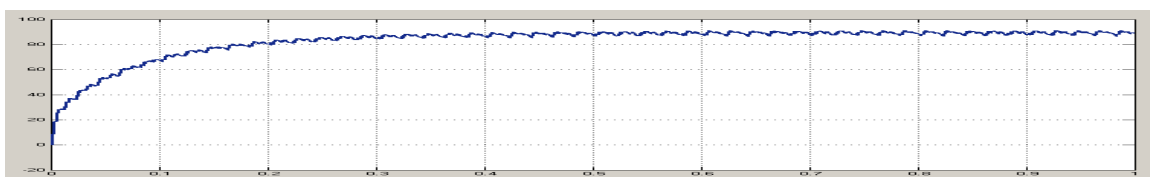


Fig 7: Simulation results of proposed system with PI controller

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**Table 2: Variation of DC Link Voltage and Speed with Reference Voltage:**

Vref(v)	0.5	1	2	5	10	20
Vdc(V)	65	70	80	120	120	150
Speed(rpm)	477	620	625	630	650	670

### EXTENSION:Fuzzy Controller:

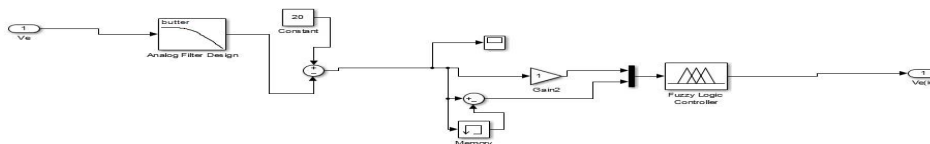
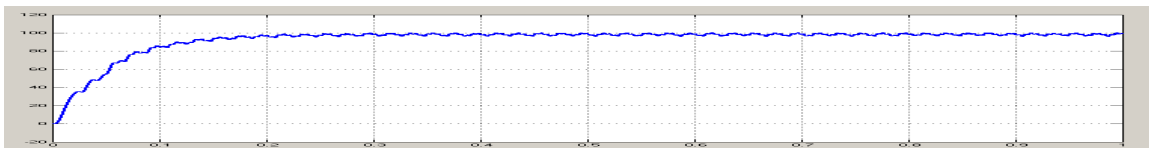


Fig 8 Simulink model of FLC

### Speed Vs time:



### DC link Voltage Vs time:

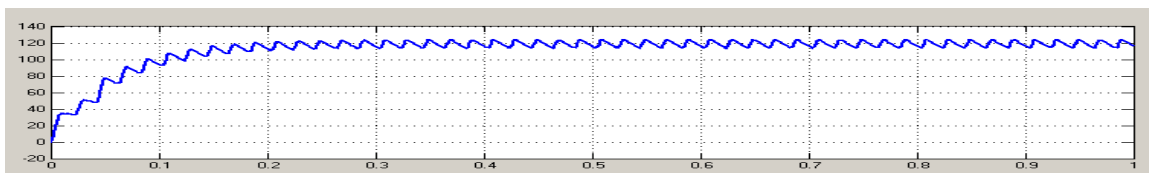


Fig 9 Simulation results of proposed converter with FLC

**Table 3: Comparison between PI and Fuzzy Controller**

s.no	Type of controller	Rise Time	Settling Time	Overshoot	Under shoot	Peak
1	PI	1.45	2.97	134.69	0	115
2	Fuzzy	0.8	1.98	16.16	0	115

### VILCONCLUSION

A BL buck–boost converter-based VSI-fed BLDC motor drive has been proposed for low-power applications. A new method of speed control has been utilized by controlling the voltage at dc bus .In this proposed scheme operating the VSI at fundamental frequency for the electronic commutation of the BLDC motor is proposed for reducing the switching losses in VSI. Fuzzy Controller is used instead of PI Controller for wide range speed control of BLDC motor. The proposed scheme has shown satisfactory performance, and it is a recommended solution applicable to low-power BLDC motor drives.





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