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A Comparative Analysis on PV fed Seven Level CHB and NPC Converters using MPPT Technique for Low Power Applications

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ABSTRACT: With the advent of efficient DC to DC and DC to AC converters, the performance of standalone and grid connected photovoltaic systems has been improved upto a great extent. Due to the considerably gaining popularity of photovoltaic systems among other renewable resources, power electronic device interface have become an essential key element. This paper describes the comprehensive analysis of seven level cascaded H-bridge (CHB) and neutral point clamped (NPC) multilevel inverters with boost converter using maximum power point tracking algorithm. Maximum power point tracking technique in the photovoltaic systems is implemented using perturb and observe (P&O) to obtain optimal output of PV array by continuously tracking along the maximum power point (MPP). The simulation study has been carried out under MATLAB/Simulation environment.

KEYWORDS: multilevel inverters, cascaded H-bridge, neutral point clamped, maximum power point tracking, photovoltaic cell.

I. INTRODUCTION

The photons carrying the energy of sunlight incident on photovoltaic array is converted into electrical energy. The output power of PV array is capable enough to feed the light loads such as lighting systems and DC motors. However, sensitive and sophisticated applications demand for power electronic converters to process the power output of array. The converters regulate the voltage and current at the load terminal and hence operate the array at maximum power in the grid connected systems [2-3]. The converters equipped with maximum power point tracking (MPPT) technique is based on an algorithm which keeps on detecting the maximum instantaneous power of the PV array. Since the operating point of the array vary intermittently, so the MPPT algorithm is required to set the operating point so as to extract and deliver maximum instantaneous power to the ac load through multilevel inverters [8]. The key advantage lying with the multilevel inverter is the ease of interface with any of the renewable sources such as photovoltaic, wind and fuel cells at the dc input.

Multilevel inverters employ a series of power semiconductor devices and capacitors with a single dc source or a multiple dc sources without a capacitor, which generate voltages with stepped waveforms in the output. With the rise in level, the synthesized output waveform of MLIs consists of increased steps thereby producing a staircase wave which approach near to the desired waveform [3]. The considered topologies for this approach are the CHB and NPC MLIs which requires various independent dc sources and number of capacitors respectively. Generally, each phase of a cascaded multilevel inverter requires “n” dc sources for 2n+1 level. This paper is dedicated to implement PV fed CHB and NPC MLIs with MPPT algorithm using fixed frequency carrier based PWM which utilizes equal dc sources in each phase to generate a seven level equal step multilevel output [6-9] to extract maximum power from the PV array using P&O [10]. This structure is well-suited for high power applications which operate with less THD for increased modulation index.

During constant solar irradiation, PV panels possess a unique operating point where power output of PV is maximized. The nonlinear characteristics of PV power considering a single PV cell is shown in Fig.1. The variation in solar irradiation and temperature under load variation makes the task of extraction of maximum power quite challenging.

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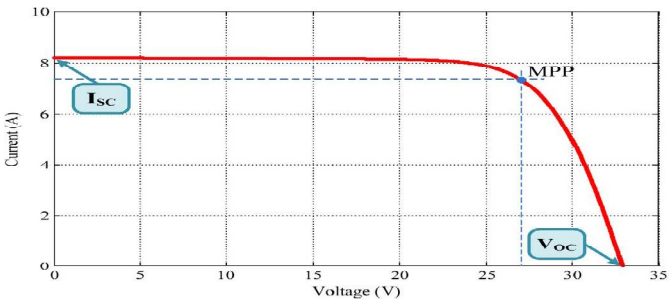

Fig.1 PV current-versus-voltage characteristics

System Composition: The system described in this paper has been categorized into three individual systems: - Generating a dc signal using photovoltaic system**,** Tracking maximum power from PV using MPPT**,** Step up of generated DC signal using boost converter, Pulse pattern generation and Conversion of DC signal to AC signal using single phase CHB and NPC-MLIs.

II. PV MODELLING

A solar cell can be modelled by connecting a current source in parallel with an inverted diode along with a series and a parallel resistance as shown in Fig.2. The series resistance represents the opposition offered in the path of flow of electrons from n to p junction and parallel resistance considers the effect of the leakage current. The output characteristic of a PV module depends on the solar insulation, the cell temperature and the output voltage of the PV module. It is required to model the PV module considering its nonlinear characteristics to implement the design and simulation of Maximum Power Point Tracking (MPPT) for PV system applications. The equivalent circuit of single diode model is depicted in Fig.2. The current source I_{ph} represents the cell photocurrent and I_D is the diode current with R_{sh} and R_s respectively denoting the shunt and series resistances of the cell.

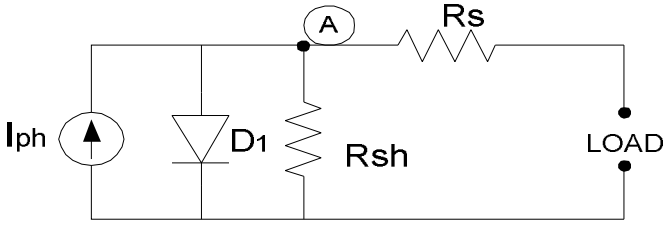

Fig.2 Equivalent model of the PV panel

The simulation model representing the PV array is based on the output current of a single PV equivalent model, and its mathematical equation is represented by

$$I = I_{ph} - I_r \cdot \left[e^{\frac{q.(V+I.Rs)}{n.k.T}} - 1 \right] - \frac{V+I.Rs}{Rp} \qquad (1)$$

Where 'V' represents the output PV voltage of one PV panel, Iph is the photocurrent, Ir is the saturation current, q is the electrical charge (1.6×10^{-19} C), η is the p-n junction quality factor, k is the Boltzmann constant (1.38×10^{-23} J/K), and 'T' is the temperature (in kelvins).

In Figs. 3 and 4, the power characteristics of the PV cell have been analysed, considering variation in solar irradiation and temperature change. The curve clearly depicts the nonlinear characteristics, and strong effect of intermittent behaviour of climate and weather conditions.

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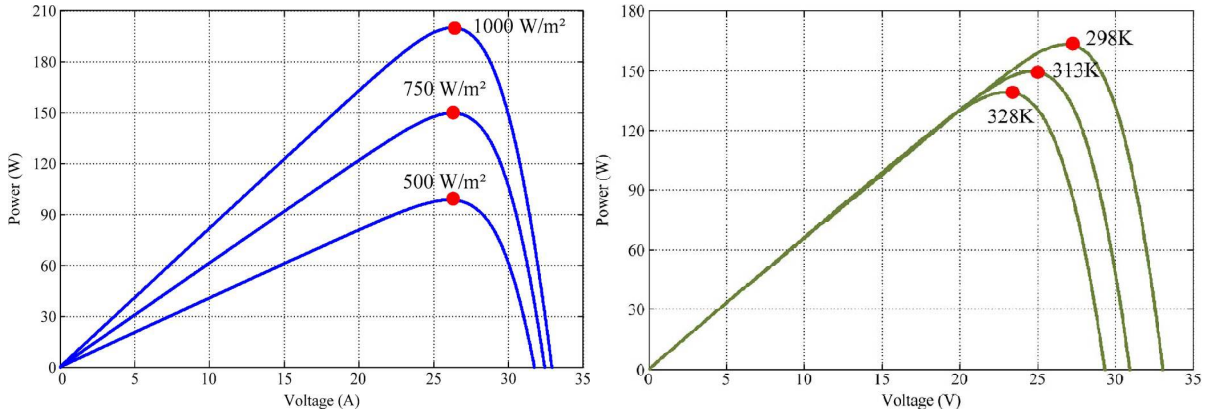

(a) **(b)**

Fig.3 PV power characteristic for (a) different irradiation levels & (b) different temperature levels

With the wide variation in solar irradiation throughout the day, the generated output of PV module varies accordingly with rapidly varying weather conditions. To get rid of this problem, Maximum Power Point Tracking (MPPT) algorithm is used which keep on tracking the operating point of I-V curve to achieve to its maximum value. Therefore the MPPT algorithm ensures the maximum power delivery from the solar modules at any particular weather condition. In the proposed study, Perturb & Observe (P & O) algorithm is used to extract maximum power from the PV modules. The operation of P&O method is governed by periodically incrementing or decrementing the output terminal voltage of the PV cell and comparing the power obtained in the current cycle with the power of the previous one (performs dP/dV). If the voltage varies and the power increases, the control system changes the operating point in that direction; otherwise, it changes the operating point in the opposite direction. Once the direction for the change of voltage is known, the voltage variation takes place at a constant rate. The flowchart for MPPT is shown in Fig.4 and the MATLAB/SIMULINK model for P&O algorithm is shown in Fig.5.

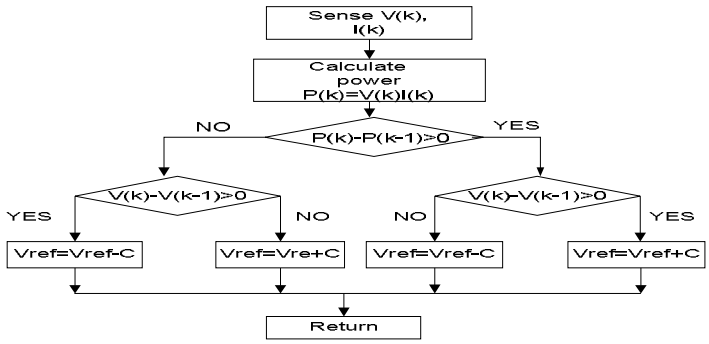

Fig.4 MPPT control flow chart

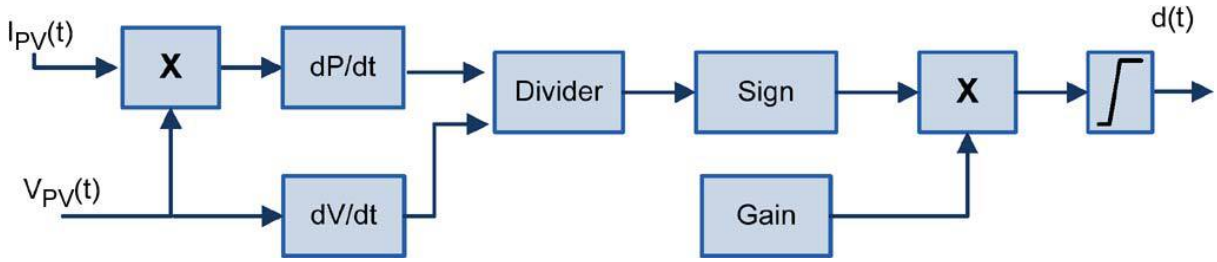

Fig.5 Implementation of P&O method through MatLab/Simulink.

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III. OPERATION OF BOOST CONVERTER, CHB & NPC CONVERTERS

In PV fed boost converter, the output voltage is greater than input voltage. In the model under study, a power IGBT is considered in boost converter as shown in Fig.6 .The output of the boost converter is shown in fig.7.

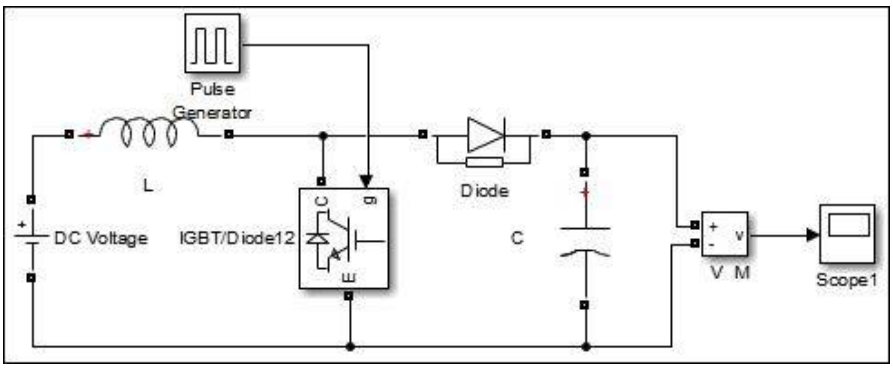

Fig.6 MATLAB/SIMULINK model for boost converter

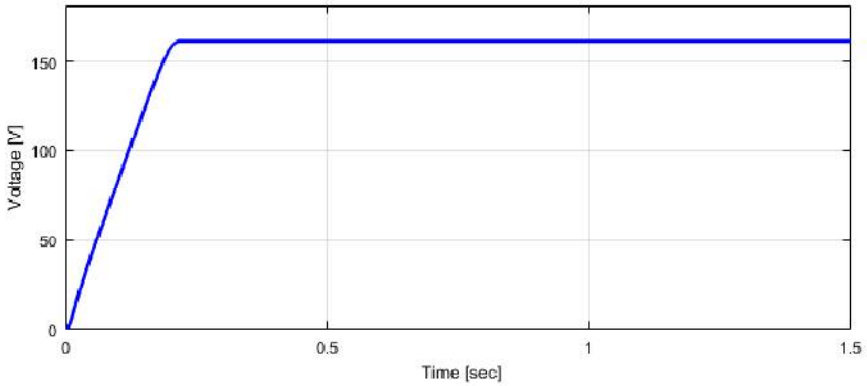

Fig.7 Output voltage of boost converter

A Cascaded H-bridge multilevel inverter is a back to back arrangement [8] of various single phase full bridge inverters. The each H-bridges consists of switches S1, S2, S3and S4 which can respectively generate three different output voltage levels +Vdc, 0, and -Vdc by suitably connecting the dc input (PV panel) to the ac output through the different combinations of the four switching devices [7]. In symmetrical topology, the magnitude of the input to each of the H-bridge is the same, whereas in an asymmetrical configuration the magnitude of the input differs for each H-bridge.
The number of output phase voltage level 'n' in a cascaded multilevel inverter is given by equation (2).

$$n=2S+1 \qquad (2)$$

Where, S is the number of dc sources.
Whereas, in NPC topology [9], semiconductor devices are connected in series and dc link is divided to smaller capacitors and connects to switches by clamp diodes. The clamp diode connections are necessarily required to block the current. The number of capacitors in each phase is proportional to the number of phase voltage levels. The ground point as shown in the figure is the common reference point and is connected to the middle of dc link. To generate N voltage levels by the aim of the diode-clamped inverter, N-1 capacitors are needed on the dc bus.

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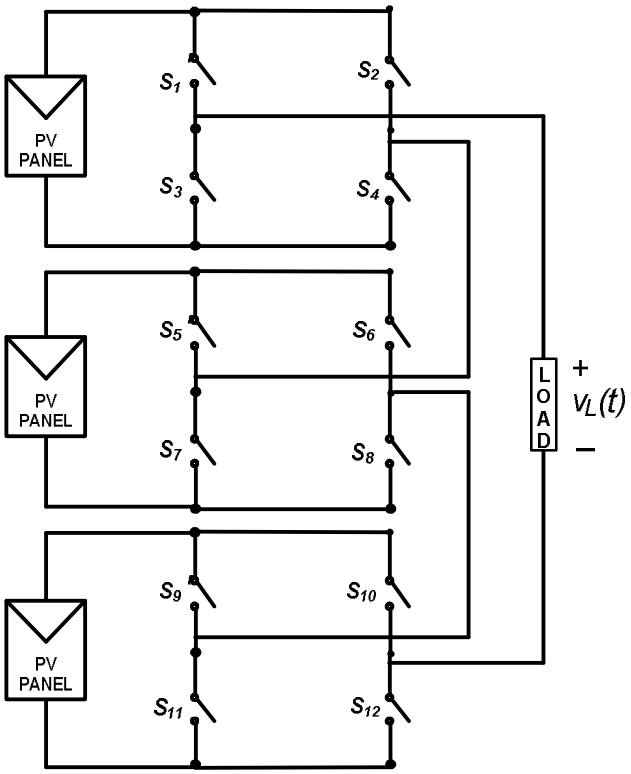

TABLE I
VALID SWITCHING STATES FOR THE STRUCTURE PROPOSED IN FIG.8

State	Switches in ON State	Output Voltage $V_L(t)$
1	S_1 S_4 S_5 S_8 S_{11} S_{12}	+3Vdc
2	S_1 S_4 S_5 S_8 S_{11} S_{12} S_3 S_4 S_5 S_8 S_9 S_{12} S_1 S_4 S_7 S_8 S_9 S_{12}	+2Vdc
3	S_1 S_4 S_7 S_8 S_{11} S_{12} S_3 S_4 S_5 S_8 S_{11} S_{12} S_3 S_4 S_7 S_8 S_9 S_{12}	+Vdc
4	S_1 S_2 S_5 S_6 S_9 S_{10} S_3 S_4 S_7 S_8 S_{11} S_{12}	0
5	S_2 S_3 S_7 S_8 S_{11} S_{12} S_3 S_4 S_6 S_7 S_{11} S_{12} S_3 S_4 S_7 S_8 S_{10} S_{11}	-Vdc
6	S_2 S_3 S_6 S_7 S_{11} S_{12} S_2 S_3 S_7 S_8 S_{10} S_{11} S_3 S_4 S_6 S_7 S_{10} S_{11}	-2Vdc
7	S_2 S_3 S_6 S_7 S_{10} S_{11}	-3Vdc

Fig.8 Seven level CHB multilevel inverter

A PV fed seven level multilevel inverters with a standalone load are shown in Fig.8 and Fig.10. It is possible to obtain voltage levels, $+3V_{dc}$, $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$,$-2V_{dc}$ and $-3V_{dc}$ by suitably firing the switches of the seven level multilevel inverters. The firing pulses are generated using multicarrier pulse width modulation technique. In this technique, as shown in Fig.9, a standard sinusoidal wave is compared with six number of triangular wave to generate the firing pulses for each switch in the multilevel inverter.

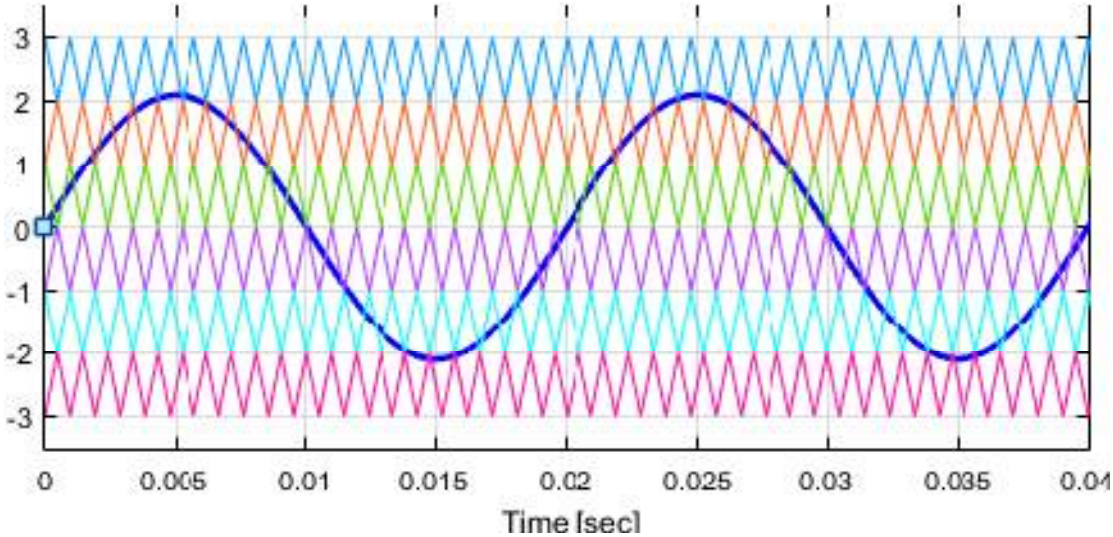

Fig.9 Multicarrier PWM technique for seven level multilevel inverter

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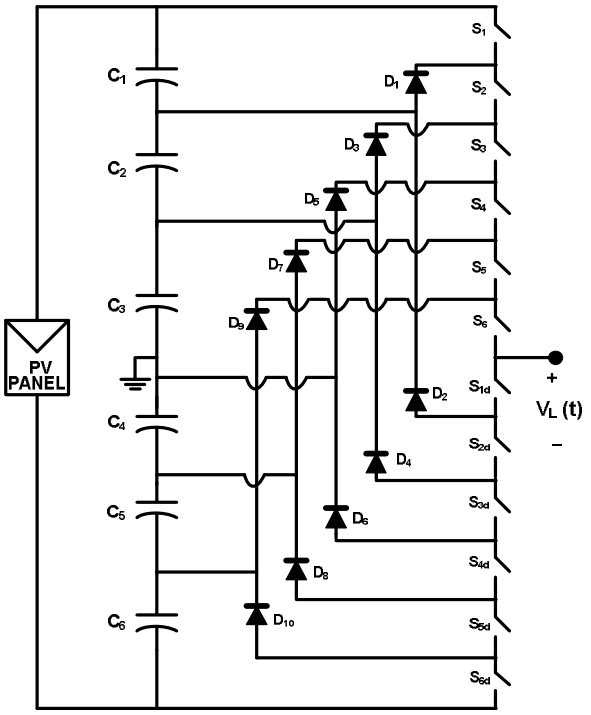

TABLE II
VALID SWITCHING STATES FOR THE STRUCTURE PROPOSED IN FIG.10

State	Switches in ON State	Output Voltage $V_L(t)$
1	S_1 S_2 S_3 S_4 S_5 S_6	+3Vdc
2	S_2 S_3 S_4 S_5 S_6 S_{1d}	+2Vdc
3	S_3 S_4 S_5 S_6 S_{1d} S_{2d}	+Vdc
4	S_4 S_5 S_6 S_{1d} S_{2d} S_{3d}	0
5	S_5 S_6 S_{1d} S_{2d} S_{3d} S_{4d}	-Vdc
6	S_6 S_{1d} S_{2d} S_{3d} S_{4d} S_{5d}	-2Vdc
7	S_{1d} S_{2d} S_{3d} S_{4d} S_{5d} S_{6d}	-3Vdc

Fig.10 Seven level NPC multilevel inverter

IV. SIMULATION STUDY AND RESULT DISCUSSION

The simulation and performance analysis of the standalone PV system with the seven level CHB and NPC MLIs are carried out under MATLAB/Simulink environment. The PV fed multilevel inverters feeding an RL load has been considered. Fig.10, fig.12 (a) & (b), 14 (a) & (b) show block diagram of PV fed MLI using MPPT and output waveform of the single phase PV based seven-level CHB and NPC multilevel inverters. The load current waveforms are sinusoidal and inductive in nature as desired. The FFT spectrum of the load voltage and current determined using the FFT analysis tool for CHB and NPC MLIs are shown in Fig.12 (c) and fig.13 (c), Fig.14 (c) and fig.15 (c) respectively and the THD of voltage and current are 23.77%, 14.85% and 27.59%, 17.62% respectively.

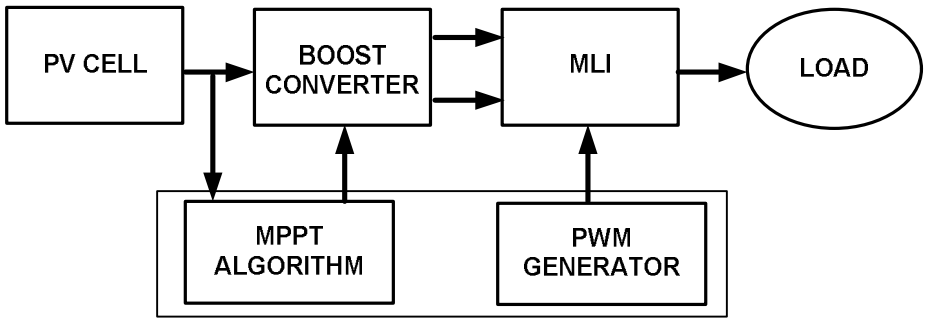

Fig.10 Block diagram of PV fed MLI using MPPT

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TABLE III
SIMULATION PARAMETERS

PV ARRAY VOLTAGE	Symmetric (54.7 V)
Modulating wave frequency	f_m = 50 Hz
Switching Frequency	f_s = 1000 Hz
Modulation Index	m_a = 0.85
Boost Converter Inductance ,capacitance values	L = 100 mH, C = 3000 µF
Load Resistance, Inductance values	R = 100Ω,L = 15 mH

Alternative phase opposition disposition triangular signals with frequency 1 kHz is employed as carriers and sinusoidal reference with frequency 50 Hz is used with an amplitude modulation index of 0.85. The so-called 'universal control scheme' as proposed in [6] is used to modulate the topology.

For a 7-level inverter, carrier and reference signals with aggregated signal are depicted in Fig.11. The simulation parameters are specified in Table III.

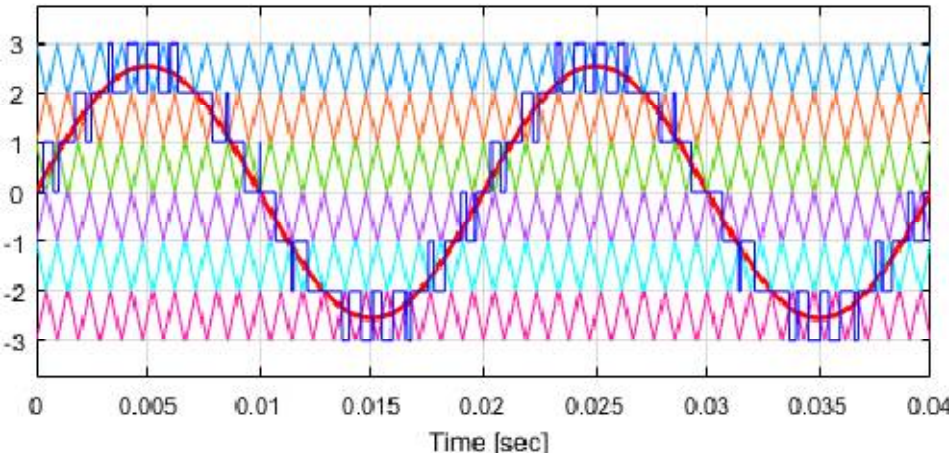
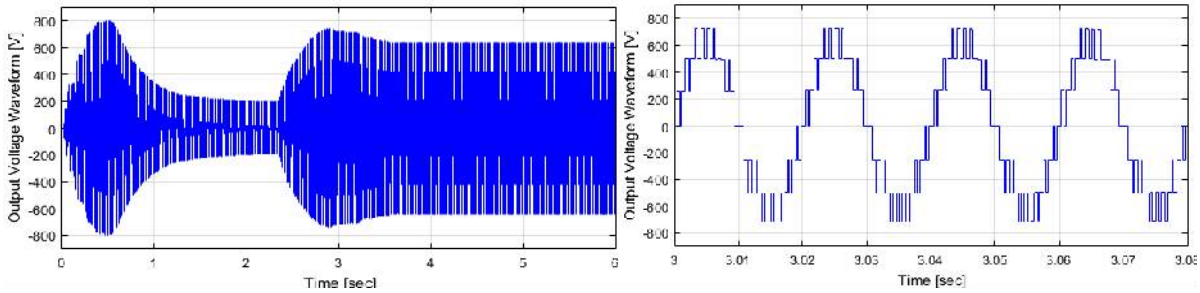


Fig.11 Reference and Carrier Waveforms with resulted Aggregated signal "a (t)"



(a) **(b)**

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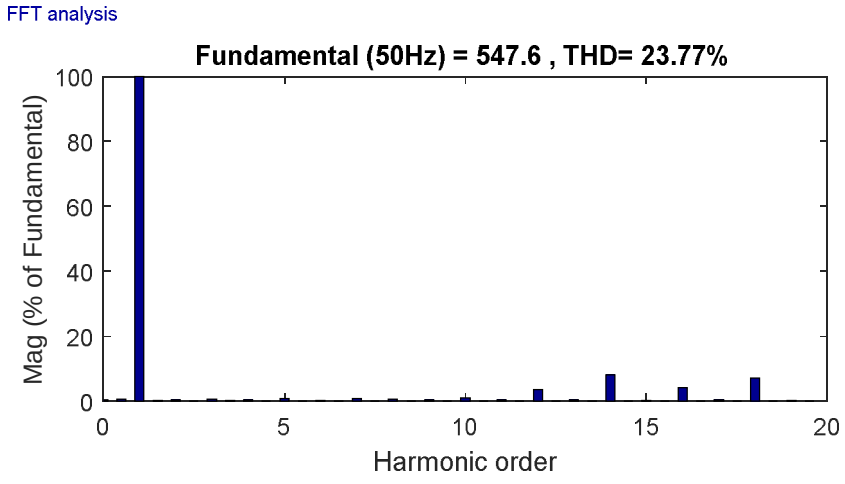
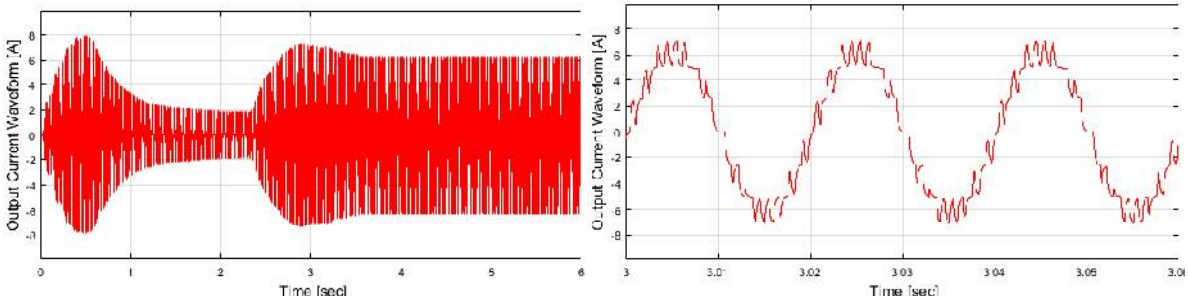
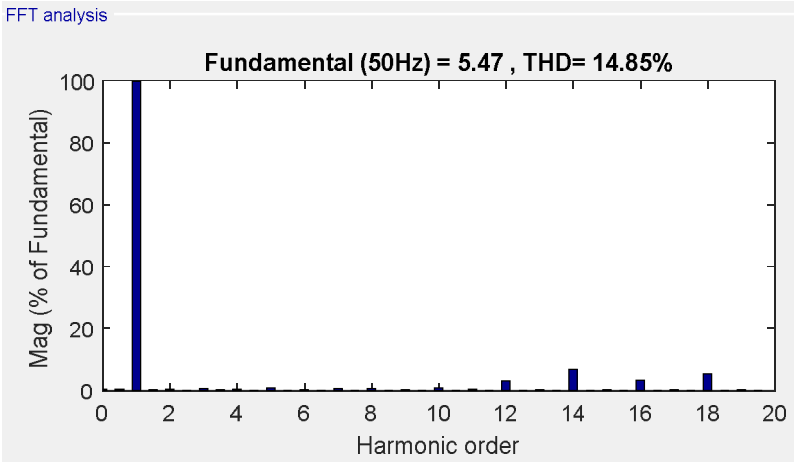


(c)

Fig.12 Simulated waveforms for 7-level cascaded inverter; (a) & (b) load voltage $V_L(t)$; and (c) Harmonic profile of load voltage



(a) **(b)**



(c)

Fig.13 (a) & (b) Load current waveform of 7-level CHB-MLI with RL load (R=100Ω, L=15 mH) (c) Harmonic spectrum of load current

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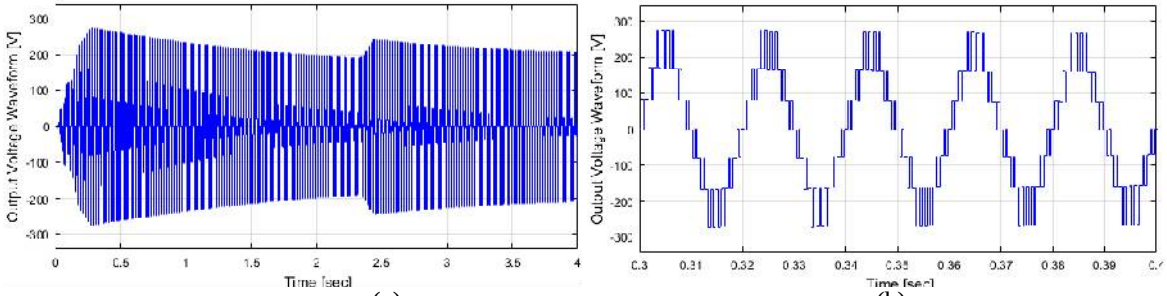
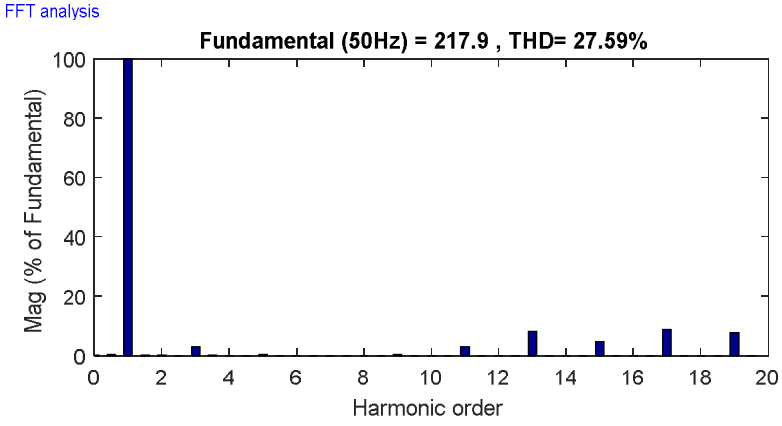
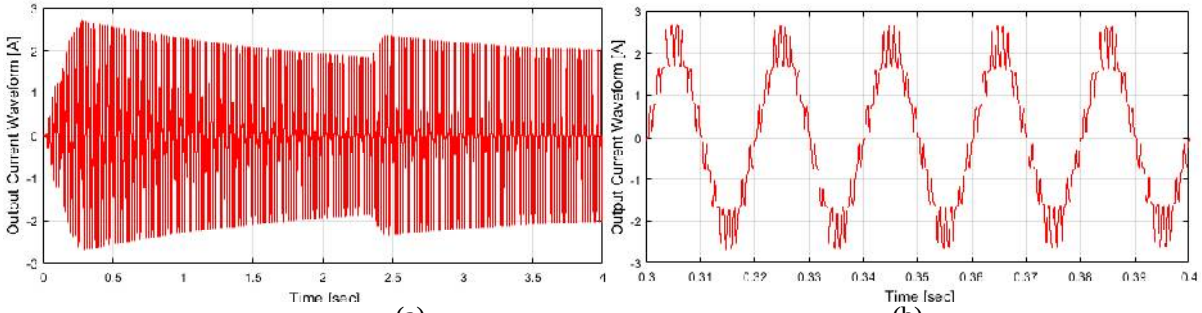


(a) (b)



(c)

Fig.14 Simulated waveforms for 7-level NPC inverter; (a) & (b) load voltage $V_L(t)$; and (c) Harmonic profile of load voltage



(a) (b)

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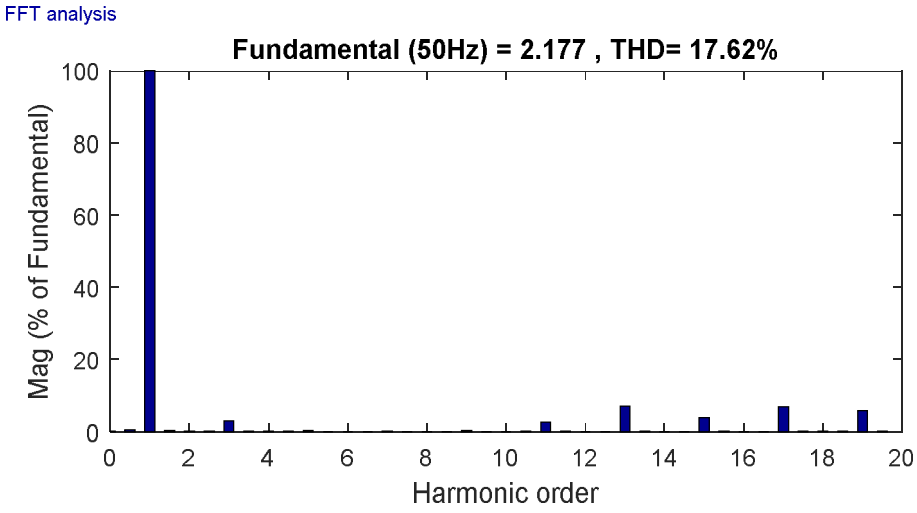

(c)

Fig.15 (a) & (b) Load current waveform of 7-level NPC-MLI with RL load (R=100Ω, L=15 mH) (c) Harmonic spectrum of load current.

TABLE IV
COMPARISON OF PV FED CHB & NPC CONVERTERS

MLIs	Output Voltage Levels	THD % (Voltage)	THD % (Current)	Switches (IGBT)	Diodes	Capacitors	PV Panel
CHB	7	23.77%	14.85%	12	NIL	NIL	3
NPC	7	27.59%	17.62%	12	10	6	1

V. CONCLUSION

The simulation of PV fed seven-level CHB and NPC MLIs with intermediate boost converter using MPPT technique has been described in the paper. The PV array output power delivered to the load can be maximized using P&O control algorithm. The boost converter is allowed to work in continuous mode and the switching sequence of multilevel inverter is generated by a PWM generator which uses APOD-PWM control scheme. Total Harmonic Distortion analysis was performed for inverters output voltage with open loop configuration. By carrying the FFT analysis to examine the performance, it is clearly observed that THD is less for CHB-MLI as compared to the NPC-MLI making it quite suitable for photovoltaic applications. Comparative analyses of investigated structures in terms of THD, device count, requirement of diodes, capacitors used are tabulated in Table IV.

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