



ISSN (Print) : 2320 – 3765  
ISSN (Online): 2278 – 8875

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: [www.ijareeie.com](http://www.ijareeie.com)

Vol. 6, Issue 4, April 2017

## PV Integrated with Multi Level Inverter using Level Shift PWM Technique

Sreenivas Kumar Kundi, C.Bharathi

Assistant Professor, Department of Electrical & Electronics Engineering, GIITS Engineering College, Aganampudi;  
Visakhapatnam (Dt), Andhrapradesh, India.

Assistant Professor, Department of Electrical & Electronics Engineering, GIITS Engineering College, Aganampudi;  
Visakhapatnam (Dt), Andhrapradesh, India.

**ABSTRACT-** For medium voltage and high power applications, multilevel inverter has been accepted as a better alternative; as it has better waveform quality, low stresses on switching devices and better performance. Among the various topology of multi level inverter cascaded H-bridge inverter has been found as more reliable, easy to implement and better performance. This paper reviews the application of multilevel converters in the integration of renewable energy sources. This new type of converters is suitable for high voltage and high power application due to their ability to synthesize waveforms with reduced harmonic distortion. Number of topologies have been introduced and widely studied, amongst the CHB topology is the proper option from the point of view of modularity and simplicity of control. Main disadvantage of multilevel configuration is increase in number of power semiconductor switches and its complexity to design gate driver circuit individually, its cost and switching losses. Complexity of the system reduces reliability of the inverter. By reducing number of switches for the same levels of voltages these disadvantages can be reduced effectively. This project presents a new technique for getting a synthesized multilevel output and also uses PWM control techniques for CHB topology, in this technique, the number of dc voltage sources, switches, and power diodes used for the dc to ac conversion is reduced. So this dc to ac conversion significantly reduces the initial cost. The proposed topologies are IPD (In-phase Disposition), POD (Phase Opposition Disposition) and APOD (Alternate Phase Opposition Disposition). The simulations for the same are carried out for single phase and three phase open loop and closed loop configurations in MATLAB/Simulink software. The proposed concept can be implemented level shift PWM technique with RES system using mat lab/Simulink software.

**KEYWORDS:** Cascaded H-bridge multi level inverter, level-shift PWM, Total Harmonic Distortion PV system.

### I. INTRODUCTION

Now a days in the field of medium voltage and high power applications multi level voltage source inverter (VSI) playing vital role; as it has better waveform quality, low dv/dt stresses on switching devices and no electromagnetic interferences problem compared to conventional two level voltage source inverter [1]. In many practical applications a sinusoidal voltage becomes necessity; owing to cost effectiveness of multi level inverter became popular choice as it generates staircase voltage closer to sinusoid, also as the number of levels increases waveform quality improves and the filter requirement reduces [2-3]. Cascaded multilevel inverters are based on a series connection of several single phase inverters. This structure is capable of reaching medium output voltage levels using only standard low-voltage mature technology components. Typically, it is necessary to connect three to ten inverters in series to reach the required output voltage. These converters also feature a high modularity degree because each inverter can be seen as a module with similar circuit topology, control structure, and modulation [4-5].

In case of PV system it's advantageous to use cascaded H bridge converter as each converter requires separate DC sources. Additional advantages are possible elimination of the DC/DC converters [6-7], significant reduction of the power drops caused by sun darkening and hence potential increase of efficiency and reliability. Main disadvantage of multilevel configuration is increase in number of power semiconductor switches and its complexity to design gate

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: [www.ijareeie.com](http://www.ijareeie.com)

Vol. 6, Issue 4, April 2017

driver circuit individually, its cost and switching losses. Complexity of the system reduces reliability of the inverter. By reducing number of switches for the same levels of voltages these disadvantages can be reduced effectively.

Total Harmonic Distortion (THD) and to control the output voltage of multilevel inverter; carrier based PWM is one of them [8-9]. It is a so called sine triangle PWM; as a reference is sine wave and carrier is triangular wave. Level shifted method is a type of sine PWM technique and it has three types, namely: In phase disposition, phase opposition disposition, alternative phase opposition disposition.

This paper focuses on improving the efficiency of the multilevel inverter and quality of output voltage waveform. Harmonics Elimination was implemented to reduce the Total Harmonics Distortion (THD) [10-11] value. To minimize the power demand and scarcity we have to improve the power extracting methods. There are many limitations in extracting power from renewable energy resources. To extract power from solar cells multilevel inverter is used. It synthesizes the desired ac output waveform from several dc sources. In industrial applications multilevel inverter shows hope to reduce initial cost and complexity [12-13].

A single sinusoidal reference is compared with each carrier signal to determine the output voltage for the inverter. In case of the N-level NPC type multi-level [14] inverter, N-1 triangular carrier signals with the same frequency and amplitude are used so that they fully occupy contiguous bands over the range +VDC to -VDC.

If the capacitor voltage is unbalanced, the output voltage becomes unsymmetrical and it results in a high harmonic content in the load current three dispositions of the carrier signal to generate the PWM signal are considered as follows; 1) Phase disposition (PD); where all carriers are in phase. 2) Alternative phase opposition disposition (APOD); where each carrier is phase shifted by 180 degree from its adjacent carrier [15].

## II. CASCADED H-BRIDGE INVERTER

### 1 Principle of Operation:

The circuit arrangement of a single phase five level voltage source inverter is shown in fig.1 (a), it consists of two single phase full bridge inverter with separate DC source [6]. Each voltage source inverter is capable of producing voltage levels 0, +Vdc, or -Vdc. In symmetrical mode for 'x' number of separate DC sources; the output voltage level will be 2x+1. Hence two separate DC sources produce voltage levels of +2Vdc, +Vdc, 0, -Vdc & -2Vdc in symmetrical mode.

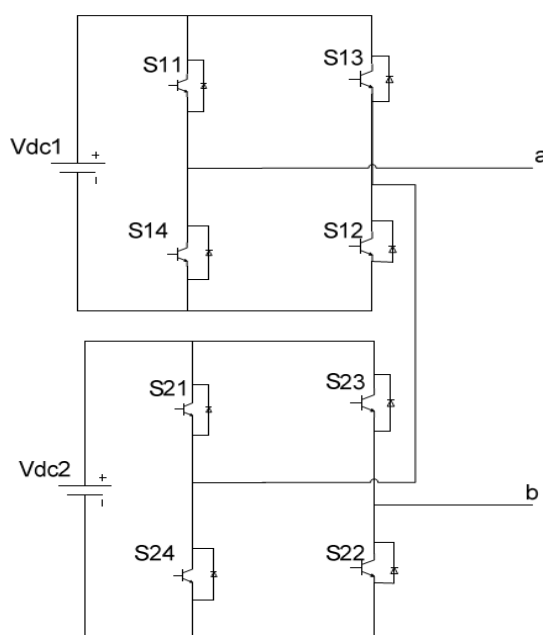


Fig.1 (a) single phase five levels Cascaded H-bridge inverter

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: [www.ijareeie.com](http://www.ijareeie.com)

Vol. 6, Issue 4, April 2017

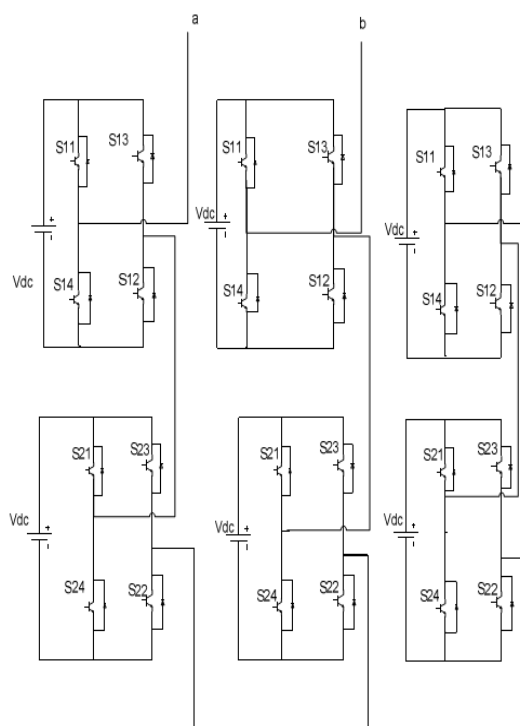


Fig.1 (b) three phase circuit arrangement for five level in star configuration.

The Cascaded H-bridge is basically of two types:

**a) Symmetrical CMLI:** if  $V_{dc1} = V_{dc2}$ , The output voltage of the inverter is the sum of the each inverter's phase voltage i.e.  $V_{ab} = V_{ao} + V_{bo}$ . All the possible combination of switching sequence for five levels is shown in Table I, where '1' shows conducting state of a switch and '0' shows non-conducting state of the switch. For 5-level inverter the phase output voltage for resistive load is shown in fig. 3.1 (c).

TABLE I

Vab	S11	S12	S21	S22
2Vdc	1	0	1	0
Vdc	1	0	1	1
	1	0	0	0
	1	1	1	0
	0	0	1	0
0	0	0	0	0
-Vdc	0	1	1	1
	0	1	0	0
	1	1	0	1
	0	0	0	1
-2Vdc	0	1	1	0



# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: [www.ijareeie.com](http://www.ijareeie.com)

Vol. 6, Issue 4, April 2017

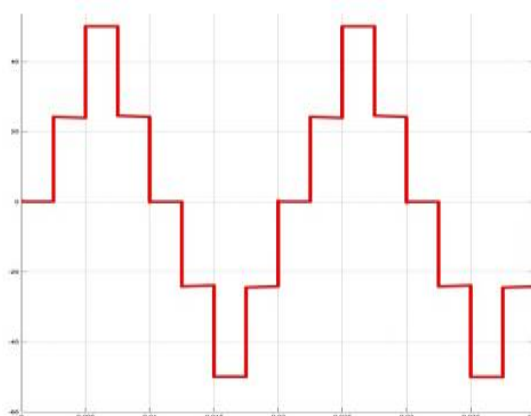


Fig.1 (c) output voltage of five level inverter.

**b) Asymmetrical CMLI:** if  $V_{dc1} \neq V_{dc2}$ ; then by using the fig.1 (a) seven levels of voltage can be produced if  $V_{dc1} = 2V_{dc2}$  in asymmetrical mode [19]. The switching transition for seven levels asymmetrical inverters is shown in Table II.

TABLE II

Sl. No	S11	S12	S21	S22	Vab
01.	1	0	0	0	3Vdc
02.	1	0	0	1	2Vdc
03.	0	0	1	0	Vdc
04.	0	0	0	0	0
05.	0	0	0	1	-Vdc
06.	0	1	1	0	-2Vdc
07.	0	1	0	0	-3Vdc

In achieving higher voltage levels the asymmetrical configuration has certain limitations such as tedious calculation of switching transition, loss of modularity and modulation index restrictions. In this paper further symmetrical mode has considered.

## 2Applications

- Industry up-to multi-MW range in Tractions and Naval systems.
- High Power Propulsion systems.
- STATCOM, FACTS, UPFC Active power filters, etc.
- A Green Energy source with Photo Voltaic cells.
- Storage battery charger where high power and efficient energy conversion are required with improved power quality.



# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: [www.ijareeie.com](http://www.ijareeie.com)

Vol. 6, Issue 4, April 2017

## III. PWM STRATEGY

Among the various methods of PWM, level-shift PWM technique is used to simulate the above mentioned levels [11]. Level-shift PWM is of three types:

### *a) Phase Opposition Disposition (POD):*

In this category of level shift PWM technique modulating signal above the reference (zero) line is 180 degrees out of phase with modulating carrier signals below the reference line.

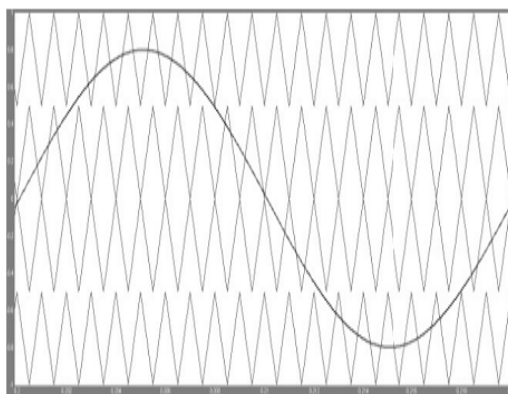


Fig.2 Phase opposition disposition level shift PWM

*b) In Phase Disposition (PD):* in this technique all the modulating signals are in phase, and a sinusoidal reference signal is continuously compared to producing the gating signals

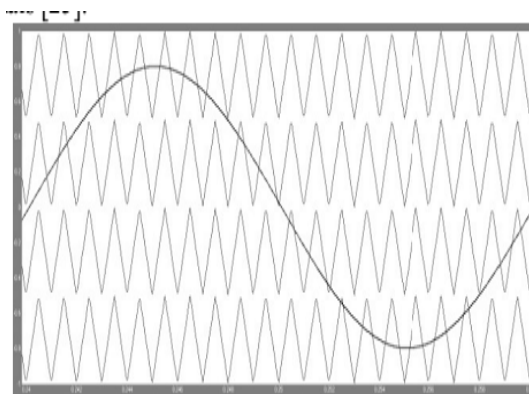


Fig.3 in Phase Disposition level shift PWM

*c) Alternative Phase Opposition Disposition (APOD):* in this PWM each modulating carrier is 180 degrees out of phase with its adjacent neighbor carriers

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: [www.ijareeie.com](http://www.ijareeie.com)

Vol. 6, Issue 4, April 2017

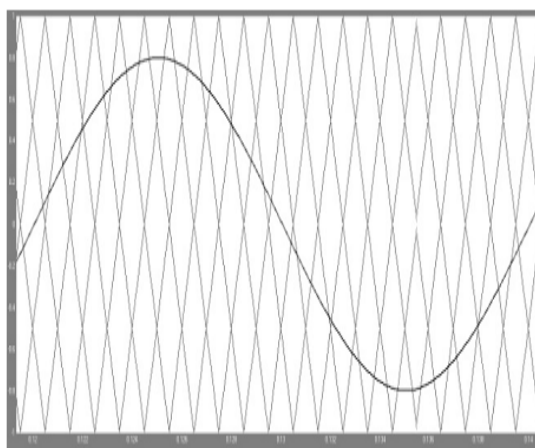


Fig. 4 Alternative POD level shifts PWM

## IV. A PHOTOVOLTAIC SYSTEM

A photovoltaic system, converts the light received from the sun into electric energy. In this system, semi conductive materials are used in the construction of solar cells, which transform the self contained energy of photons into electricity, when they are exposed to sun light. The cells are placed in an array that is either fixed or moving to keep tracking the sun in order to generate the maximum power [9]. These systems are environmental friendly without any kind of emission, easy to use, with simple designs and it does not require any other fuel than solar light. On the other hand, they need large spaces and the initial cost is high.

PV array are formed by combine no of solar cell in series and in parallel. A simple solar cell equivalent circuit model is shown in figure. To enhance the performance or rating no of cell are combine. Solar cell are connected in series to provide greater output voltage and combined in parallel to increase the current. Hence a particular PV array is the combination of several PV module connected in series and parallel. A module is the combination of no of solar cells connected in series and parallel.

The photovoltaic system converts sunlight directly to electricity without having any disastrous effect on our environment. The basic segment of PV array is PV cell, which is just a simple p-n junction device. The manifests the equivalent circuit of PV cell. Equivalent circuit has a current source (photocurrent), a diode parallel to it, a resistor in series describing an internal resistance to the flow of current and a shunt resistance which expresses a leakage current. The current supplied to the load can be given as.

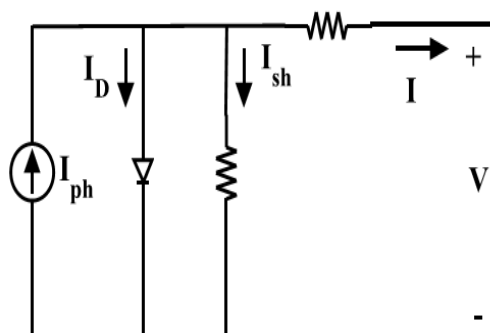


Fig 5 Equivalent circuit of Single diode modal of a solar cell

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: [www.ijareeie.com](http://www.ijareeie.com)

Vol. 6, Issue 4, April 2017

$$I = I_{PV} - I_0 \left[ \exp \left( \frac{V + IR_S}{aV_T} \right) - 1 \right] - \left( \frac{V + IR_S}{R_p} \right)$$

Where

$I_{PV}$ –Photocurrent current,

$I_0$ –diode’s Reverse saturation current,

$V$ –Voltage across the diode,

$a$ – Ideality factor

$V_T$ –Thermal voltage

$R_s$  – Series resistance  $R_p$  –Shunt resistance

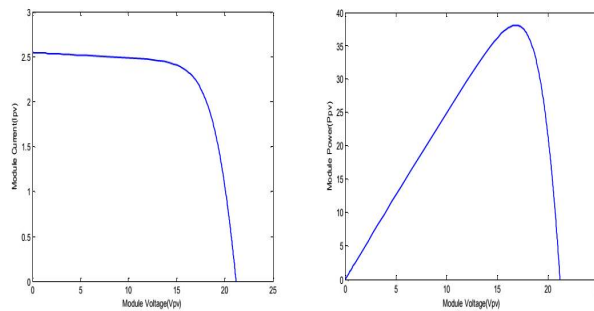


Fig.6 V-I & P-V Characteristics of a 36w PV module

## The Effect of Different Solar Irradiation

The Voltage vs Power characteristics and Voltage vs Current characteristics of a solar cell are mainly dependents upon the solar irradiation. If there is change in the environmental condition then the solar irradiation level change which results different maximum power. So maximum power point tracking algorithm are used to maintain the maximum power constant if there is any change in the solar irradiation level. If the solar irradiation level is higher, then the input to the solar cell is more which results more magnitude of the power with the same voltage value. Also when there is increase in the solar irradiation the open circuit voltage increases. Because, when there is more solar light fall on the solar cell, with higher excitation energy the electrons are supplied, they increase the mobility level of electron and more power is generated.

## V. MATLAB/SIMULINK RESULTS

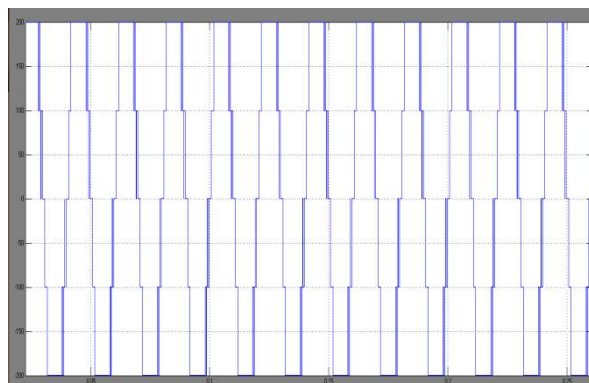


Fig 7 Single Phase 5-level output voltage



# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: [www.ijareeie.com](http://www.ijareeie.com)

Vol. 6, Issue 4, April 2017

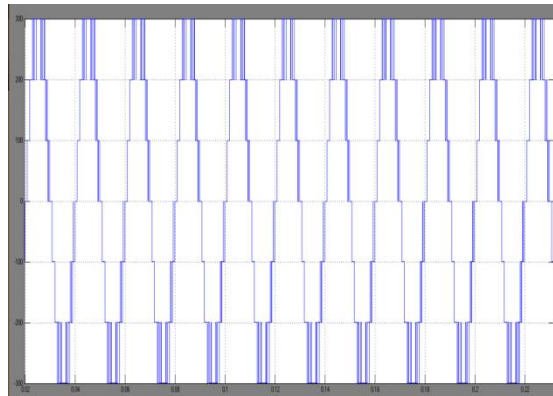


Fig 8 Single Phase 7-level output voltage

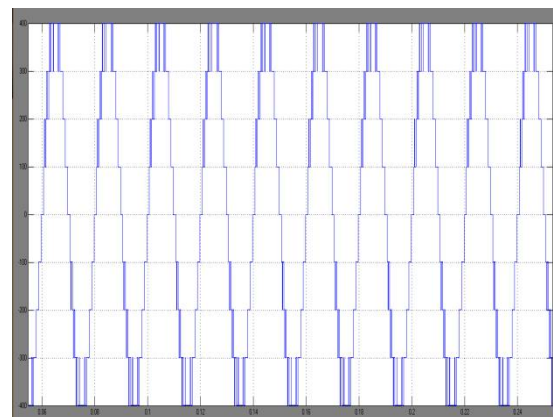


Fig 9 Single Phase 9-level output voltage

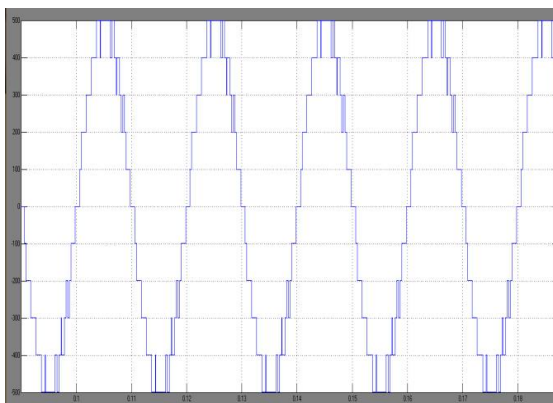


Fig 10 Single Phase 11-level output voltage





# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: [www.ijareeie.com](http://www.ijareeie.com)

Vol. 6, Issue 4, April 2017

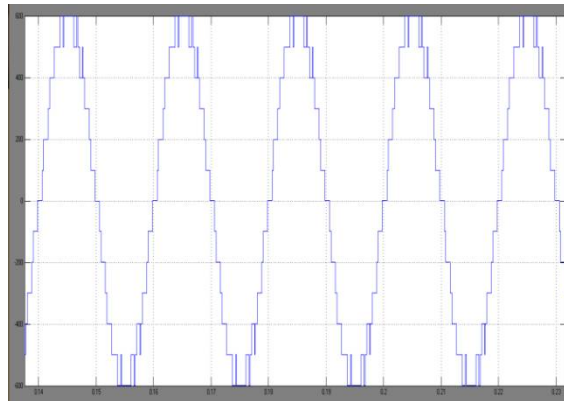


Fig 11 Single Phase 13-level output voltage

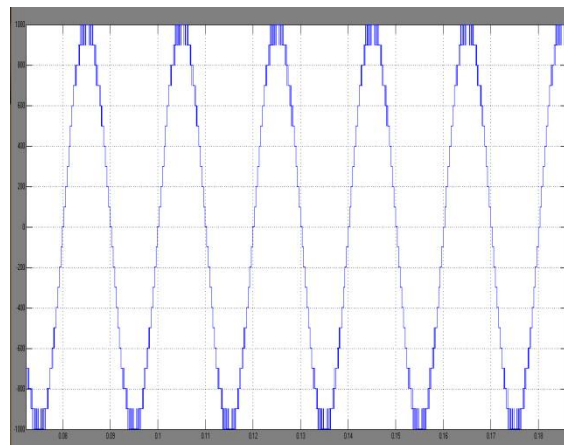


Fig 12 Single Phase 21-level output voltage

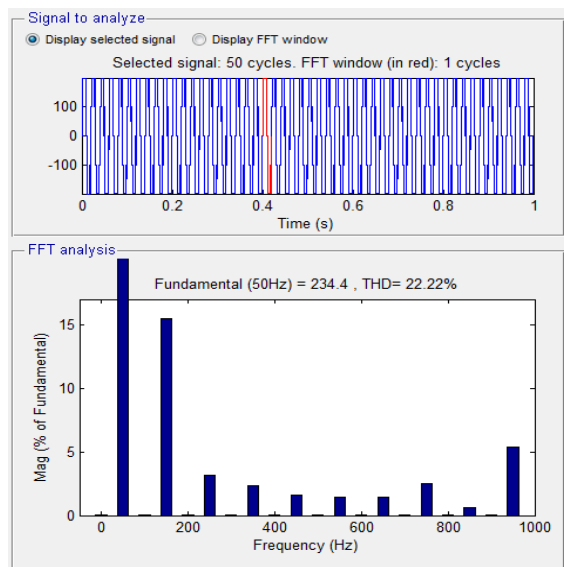


Fig 13 Single phase 5-level FFT analysis using PD

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: [www.ijareeie.com](http://www.ijareeie.com)

Vol. 6, Issue 4, April 2017

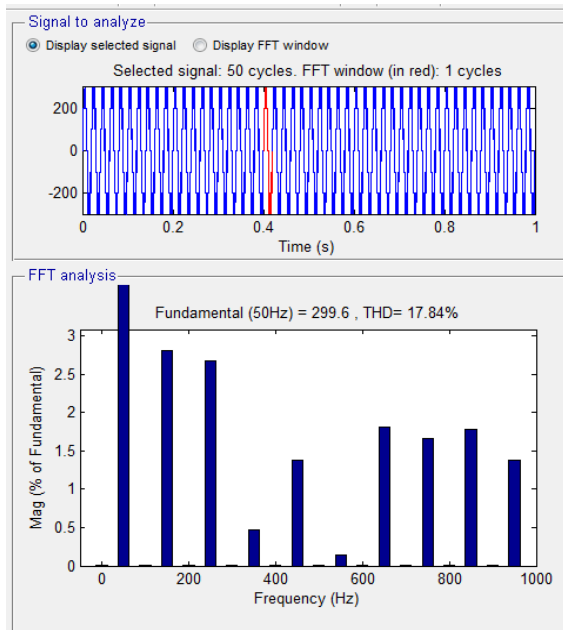


Fig 14 Single phase 7-level FFT analysis using PD

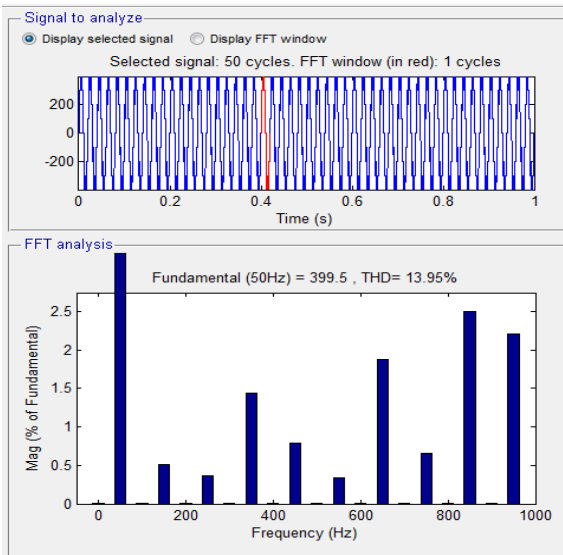


Fig 15 Single phase 9-level FFT analysis using PD

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: [www.ijareeie.com](http://www.ijareeie.com)

Vol. 6, Issue 4, April 2017

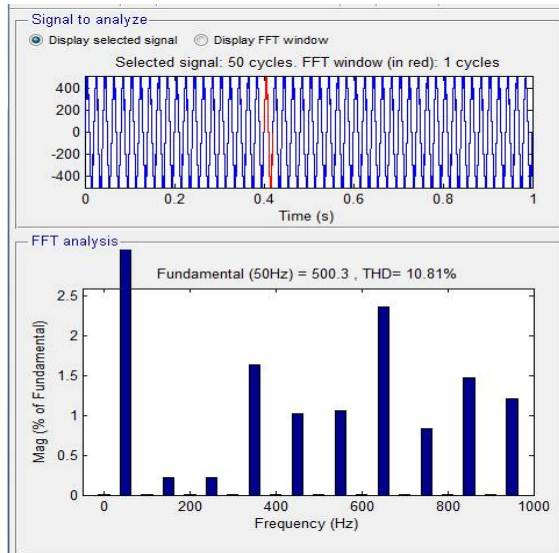


Fig 16 Single phase 11-level FFT analysis using PD

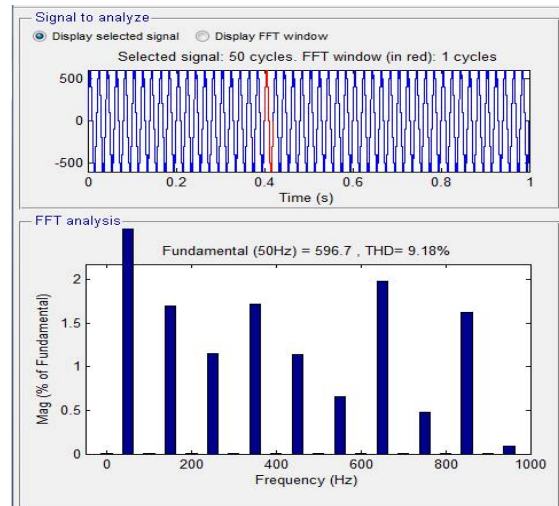


Fig 17 Single phase 13-level FFT analysis using PD

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: [www.ijareeie.com](http://www.ijareeie.com)

Vol. 6, Issue 4, April 2017

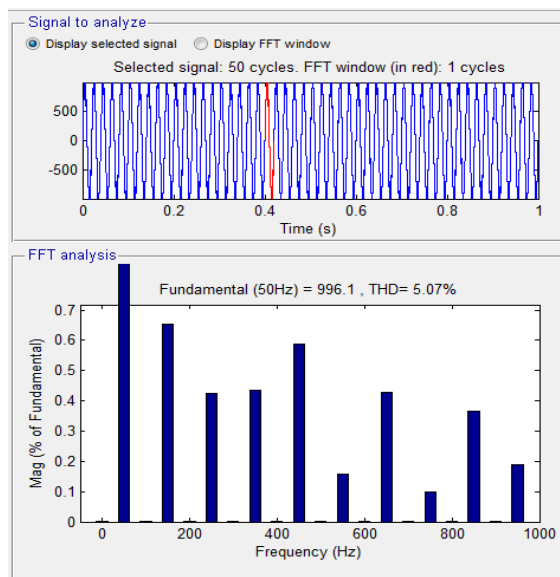


Fig 18 Single phase 21-level FFT analysis using PD

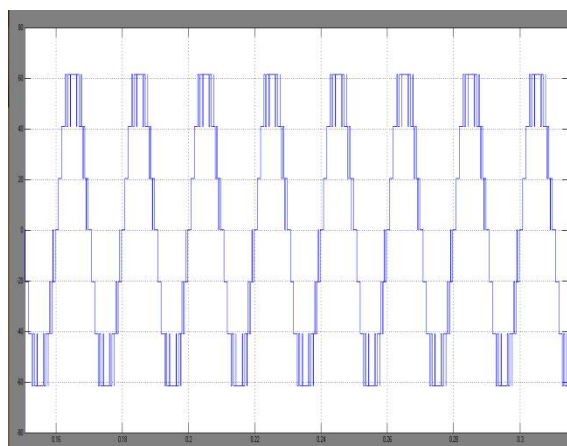


Fig 19 Single Phase 7-level output voltage with PV

## VI. CONCLUSION

Multilevel inverters offer improved output waveforms and lower THD. This paper has presented PWM switching scheme for the proposed multilevel inverter. It utilizes reference signals and a triangular carrier signal to generate PWM switching signals. The behavior of the proposed multilevel inverter was analyzed in detail. Symmetrical multilevel inverter topology has been proposed in this paper. From the theoretical discussion and simulation results we can come to conclude that the results of output voltage and current obtain from different levels of cascaded H-bridge Inverter Using Phase-Shifted PWM Technique are very close to fundamental. So, harmonic contains will be very less. Compare to other MLI topology cascaded bridge MLI become an effective and practical solution for increasing power and reducing harmonics of ac waveforms. The objective of work was to implement all the level-shift PWM method to symmetrical cascaded H-bridge inverter. Their Fourier analysis of THD has been studied at different carrier frequencies and at different voltage levels. For this 5-level, 7-level, 9-level, 11-level, 13-level and 21-levels of voltage has been simulated. Their corresponding FFT analysis has done for resistive load.



ISSN (Print) : 2320 – 3765  
ISSN (Online): 2278 – 8875

# International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Website: [www.ijareeie.com](http://www.ijareeie.com)

Vol. 6, Issue 4, April 2017

## REFERENCES

- [1] Beser, E.; Camur, S.; Arifoglu, B.; Beser, E.K. , — Design and application of a novel structure and topology for multilevel inverter,| in Proc. IEEE SPEEDAM, Tenerife, Spain, 2008, pp. 969 – 974.
- [2] Tae-Jin Kim; Dae-Wook Kang; Yo-Han Lee; Dong-Seok Hyun. , —The analysis of conduction and switching losses in multi-level inverter system,| In Proc. IEEE Power Electron.Specialist conf., 2001, vol. 3, pp. 1363 - 1368.
- [3] R.H. Baker, —High-Voltage Converter Circuit,| U.S. Patent Number 4,203,151, May 1980.
- [4] M.E.Ahmed, S.Mekhilef, —Design and implementation of a multilevel three-Phase inverter with less switches and low output voltage distortion,| Journal of Power Electronics, vol.9, no.4, pp.593–603, Jul. 2009.
- [5] S. Mekhilef and M. N. Abdul Kadir —Voltage control of three-stage hybrid multilevel inverter using vector transformation| IEEE Transactions on Power Electronics DOI:10.1109/TPEL.2010.2051040(in press), 2010, available online at (<http://ieeexplore.ieee.org>)
- [6] Daher, S.; Schmid, J.; Antunes, F.L.M, —Multilevel inverter topologies for stand-alone PV systems,| IEEE Trans. Ind. Electron.,vol. 55, no. 7, pp. 2703 – 2712 , Aug. 2008.
- [7] M. N. A. Kadir S. Mekhilef, and H. W. Ping —Voltage vector control of a hybrid three-stage eighteen-level inverter by vector decomposition| IET Trans. Power Electron.,vol.3,no. 4, pp.601- 611, 2010
- [8] J. Rodriguez, J. S. Lai and F. Z. Peng, —Multilevel inverters: Survey of topologies, controls, and applications,| ,| IEEE Trans. Ind. Applicant., vol. 49, no. 4, pp. 724-738, Aug. 2002.
- [9] R. H. Baker and L. H. Bannister, —Electric power converter,| U.S. Patent 3 867 643, Feb. 1975.
- [10] D P.Kothari, —Cascaded Seven Level Inverter With Reduced Number Of Switches Using Level Shifting PWM Technique|, 2013 International conference on power, energy and control (ICPEC).pp 676-679.
- [11] Abhishek Kumar Ranjan, D.Vijaya Bhaskar and Nibedita parida, “Analysis and Simulation of Cascaded H-Bridge Multi Level Inverter Using Level-Shift PWM Technique”, ICCPCT 2015.
- [12] Mariusz Malinowski, K. Gopakumar, Jose Rodriguez and Marcelo A. Pérez, “A Survey on Cascaded Multilevel Inverters” IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2197–2206, Jul. 2010.
- [13] Elimination of Harmonics in a Multilevel Converter with Nonequal DC Sources, L. M. Tolbert, J. N. Chiasson, Z. Du and K. J. McKenzie, IEEE Transactions on Industry Applications, Vol. 41, No. 1, January/February 2010
- [14] Performance analysis of SPWM control strategies using 13 level cascaded MLI, D Mohan, Sreejith B Kurub, IEEE international conference on advances in engineering science &management (ICAESM). 2012.
- [15] Energy Management system for Hybrid RES with Hybrid Cascaded Multilevel inverter, R Naveen Kumar, International Journal of Electrical and Computer Engineering (IJECE). 2014

## BIOGRAPHY



SREENIVAS KUMAR KUNDI Received his B.Tech Degree from Pydah Engineering college, Visakhapatnam, Andhrapradesh and M.Tech from Sri Vasavi Engineering College, Tadepalligudem, Andhrapradesh. He is currently working as Assistant Professor in Department of EEE , GIITS Engineering College, Aganampudi, Visakhapatnam (Dt), Andhra Pradesh, India. His area of Interest is Power Electronics.



C.BHARATHI Received her B.Tech Degree from Ranippettai Engineering College, Walaja, Vellore, Tamilnadu and M.Tech from Bharathi University, Chennai. She is currently working as Assistant Professor in Department of EEE, GIITS Engineering College, Aganampudi, Visakhapatnam (Dt), Andhra Pradesh, India. Her area of Interest is Electric Drives, Power Electronics, Power Systems.