



Bridgeless PFC Converter for LED Driver Application

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ABSTRACT: Pseudoboost rectifier used for natural power factor correction is proposed in this paper. Power factor is a measure of how effectively the current is being converted into useful work output and more particularly is a good indicator of the effect of the load current on the efficiency of the supply system. It has the advantages of less component count, high power density, less conduction loss and high efficiency. Power supplies with active power factor correction (PFC) techniques are becoming necessary for many types of electronic equipment to meet harmonic regulation and standards. This paper compared with conventional topology has an absence of input diode bridge and there is only one diode in the current path, thus improving the thermal management. To achieve an automatic power factor correction close to unity the topology works in resonant mode, which has the additional advantages such as zero-current turn-on in active switches and zero-current turn-off in the output diodes which reduce the complexity of the circuit. A prototype for bridgeless resonant pseudoboost PFC converter has been executed and analysed experimentally. Performance of the converter is evaluated and presented.

KEYWORDS: Power factor correction (PFC), Bridgeless rectifier, Total harmonic distortion

I. INTRODUCTION

Active power factor correction techniques are necessary adopted in telecommunication and computer industries to meet harmonic regulation and standards. Modern electronic equipment does not represent a completely passive load to the AC mains or power line. Most electronic systems now use one or more switch mode power converters that will tend to draw current from the power line in a non sinusoidal fashion. This input current characteristic results in current and possibly voltage distortions that can create problems with other equipment connected to the power line and degrade the capability of the mains. These problems have led to the creation of design standards for the purpose of limiting the allowable harmonic distortion on the power line. Fortunately, solutions are available for meeting these standards. These solutions are referred to as Power Factor Correction (PFC) techniques. Conventional PFC scheme has lower efficiency due to significant losses in the diode bridge. Most of the PFC rectifiers utilize a boost converter at their front end. However, a conventional PFC scheme has lower efficiency due to significant losses in the diode bridge. Which leads to a significant conduction loss, caused by the forward voltage drop across the bridge diode, would degrade the converter's efficiency, especially at a low line input voltage.

Bridgeless PFC circuit allows the current to flow through the minimum number of switching devices. Previous PFC converters have drawbacks such as high component count, components are not fully utilized over whole AC line cycle, complex control, DC output voltage is always higher than peak input voltage, lack of galvanic isolation and due to floating ground, some topologies require additional diodes and/or capacitors to minimize EMI. In order to overcome these problems proposed topology with two semiconductor in current conduction path during each switching cycle is presented. The proposed topology has low component count, single control signal and non floating output.

Proposed topology operates in discontinuous conduction mode for low power application. It has one less component than Totem-pole bridgeless PFC boost rectifier. The proposed topology not be considered as an "ideal" automatic current shaper, since the input current is not directly proportional to input voltage for a constant duty cycle.

II. BLOCK DIAGRAM

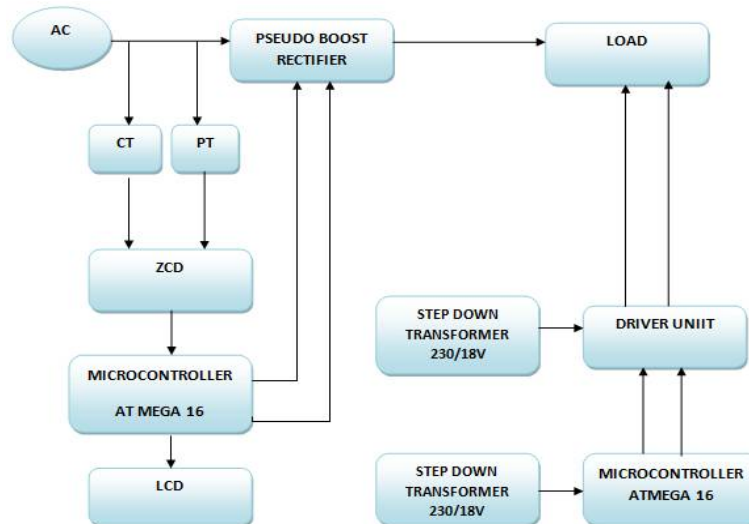


Fig1: Block diagram of pseudoboost converter

The pseudoboost converter is possible for ac-dc conversion. The power line voltage and current is taken through the potential and current transformer respectively. The potential transformer is used to step down the mains supply voltage to low voltage level. The voltage level is from 230 V AC to 12V AC. Then the output of the transformer is given to Zero Crossing Detector. The current consumed by the load is measured with the help of a current transformer. Then the corresponding AC voltage is given to zero crossing detector. The Zero Crossing Detector is used to convert the sine wave to square wave signal. The zero crossing detectors are constructed by the operational amplifier UA 741. The inverting and non inverting input terminals are connected to the potential transformer and current transformer terminals respectively. So the input sine wave signal is converted in to square wave signals. The square signal is in the range of +12v to -12v level. Then the both ZCDs outputs are given to logical XOR gate 7486 to find the phase angle difference between the voltage and current. The XOR gate output is given to microcontroller AT mega 16 and calculates the power factor with help of software.

III. POWER FACTOR MEASUREMENT CIRCUIT

The power factor measurement circuit is designed to find the power factor in the power line. Figure 2 shows the block diagram of the power factor measurement circuit. The power line voltage and current is taken through the potential and current transformer respectively. The potential transformer is used to step down the mains supply voltage to low voltage level. The voltage level is from 230 V AC to 12V AC. Then the output of the transformer is given to Zero Crossing Detector. The current consumed by the load is measured with the help of a current transformer. Then the corresponding AC voltage is given to zero crossing detector. The Zero Crossing Detector is used to convert the sine wave to square wave signal. The zero crossing detectors are constructed by the operational amplifier UA 741. The inverting and non inverting input terminals are connected to the potential transformer and current transformer terminals respectively. So the input sine wave signal is converted in to square wave signals. The square signal is in the range of +12v to -12v level. Then the both ZCDs outputs are given to logical XOR gate 7486 to find the phase angle difference between the voltage and current. The XOR gate output is given to microcontroller ATmega 16 and calculates the power factor with help of software.

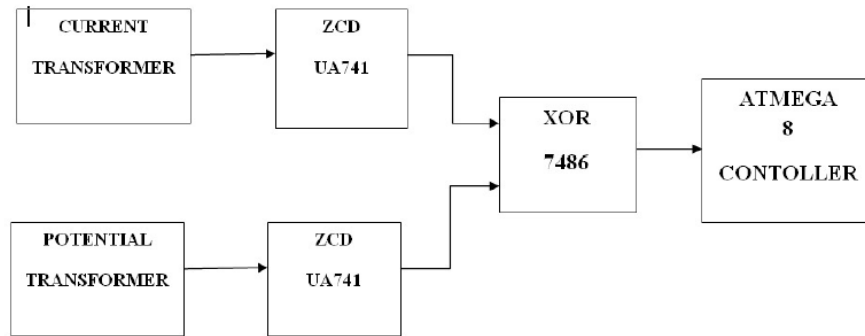


Fig 2 : Block diagram for power factor measurement circuit.

IV. PRINCIPLE OF OPERATION

The bridgeless pseudoboost rectifier designed to operate in discontinuous-conduction mode (DCM) during the switch turn-on interval and in resonant mode during the switch turn off intervals. Moreover, the two power switches Q1 and Q2 can be driven by the same control signal, which significantly simplifies the control circuitry. However, an isolated gate drive is required for the power switch Q1.

There are four modes of operation in DCM. The first stage (t_0-t_1) starts when the switch Q1 is turned-on. The body Diode of Q2 is forward biased by the inductor current i_{L1} . Diode D1 is reverse biased by the voltage across C1, while D2 is reverse biased by the voltages $V_{c1} + V_o$. In this stage, the current through inductor L1 increases linearly with the input voltage, while the voltage across capacitor C1 remains constant at voltage v_x .

During the second stage [t_1, t_2] when switch Q1 is turned OFF and diode D2 is turned ON simultaneously providing a path for the inductor currents i_{L1} . As a result, diode D1 remains reverse biased during this interval. The series tank consisting of L1 and C1 are excited by the input voltage V_{ac} through diode D_2 . The stage ends when the resonant current i_{L1} reaches zero and diode D2 turns OFF with zero current. During this stage, capacitor C1 is charged until it reaches a peak value.

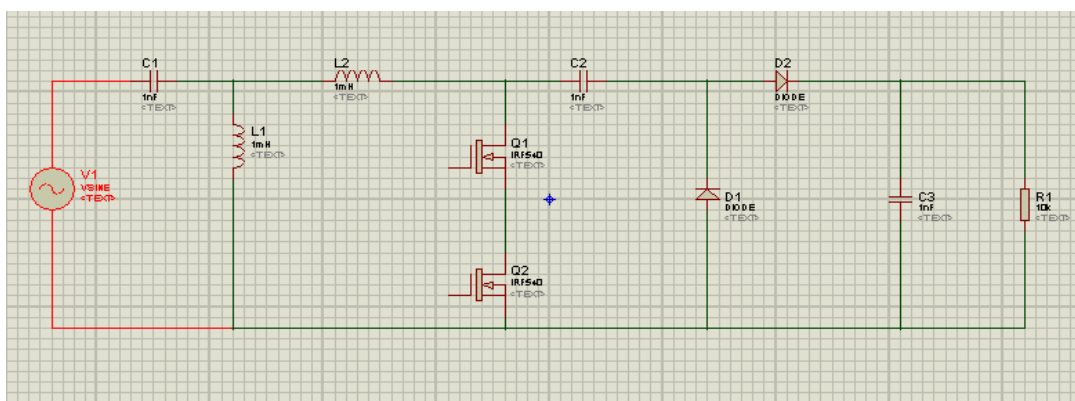


Fig 3: Circuit diagram of proposed pseudoboost converter

During the third stage [t_2, t_3] During this stage diode D1 is forward biased to provide a path during the negative cycle of the resonating inductor current i_{L1} . This stage ends when the inductor current reaches zero. Thus, during this stage diode D1 is switched ON and OFF under zero current conditions. Assuming the constant input voltage over a switching period, the capacitor is discharged until it reaches a voltage V_x .

During the fourth stage [t_3, t_4] switches are in their off state. The inductor current is zero, while the capacitor voltage remains constant. The resonant mode achieves an automatic PFC close to unity in a simple and effective



manner. The resonant mode operation gives additional advantages such as zero current turn on in the active power switches, zero current turn off in the output diode and reduces the complexity of the control circuitry.

IV.DESIGN PROCEDURE

In pseudoboost rectifier $V_{ac}=13V$, $V_0=24V$, $P_{out}=115W$ and $f_s=50kHz$.

The equations are derived from the base quantities such as

$$\text{Base voltage}=\text{Output voltage}, V_0 \tag{1}$$

$$\text{Base impedance}=\text{Z}_0=\sqrt{\frac{L_1}{C_1}} \tag{2}$$

$$\text{Base current}=\frac{V_0}{Z_0} \tag{3}$$

$$\text{Base frequency, Fr}=\frac{\omega_r}{2\pi}=\frac{1}{2\pi\sqrt{L_1C_1}} \tag{4}$$

The circuit components are designed by assuming the efficiency as 100%.

1.The voltage conversion ratio,

$$M=\frac{V_0}{V_m}=\frac{d_1}{\sqrt{2K}}=\sqrt{\frac{RL}{2R_e}} \tag{5}$$

$$\text{Since, } R_e=\frac{2L_1}{d_1^2T_s} \tag{6}$$

The value of M is obtained by

$$M=\frac{V_0}{V_m}=\frac{24}{\sqrt{2}\times 13}=1.305 \tag{7}$$

2. For ensuring the DCM operation,the normalised switching frequency must be less than one. So for that F is chosen as 0.8

3. The dimensionless conduction parameter ,

$$K=\frac{2L_1}{R_L T_s} \tag{8}$$

$$K<\frac{1}{2}\times\left(\frac{f}{\pi}\right)^2=K_{cr} \tag{9}$$

From these the value of critical inductance required to maintain DCM operation is

$$L_1\leq\frac{R_L T_s}{4}\times\left(\frac{f}{\pi}\right)^2 \tag{10}$$

4. The value of resonant capacitance can be calculated from (4)

$$C_1 = \frac{1}{L_1 (2\pi fr)^2} = 65 \text{ nF} \quad (11)$$

The switch duty cycle,

$$d_1 = M \sqrt{2K} = 0.4 \quad (12)$$

5. Input power factor

$$PF = \frac{(P_{in(t)})_{TL}}{V_{ac, rms} I_{ac, RMS}} \quad (13)$$

6. The line current distortion is represented by the factor total harmonic distortion (THD). THD is the ratio of harmonic contents to the fundamental contents. It can be calculated by using the relation

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} I_{ac, rms}^2(n)}}{I_{ac, rms}(1)} \quad (14)$$

The total harmonic distortion and power factor can be related as

$$THD = \sqrt{\left(\frac{\cos(\theta_1)}{PF}\right)^2 - 1} \quad (15)$$

V. HARDWARE SETUP

Fig 4 shows the hardware of bridgeless resonant pseudoboost converter for powerfactor correction. Thus we can improve the efficiency and reduce the cost.

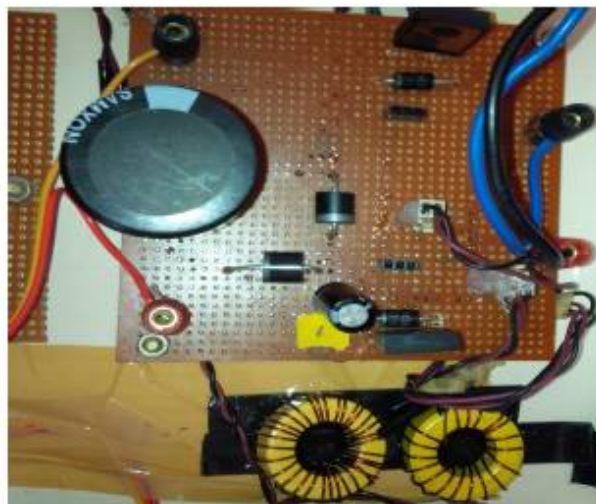


Fig 4: Hardware of bridgeless pseudoboost converter

Components:

- 1) MOSFET(2 no) : IRFP250N
- 2) Diodes(2 no.) : 4A, IN4001 rectifier diode
- 3) Filter capacitor : 10 microfarad, 250 V.

- 4) Filter inductor : 22 turns, torroid core, 22 SWG wire.
- 5) Output capacitor : 1000 microfarad, 250 V.
- 6) Tank inductor : 22 turns, torroid core, 22 SWG wire.
- 7) Potential transformer : 230/12 V
- 8) Current transformer : 5A
- 9) Operational amplifier : UA 741
- 10) Logical XOR gate : 7486
- 11) Microcontroller : AT mega 8A

The hardware picture of the developed Driver circuit is shown in Figure



Fig 5: Hardware of driver circuit

Each MOSFET switch needs a separate driver circuit. Here two driver circuit is used. Driver circuit is used to provide 9 to 20 volts to switch the MOSFET Switches of the inverter. Driver amplifies the voltage from micro controller which is 5 volts. Also it has an optocoupler for isolating purpose. So damage to MOSFET is prevented. The driver circuit forms the most important part of the hardware unit because it acts as the backbone of the inverter because it gives the triggering pulse to the switches in the proper sequence.

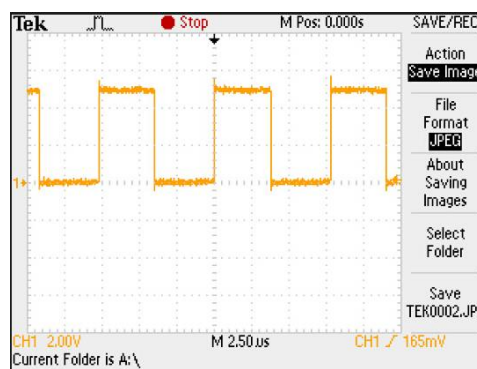


Fig 6: Gate pulse waveform

For pseudoboost rectifier the two switches are active during each half cycle of total operation. The pulses are applied in such a way that only one switch will close for one half cycle and the other switch will close for next half cycle. The microcontroller is programmed for providing pulse to the MOSFET with a frequency range of 50kHz. Fig6 shows gate pulse waveform obtained from oscilloscope(DSO)



VI. CONCLUSION

The prototype for Pseudoboost rectifier has been executed and the design procedure of the converter is suitably implemented for LED driver application. The analysis results meet the harmonics requirements according to Class D, we could get power factor almost close to unity. The power switches of proposed topology need same control signal and low component count. Thus circuit is simple with high efficiency and low cost.

REFERENCES

- [1] J. Marcos Alonso, J. Vina, D. G. Vaquero, G. Martinez, and R. Osorio, "Analysis and design of the integrated double buck-boost converter as a high-power factor driver for power-LED lamps," *IEEE Trans. Ind. Electron.*, vol. 59, no. 4, pp. 1689–1696, Apr. 2012.
- [2] S. K. Khand and D. D. Lu, "Implementation of an efficient transformer less single-stage single-switch AC/DC converter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4095–4104, Dec. 2010.
- [3] H. J. Chiu, Y. K. Lo, H. C. Lee, S. J. Cheng, Y. C. Yan, C. Y. Lin, T. H. Wang, and S. C. Mou, "A single-stage soft-switching flyback converter for power-factor-correction applications," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2187–2190, Jun. 2010.
- [4] Y. Jang and M. M. Jovanovic, "Bridgeless high-power-factor buck converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 602–611, Feb. 2011.
- [5] Z. Chen, J. Xu, G. Zhou, and F. Zhang, "Analysis of bridgeless pseudo-boost PFC Converter," in *Proc. IEEE Int. Symp. Ind. Electron.*, May 2012.
- [6] D. D. Chuan Lu and W. Wang, "Bridgeless power factor correction circuits with voltage-doubler configuration," presented at the *IEEE Int. Conf. Power Electronic and Drive Systems*, Singapore, Dec. 2011.
- [7] C. M. Wang, "A novel single-stage high-power-factor electronic ballast with symmetrical half-bridge topology," *IEEE Trans. Ind. Electron.*, vol. 55, no. 2, pp. 969–972, Feb. 2008.
- [8] R. W. Erickson and D. Maksimovic, in *Fundamentals of Power Electronics*, M. A. Norwell, Ed., 2nd ed. Norwell, MA, USA: Kluwer, 2001.
- [9] B. A. Mather and D. Maksimovic, "A simple digital power-factor correction rectifier," *IEEE Trans. Power Electron.*, vol. 26, no. 1, pp. 919, Jan. 2011.
- [10] J. C. Tsai, C. L. Ni, C. L. Chen, Y. T. Chen, C. Y. Chen, and K. H. Chen, "Triple loop modulation (TLM) for high reliability and efficiency in a power factor correction (PFC) system," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3447–3458, July. 2013.