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PFC Converter Topologies with Improved Constant On-Time Control

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ABSTRACT: Power factor correction converter topologies with Constant On-Time (COT) control are presented in this paper. Conventional buck PFC converter with COT control exhibit dead zones in ac input current. An improved buck power factor correction converter combining the advantages of COT control is presented. An integrated Buck-flyback non isolated PFC converter is proposed which is an inherent integration of a buck converter and a flyback converter, which operates in either flyback mode or buck mode according to whether the input voltage is lower or higher than the output voltage. In this way, the dead zones of ac input current in traditional buck converter can be eliminated. Therefore, integrated buck–flyback power factor correction converter can achieve high power factor under universal ac input range, and its input current harmonics can be reduced. Different converter topologies with COT control are simulated using MATLAB/Simulink. A 10W laboratory prototype of the integrated Buck-flyback power factor correction converter with 12V input voltage was setup using PIC 16F877 microcontroller. Compared to conventional power factor correction converters, the power factor was improved greatly with the proposed topology. This proposed topology is very suitable for high-power non isolated LED drivers with high power factor requirements.

KEYWORDS: AC–DC Converter, Power factor correction, buck–flyback converter, harmonic currents, Constant On-Time (COT) control, high power factor (PF).

I. INTRODUCTION

AC/DC converter plays a major role in day to-day life. Electrical energy is almost exclusively generated, transmitted and distributed in the form of alternating current. Therefore the question of power factor immediately comes into picture. In recent years, the power electronic systems and devices, which are used more frequently, create harmonic current and pollute the electricity network. Harmonics have a negative effect on the operation of the receiver, which is fed from the same network. AC-DC converters have drawbacks of poor power quality in terms of injected current harmonics, which cause voltage distortion and poor power factor at input ac mains and slow varying ripples at dc output load, low efficiency and large size of AC-DC filters. SMPS, the most frequently used power electronic system, can present nonlinear loads which impose current harmonics onto the main power network. Awareness of the necessity of power quality is increasing, and power factor correction is being implemented on a growing scale.

Power factor correction technique is well applied to the ac/dc converters because it can provide almost sinusoidal input current. Because we want a constant dc supply in the output, so we connect a capacitor in the output of ac/dc converters. This capacitor distorts the input current waveform. To overcome these drawbacks, low harmonic and high power factor converters are used. We replaced the single AC-DC rectifier by a rectifier followed by a DC-DC power factor correction.

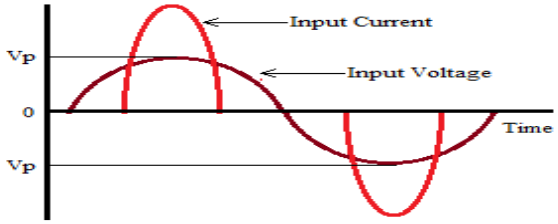

Fig .1 Input waveforms for SMPS with poor power factor

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In the past few years, the boost power factor correction converter was the most popular topology due to its inherent shaping ability of the input current. A bridgeless power factor correction boost rectifier, also called dual boost PFC rectifiers is presented in [3]. The boost PFC cannot achieve high efficiency at low line because it works with large duty cycle in order to get high voltage conversion gain. It is hard to increases the power density of boost PFC converter attributes to the thermal problem at low line. With bridgeless structure for boost PFC converter, the efficiency can be improved at low line. But, more components should be added to deal with the electromagnetic interference issue, which leads to high cost. The efficiency improvement of the bridgeless PFC boost rectifier over the conventional PFC boost rectifier is predominantly limited by the on-resistance of the boost switches.

The buck PFC converter can achieve a relatively high efficiency particularly at low input voltage due to the low average input current and rms current, while the voltage stress of the switch is also low. Therefore, the buck PFC converter has drawn much attention.

II. PFC TOPOLOGIES WITH COT CONTROL

A. Conventional Buck PFC Converter

A CRM Buck PFC converter with constant on-time (COT) control is proposed in [5]. In COT control, although the switching period is variable, the on time of one switching cycle of the switch is almost constant in one line cycle. Compared to the conventional boost power factor correction converter, the buck PFC converter can achieve high efficiency in the entire universal input voltage range. The buck converter operates in CRM may eliminate the diode reverse-recovery losses, and provide its advantage for ZVS for the turn ON of the switch if the input voltage is lower than double of the output voltage. A CRM Buck PFC converter with constant on-time (COT) control is shown in Figure 2.

a. Control Strategy

The buck converter operates in CRM may eliminate the diode reverse-recovery losses, and provide its advantage for ZVS for the turn ON of the switch if the input voltage is lower than double of the output voltage. In order to demonstrate the COT control principle and soft switching performance of the buck PFC converter, Fig. 3 shows the key waveforms in one switching cycle according to simplified control schematic in Fig. 2. When load and input are constant, the on time of the switch is fixed, which is determined by comparing the constant-slope ramp V_{ramp} and *V*EAO. When switch is ON, inductor current increases linearly and the slope is determined by the difference between input and output voltage and the inductance. Thus, the peak current value is a function of the input voltage as described in (1).

$$\frac{\text{Vin}-\text{Vout}}{\text{L}} = \text{I}_\text{p} \qquad (1)$$

where V_{in} is the rectified input supply voltage, V_o is output voltage across the output capacitor, L is the inductance of the transformer secondary winding, T_{on} is the ON duration of the switch and I_p is the peak value of the input current in the working region. From (1) inductance L and input supply voltage are constants. V_o is kept almost consant by using a large value of output capacitance. If T_{on} is kept constant from (1) it is clear that I_p will be proportional to V_{in}.

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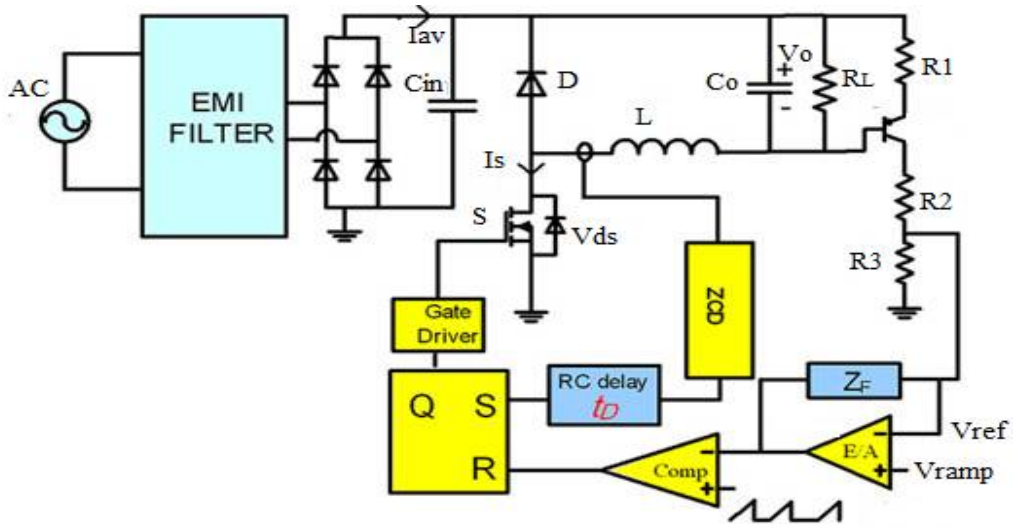

Fig .2 Circuit diagram of CRM buck PFC with constant on-time control.

Accordingly, the peak current in working region can follow the input voltage, when output voltage V_o is constant. When S is turned OFF, current in inductor begins decreasing and V_{ds} increases rapidly because the inductor current charge the intrinsic capacitors very fast. When the inductor current drops to zero, it is detected by a detecting circuit. At the same time, a resonant interval caused by the intrinsic capacitor and inductor L appears. The voltage V_{ds} decreases due to this resonance and the inductor current reverses a little. And after a certain time delay t_D , the switch S is turned ON. With the decrease of V_{ds}, the switching ON losses of S and the reverse recovery in diode D can be reduced significantly.

Although the peak current in the switch is almost proportional to the input voltage, if output is assumed constant during one whole line cycle because the output capacitance C_o is large enough, there are dead zones in the input current because when the input is lower than output V_o , the converter does not work. The low frequency distortion in the line current arises from its unavoidable notches around the zero crossings of the line voltage, caused by the inability of the buck converter to draw current when the instantaneous input voltage is lower than the output one. So it is difficult for the buck PFC converter to pass the IEC61000-3-2 Class C limits due to the dead zones in the input current which occur when the input voltage is lower than output voltage V_o, as shown in Figure 3.

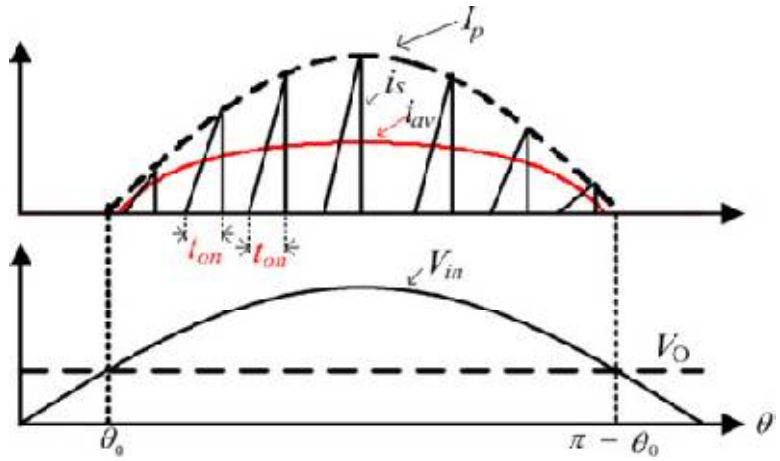

Fig .3 Relationships between input current, switch current, and output voltage with constant on-time control

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B. Improved Buck PFC Converter

In conventional buck PFC converter input current waveforms exhibit dead zones at the zero crossing instants of input voltage. This is due to the fact that a buck converter will not draw any current from the input supply when the input voltage less than the output voltage. This will affect the effective utilization of the input power supply. If current absorption is allowed when the input voltage is less than the output voltage maximum power can be drawn from the supply. An improved buck PFC converter is proposed, as shown in Fig. 4.

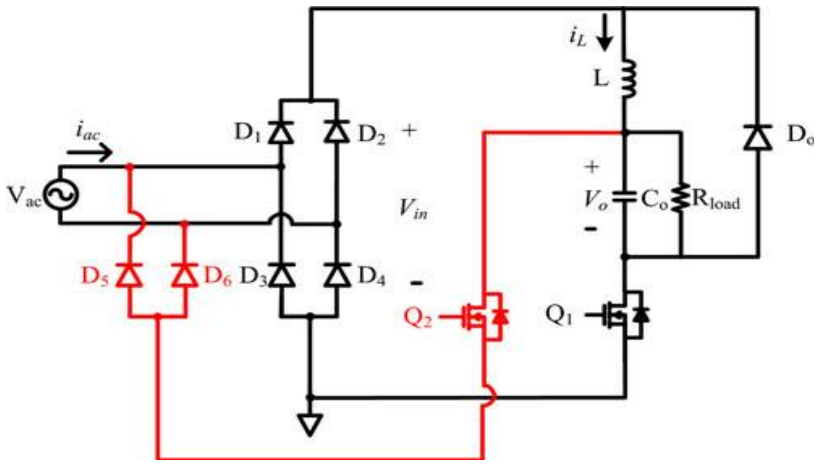

Fig .4 Circuit diagram of Improved buck PFC

Compared with the conventional buck PFC converter, an auxiliary switch and two diodes are added in the improved buck PFC converter. This converter has two different operation modes in a line period. When the input voltage is higher than the output voltage, this converter operates in buck mode, which is same as the conventional buck converter. When the input voltage is lower than the output voltage, the converter operates in buck-boost mode. Hence, there are no dead zones in the input current. The PF can be improved obviously.

a. Control Strategy:

The control signal V_{ph} used to control the converter either in buck mode or buck-boost mode is achieved by comparing the detected V_{in} signal V_{in} with a voltage reference $V_{boundary}$. Usually, $V_{boundary}$ is set to reflect the output voltage V_o with the same ratio as that reflects V_{in} . V_{ph} is high logic when V_{in} is higher than $V_{boundry}$ and is low logic when V_{in} is lower than $V_{boundry}$. The current zero crossing detection signal is generated by the auxiliary winding L. As shown in Figure 5, the control signal V_{ph} is the result of the magnitude comparison between V_{in} and $V_{boundry}$. The driving signals V_{G1} and V_{G2} are controlled by V_{ph} for the different operation modes alternately. The detected output signal V_{FB} is sent to the negative input of the error amplifier U_f . The error between V_{FB} and the set reference V_{ref} is amplified by the compensation networks C_f and an amplified error signal V_{comp} is achieved. The dc voltage signal V_{comp} applied to control the conduction period T_{ON} is achieved from V_{comp} through a control networks formed by resistors R_1 and R_2 and switch S_1 . Switch S_1 is controlled by the control signal V_{ph}. The proposed converter operates in buck mode when S_1 is OFF and operates in buckboost mode when S_1 is ON.

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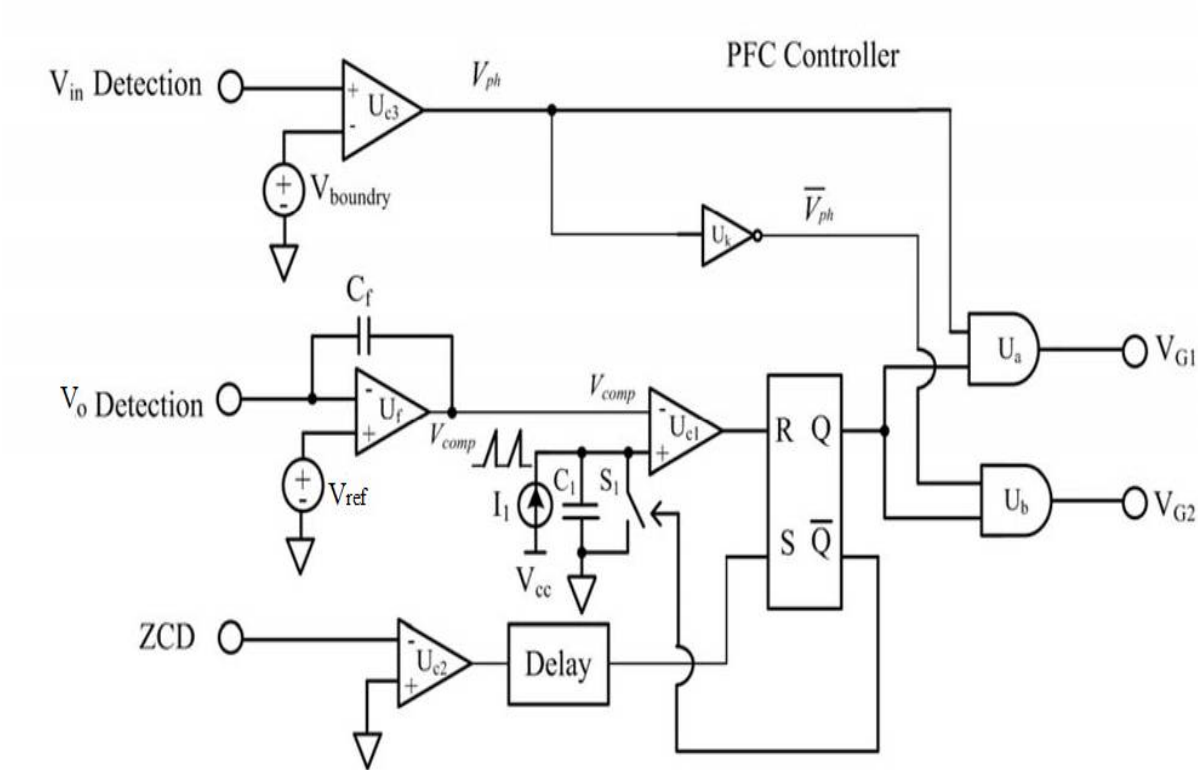

Fig .5 Constant On Time control Scheme for improved buck converter

b. Operation Stages

i. Positive Buck-Boost Operation Mode

When the input voltage V_{ac} is in positive half cycle and the magnitude of V_{ac} is smaller than V_o , the proposed converter operates in buck-boost mode. During this mode, switch Q_1 keeps OFF and switchQ_2 keeps switching. There are two stages when the proposed converter operates under this mode:

Stage 1: When switch Q_2 is ON, the proposed converter operates in stage 1. The inductor L is charged by V_{ac} through D_1 and D_6 , and i_L increases during this stage.

Stage 2: When switch Q_2 is OFF, the proposed converter operates in stage 2. The inductor L is discharged by V_o through D_o, and i_L decreases during this stage.

ii. Positive Buck Operation Mode

When the input voltage V_{ac} is in positive half cycle and the magnitude is larger than V_o, the proposed converter operates in buck mode. During this mode, switch Q_2 keeps OFF and switch Q_1 keeps switching. There are two stages when the proposed converter operates under this mode:

Stage 3: When switch Q_1 is ON, the proposed converter operates in stage 3. The inductor L is charged by $V_{ac}-V_o$ through D_1 and D_4 , and i_L increases during this stage.

Stage 4: When switch Q_1 is OFF, the proposed converter operates in stage 4. The inductor L is discharged by V_o through D_o and i_L decreases during this stage.

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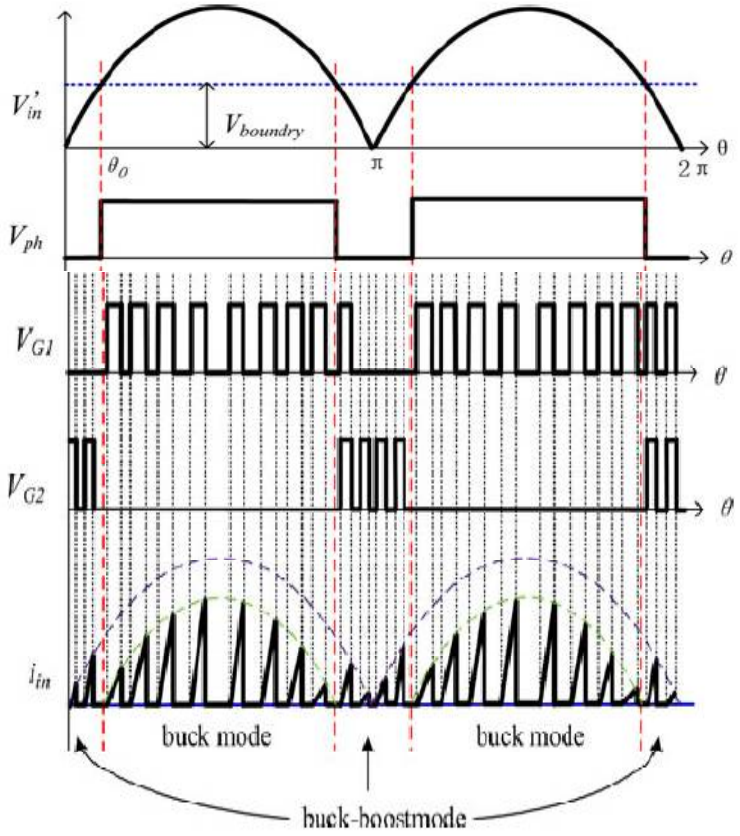

Fig .6 Waveforms for improved Buck PFC converter

When the input voltage V_{ac} is in negative half cycle, there also exist two operation modes of negative buck-boost operation mode and negative buck operation mode of the proposed converter. The negative half cycle operation processes of the proposed converter are similar to those of the positive half cycle. For simplicity, the negative operation processes are not depicted in detail here. Some key waveforms are shown in Fig. 6. As shown in Fig. 6, the control signal V_{ph} used to control the converter either in buck mode or buck-boost mode is achieved by comparing the detected V_{in} signal V_{in} with a voltage reference $V_{boundry}$.

C. Integrated Buck-Flyback PFC Converter

Another efficient possible solution for the problem in conventional buck PFC converter is an integration of flyback converter with buck power factor correction converter. Proposed integrated buck–flyback non isolated power factor correction converter is derived from a buck converter and a flyback converter. Derivation of the proposed converter is shown in the Figure 7.

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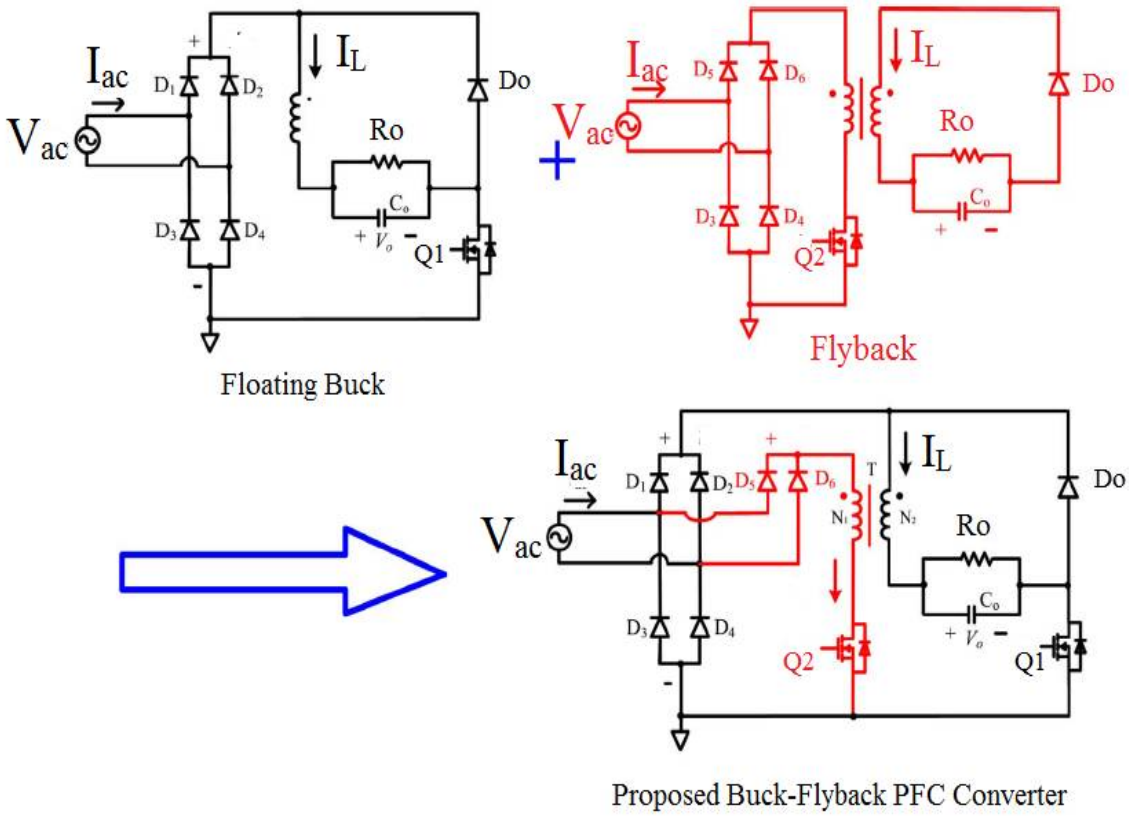

Fig .7 Derivation of the proposed integrated buck–flyback non isolated PFC converter.

Proposed integrated buck–flyback non isolated power factor correction converter is derived from a buck converter and a flyback converter. Derivation of the proposed converter is shown in the Figure 4.The structure of the proposed converter is very simple. It is formed by adding two rectifier diodes, one winding of the inductor, and one switch into the conventional buck PFC converter. The source nodes of the added switch Q_2 and the buck switch Q_1 are connected to the ground. The power loops of the buck mode and flyback mode are separated, and no additional component causing losses is added to the power loops. Obviously, the proposed integrated buck–flyback converter can achieve higher efficiency.

a. Control Strategy:

A constant on time control strategy is adopted which a sinusoidal input current that follows the input voltage waveform. The propoed converter is operated in Critical Conduction Mode thus ensures Zero Current Switching which reduces the switching losses. Circuitry for the improved Constant On Time (COT) control is shown in the Figure 8. The output current is detected for constant output current control of the LED load.

The control signal V_{ph} is the result of the magnitude comparison between V_{in} and $V_{boundry}$. V_{ph} is high logic when V_{in} is larger than $V_{boundry}$ and vice versa. The driving signals V_{G1} and V_{G2} are controlled by V_{ph} for the different operation modes alternately. The current zero crossing detection signal generated by the auxiliary winding of transformer T can be applied to both of the flyback and buck modes. As shown in Figure 8, the control signal V_{ph} is the result of the magnitude comparison between V_{in} and $V_{boundry}$. Vph is high logic when V_{in} is larger than Vboundry and vice versa. The

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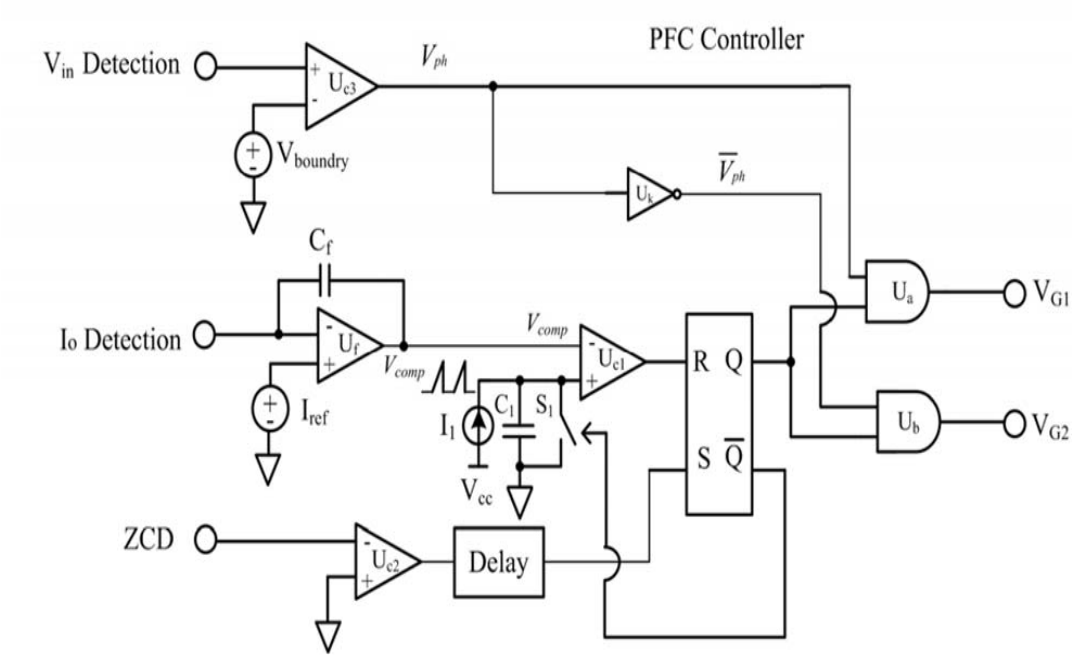

Fig .8 Improved Constant On Time control Scheme for integrated buck-flyback converter

Some key waveforms are shown in Figure 9. The proposed integrated buck–flyback non isolated PFC converter operates in buck mode when V_{ph} is in high logic level, while it operates in flyback mode when V_{ph} is in low logic level. Transition processes between those two modes are natural.

b. Operation Stages:

There are two different operation modes in a line period for the proposed converter. The proposed converter operates in flyback mode when the input voltage is lower than the output voltage and operates in buck mode when the input voltage is higher than the output voltage. Thus a current can be drawn from the supply even when the main buck converter is idle. In this way, there are no dead zones in the input current of the proposed converter. Therefore, it can achieve high power factor and pass the IEC61000-3-2 Class C limits easily. An improved Constant On Time (COT) control is applied to the proposed integrated Buck-Flyback power factor correction converter and forces it to operate in critical conduction mode (CRM). The peak current in working region can follow the input voltage, when output voltage V_o is constant. That means the input voltage and input current will be in phase and sinusoidal. Thus the power factor of the input will get improved with the proposed integrated Buck- Flyback power factor correction converter.

The operation process of the proposed converter in a line period can be divided into 12 operation stages, 6 for positive half cycle and 6 for negative half cycle.

i. Positive Half Cycle of AC input:

When the input voltage V_{ac} is positive and the magnitude of V_{ac} is smaller than V_o, the proposed converter operates in flyback mode. In this mode, switch Q_1 keeps off, and switch Q_2 keeps switching. There exist three stages when the proposed converter operates in this mode.

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Stage 1: Before this stage, the output diode D_o carries the output current, and switch Q_2 is off. Once the current flowing through D_o falls to zero, D_o turns off, and the equivalent capacitor of switch Q_2 is resonant with the magnetizing inductor of the transformer T, as shown in Figure 10(a)

Stage 2: When the voltage across the auxiliary winding of the transformer T falls to zero, the output of comparator U_{c2} flips from a low voltage level to a high voltage level. After a delay time, switch Q_2 is turned on at the valley of V_{DS_Q2}. The primary magnetizing inductor of transformer T is charged by V_{ac} through D_5 and D_4, as shown in Figure 10(b).

Stage 3: When switch Q_2 is off, the secondary magnetizing inductor of transformer T is discharged by V_o through D_o on the secondary side of the transformer, as shown in Figure 10(c).

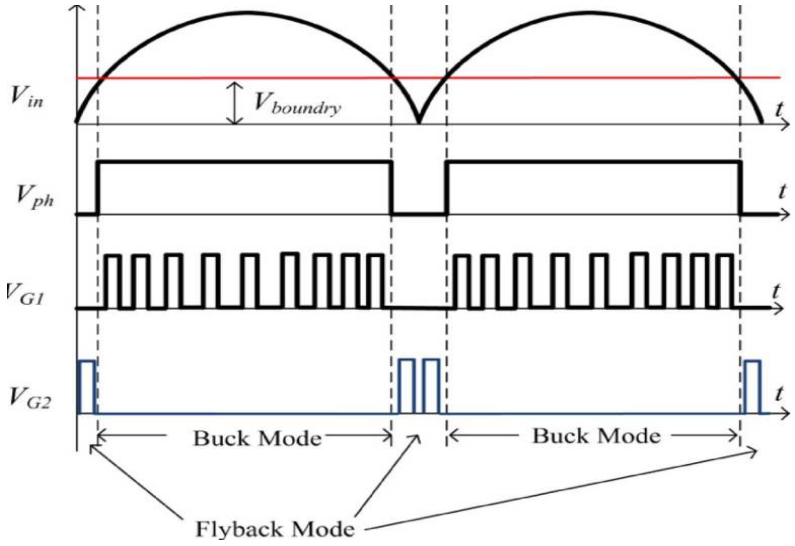
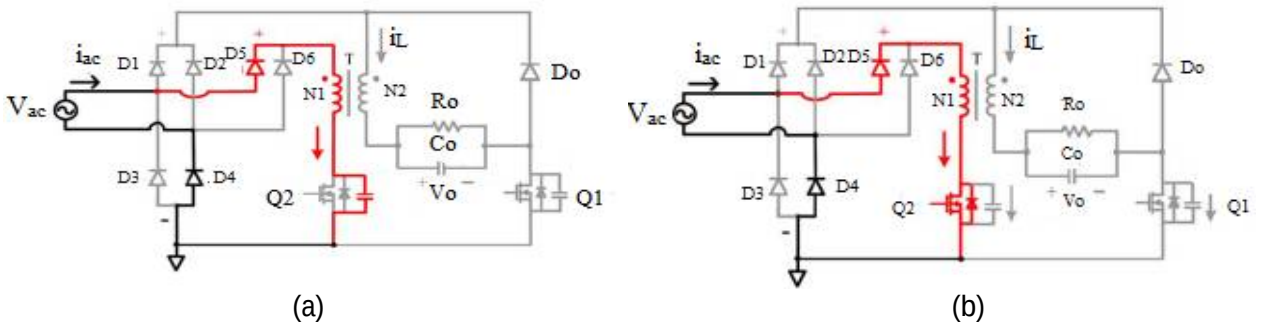


Fig .9 Key waveforms in COT control diagram.

When the input voltage V_{ac} is positive and the magnitude is larger than V_o, the proposed converter operates in buck mode. In this mode, switch Q_2 keeps off, and switch Q_1 keeps switching. There also exist three stages when the proposed converter operates in this mode.

Stage 4: Before this stage, the output diode D_o carries the output current, and switch Q_1 is off. Once the current flowing through D_o falls to zero, D_o turns off, and the equivalent capacitor of switch Q_2 is resonant with the magnetizing inductor of the transformer, as shown in Figure 10(d).



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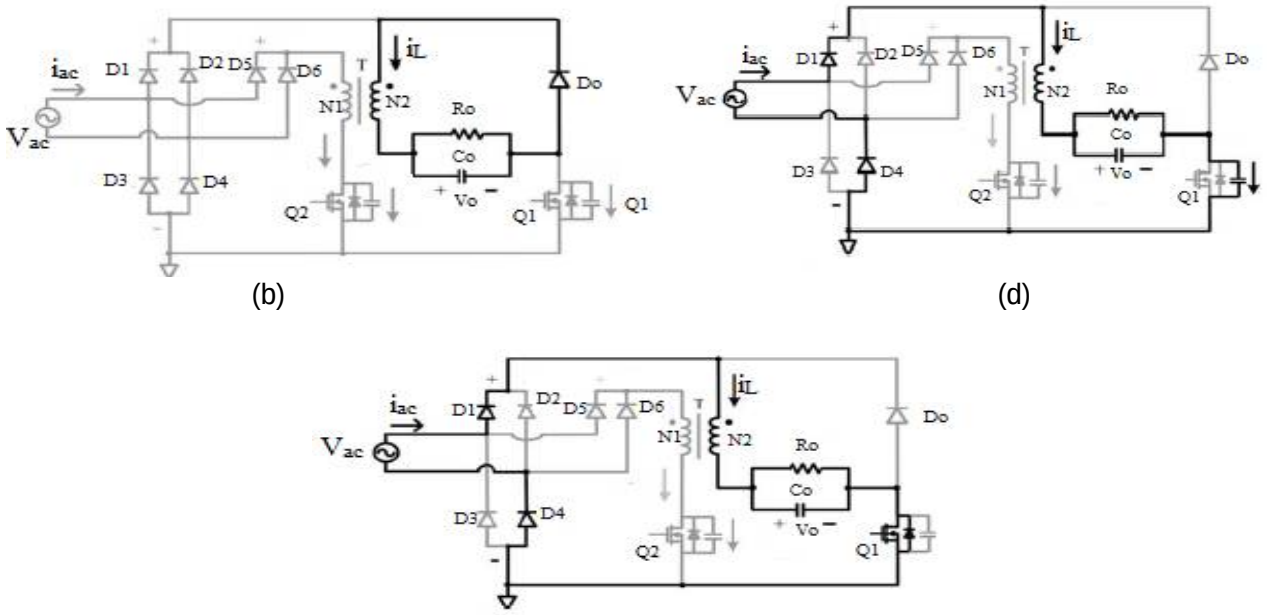
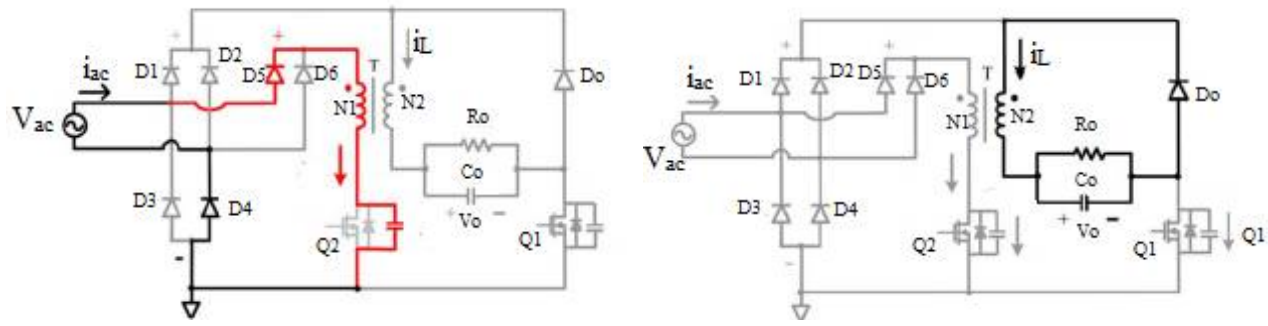


Fig .10 Equivalent circuits of the proposed converter for positive half cycle

Stage 5: When the voltage across the auxiliary winding of the transformer falls to zero, the output of comparator U_{c2} flips from a low voltage level to a high voltage level. After a delay time, switch Q_1 is turned on at the valley of V_{DS_Q1}. The secondary magnetizing inductor of transformer T is charged by $V_{ac} - V_o$ through D_1 and D_4, as shown in Figure 10(e).

Stage 6: When switch Q_1 is off, the secondary magnetizing inductor of transformer T is discharged by V_o through D_o as shown in the Figure 10(c)



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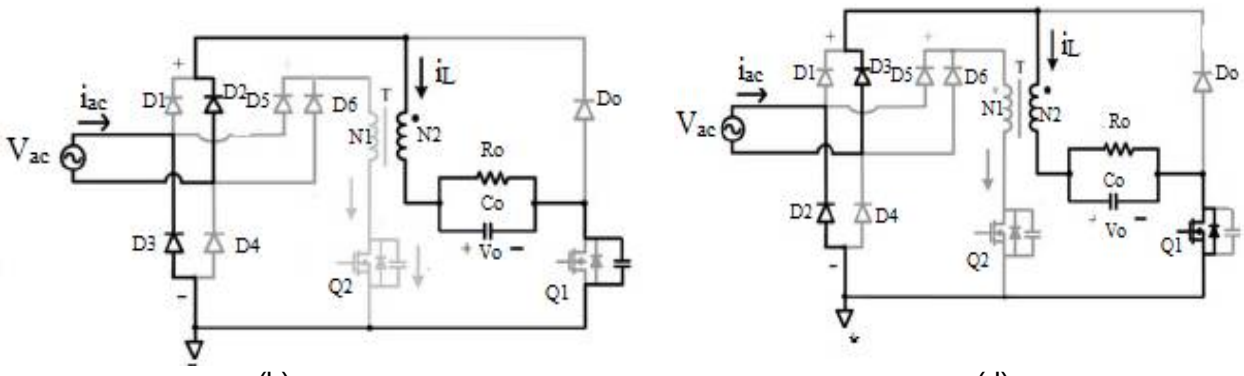

Fig .11 Equivalent circuits of the proposed converter for negative half cycle

ii. Negative Half Cycle of AC Input:

When the input voltage V_{ac} is negative, the proposed converter also operates in flyback mode and buck mode in different input voltage regions. The operation processes in negative half-cycle of ac input can also be divided into six operation stages, and the equivalent circuits are shown in Figure 11(a) to 11(d) The operation processes of the proposed converter in the negative half-cycle of ac input are similar to those of the positive half-cycle.

III. DESIGN CONSIDERATIONS

Design considerations for integrated Buck-Flyback non isolated PFC with COT control is made as follows.

A. Input Current Analysis:

When the input voltage is lower than the output voltage in half line cycle, the buck converter does not work. The conduction angle of the input current during buck mode equals ($\pi - 2\theta_0$). Assuming V_{im} is the amplitude of the line voltage, then, angle θ_0 is defined as

$\theta_0 = \arcsin(V_{boundry}/V_{im})$
$\theta_0 = \arcsin(V_o/V_{im})$ (1)

When the input voltage is higher than the output voltage, the buck converter begins working, and the slope of the inductor current i_{Ls} for the buck operating region in half line cycle is given by the expression

$L di_{Ls}(t)/dt = V_{im} |\sin(\theta)| - V_o, \quad \theta \in (\theta_0, \pi - \theta_0)$ (2)

where $\theta = \omega_l t$ and $\omega_l = 2\pi f_l$ is the line angular frequency. So, the peak value of the inductor current during switching cycle during buck mode can be modified as follows:

$I_{pk1}(\theta) = (V_{im} |\sin(\theta)| - V_o) T_{on} / L_s$ (3)

where L_s in the secondary winding inductance and T_{on} is the on-time of the switch, which is almost constant during half line cycle. The peak value of the inductor current during switching cycle during flyback mode can be written as follows:
$i_{pk2}(\theta) = (V_{im}.\sin\theta) T_{on} / L_p$ (4)

where L_p in the primary winding inductance
$D(\theta) = V_o / (V_{im} |\sin(\theta)|), \quad \theta \in (\theta_0, \pi - \theta_0)$ (5)

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Then, the average input current i_{av} of the buck converter is determined as follows:

$$i_{av}(\theta) = I_{pk1}(\theta)D(\theta)/2, \quad \theta \in (\theta_0, \pi - \theta_0) \tag{6}$$

B. Output Voltage Selection:

Within a half line cycle, the input current can flow only when the input voltage is greater than the output voltage. It should be noted that the PF is affected by the output voltage significantly. With an increasing output voltage, the PF decreases. Although lower output voltage results in higher PF, the efficiency of buck converter will decrease with the decrease of output voltage at same load. The output voltage is preferred to be set around 80 V considering the voltage stress of the output capacitor

C. Inductance Selection:

The input power *P*in is calculated as follows:

$$P_{in} = \frac{2}{\pi}\int_{\theta 0}^{\pi/2} iav(\theta)Vim.\sin\theta \, d\theta \tag{7}$$

Assuming η is the efficiency of the converter, the output power *Po* can be expressed as follows:

$$P_o = \eta.P_{in} = \frac{2\eta}{\pi}\int_{\theta 0}^{\pi/2} i_{av}(\theta).V_{im}.\sin\theta \, d\theta \tag{8}$$

By substituting (6) into (8) we will get

$$P_o = \eta.P_{in} = \frac{\eta Ton}{\pi Ls}\int_{\theta 0}^{\pi/2} (V_{in}.\sin\theta - V_o).V_o d\theta \tag{9}$$

During buck mode,

$$T_{off}(\theta) = \frac{Ipk1(\theta).L}{Vo} \tag{10}$$

Switching frequency as a function of time is given by,

$$f_s(\theta) = 1/(T_{on} + T_{off}(\theta)) = V_o/(T_{on}.V_{im}\sin(\theta)) \tag{11}$$

From (9) T_{on} can be expressed as

$$T_{on} = \frac{\pi LsPo}{\eta}\frac{1}{\int_{\theta 0}^{\pi/2}(Vim.\sin\theta - Vo).Vo \, d\theta} \tag{12}$$

Combining (11) and (12),

$$f_s = \frac{\eta.Vo^2}{\pi.Ls.Po.Vim.\sin\theta}\int_{\theta o}^{\pi/2} (V_{im}.\sin\theta - V_o) d\theta,$$
$$\theta_o \le \theta \le \pi - \theta o \tag{13}$$

Obviously, the lowest frequency in half line cycle appears at $\theta = \pi/2$. Therefore, the minimum frequency as a function of input voltage *V*im can be obtained when $\theta = \pi/2$

$$f_{s\text{-}min} = \frac{\eta.Vo^2}{\pi.Ls.Po.Vim-min}\int_{\theta o}^{\pi/2} (V_{im\text{-}min}\sin\theta - V_o) d\theta \tag{14}$$

Then, the transformer secondary winding inductance L_s is obtained as follows:

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$$Ls = \frac{\eta.Vo^2}{\pi.fs-min.Po.Vim-min} \int_{\theta o}^{\pi/2} (V_{im\text{-}min} \sin\theta - V_o)\, d\theta \quad (15)$$

where $V_{im\text{-}min}$ = 60. If the minimum switching frequency $f_{s\text{-}min}$ is assumed to be 10 kHz, output power is designed at 100W and the output voltage is designed at 60V. Then,

$\theta_o = \arcsin (V_o/V_{im})$

where V_{im} is 100V. θ_o is obtained as,

$\theta_o = 0.2\pi$

For an efficiency η of 0.96, the inductance is obtained as,

L_s=1 mH.

$L_p/L_s = (N_1/N_2)^2$ (16)

where N_1/N_2 is the turns ratio which can be taken as n. Chosing n as 2.

L_p = 4 mH

D. Output Capacitance Selection:

Output capacitor is designed by the equation,

$$C_f = \frac{I_O}{8 f_S . \Delta V_{Cf}} \quad (17)$$

where ΔV_{Cf} is usually considered as 5%–10% of the output voltage. This capacitor value is chosen to be higher than the one given by the above equation and

$I_o = P_o/V_o$

C_f = 150 µF

IV. SIMULATION RESULTS

The performance of the PFC converters and the COT control strategy are evaluated by conducting the Simulation analysis. MATLAB/Simulink version R2012a is used for simulation. The input given is 100 V and the parameters are designed for a 100 W, 60V topology.

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Table 1
SIMULATION PARAMETERS FOR CONVENTIONAL BUCK CONVERETER

Parameter	Value
Input voltage	100V
Inductance, L	1mH
Output Capacitor, C_o	150μF

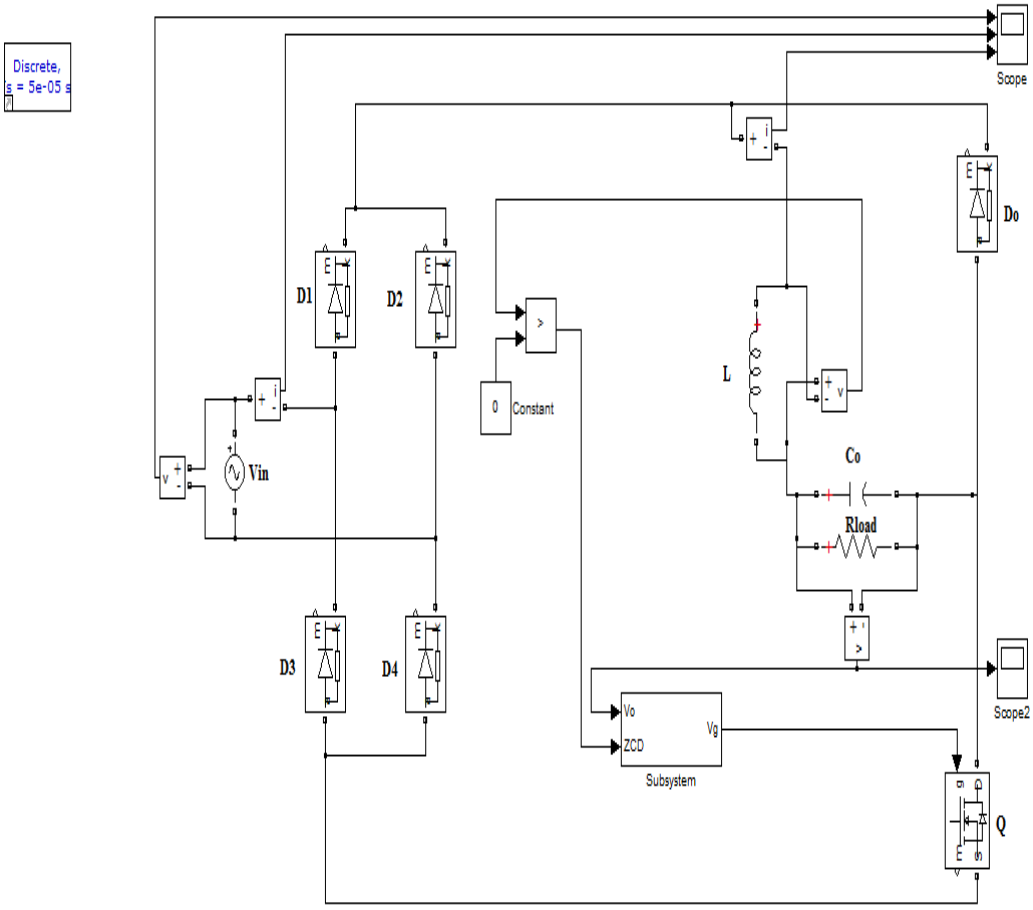

Fig .12 Conventional Buck PFC Converter Circuit

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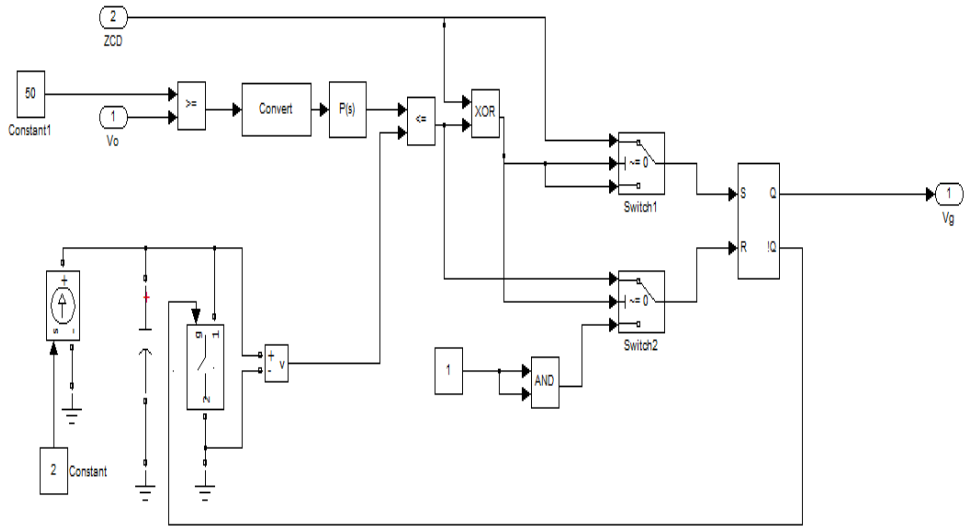

Fig .13 COT Controller for conventional Buck PFC Converter

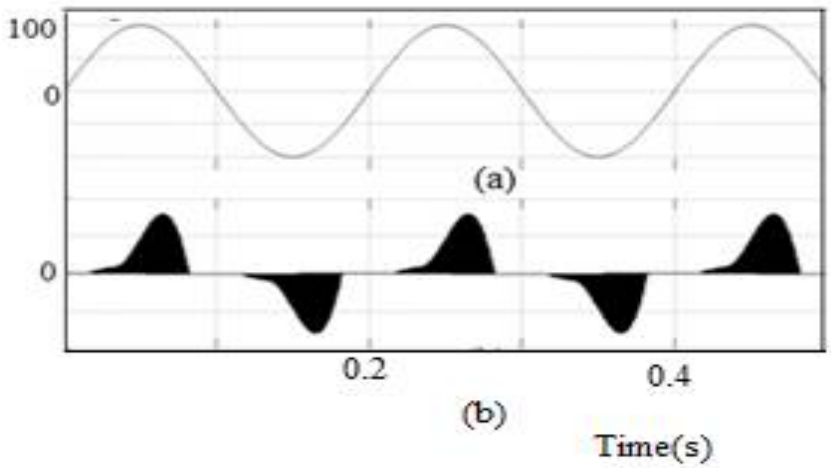

Fig .14 Input voltage, Input current and Inductor Current of conventional buck PFC converter at 100 V

Figure 14 shows the Input voltage and Input current waveforms of conventional buck PFC converter with COT control. We can see that there are significant dead zones in the ac input current waveform at the zero crossing points of input voltage.

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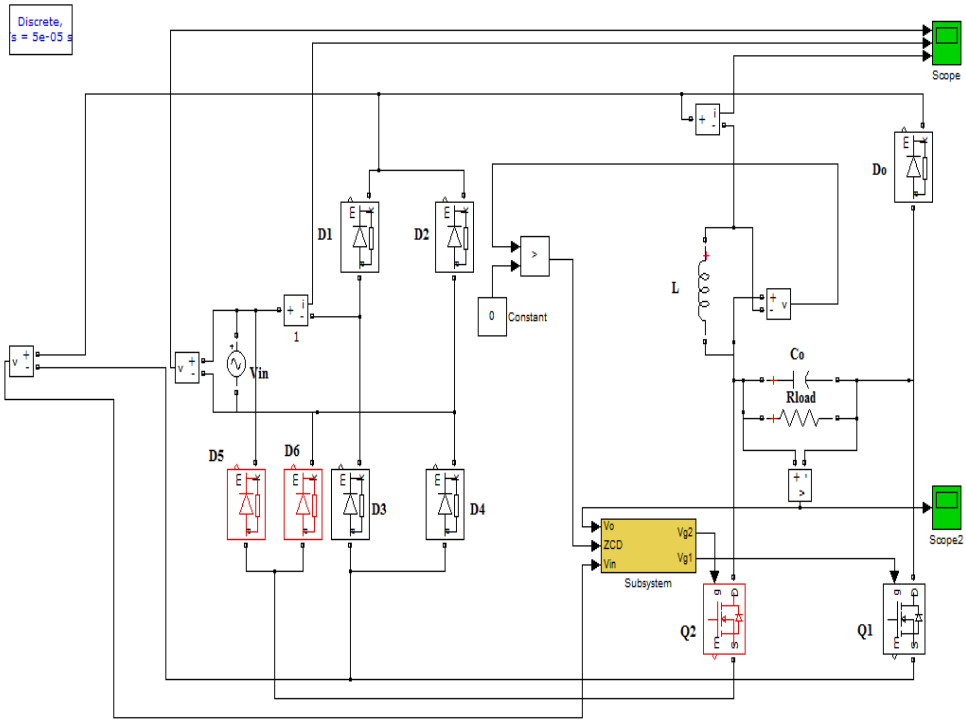

Fig .15 Improved Buck PFC Converter Circuit

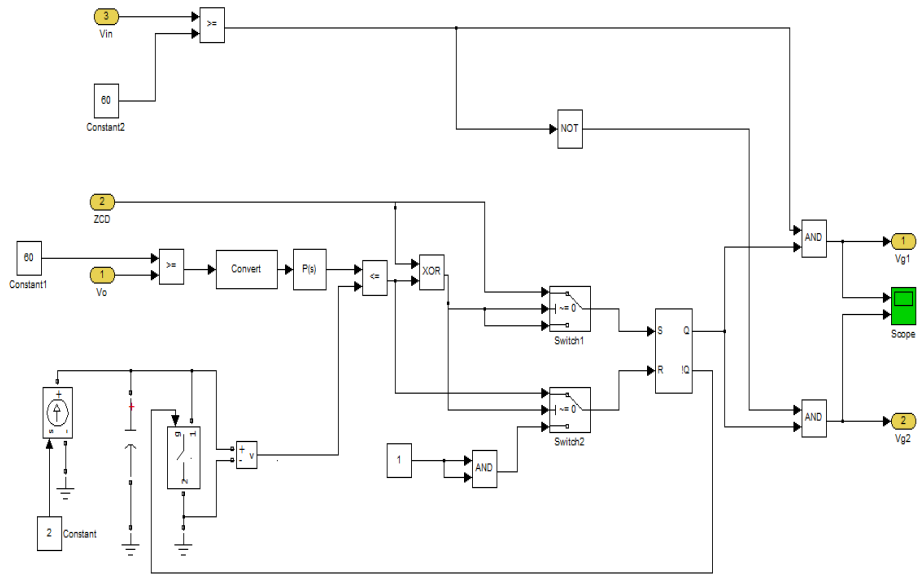

Fig .16 COT Controller for Improved Buck PFC Converter

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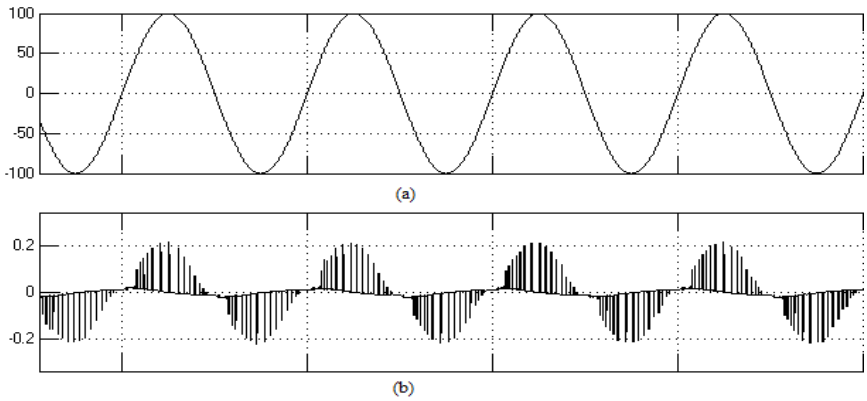

Fig .17 Input voltage and Input current of Improved Buck PFC converter at 100 Vac

Table 2
SIMULATION PARAMETERS FOR INTEGRATED BUCK- FLYBACK CONVERTER

Parameter	Value
L_p	1mH
L_s	4mH
Transformer Turns ratio, n	2
Output Capacitor, C_o	150μF
Switch Q_1, Q_2	IRF 840
Diode D_o	1N4007

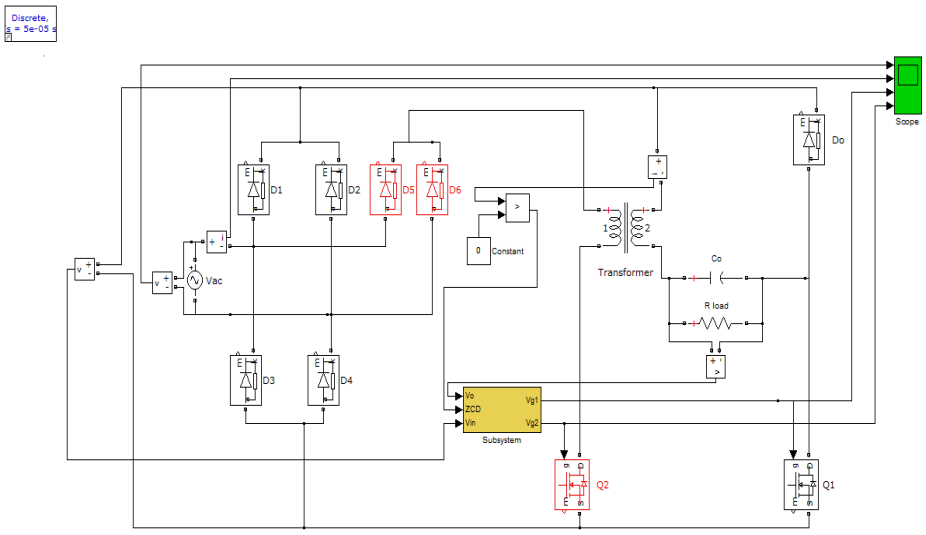

Fig .18 Integrated Buck-Flyback PFC Converter Circuit

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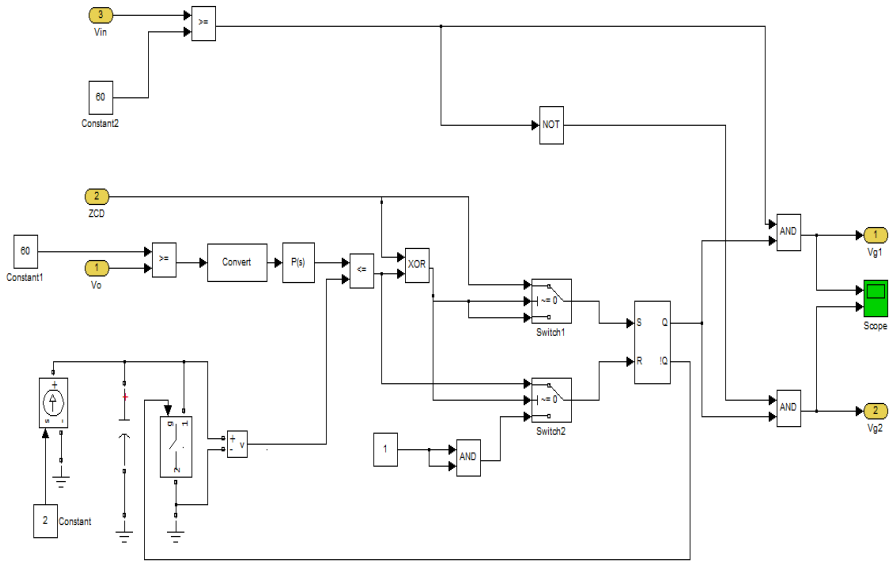

Fig 19 .COT Controller for Integrated Buck-Flyback PFC Converter

Figure 17 shows the Input voltage and Input current waveforms of improved buck PFC converter with COT control. Figure 20 shows the Input voltage and Input current waveforms of integrated buck-flyback PFC converter obtained from simulation. From fig.17 and fig.20 it is clear that the dead zone in the input current waveform is very much reduced in improved buck converter and proposed buck-flyback PFC converter. Also the input current is almost sinusoidal and the phase difference between the voltage and current is very much reduced.

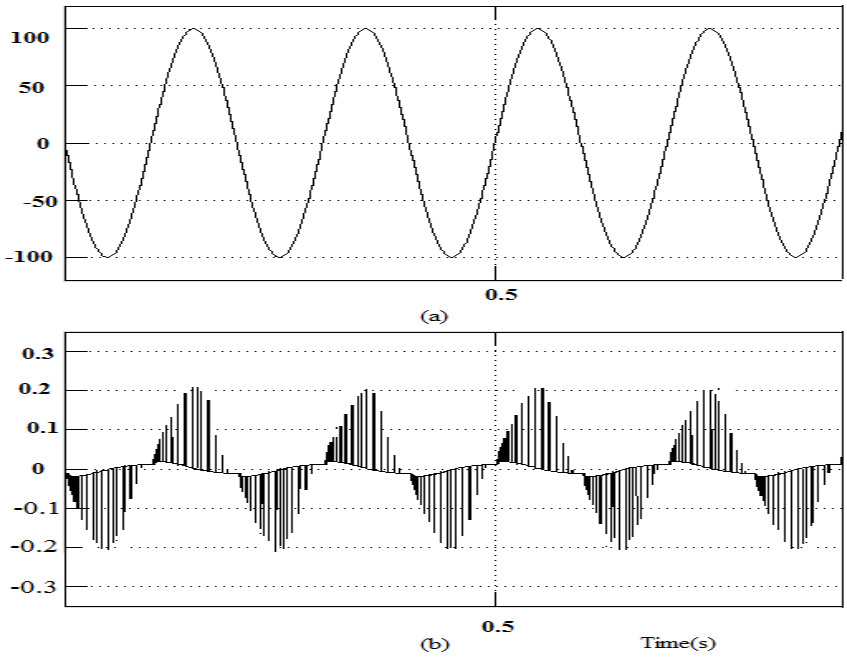

Fig .20 Input voltage and Input current of Buck-Flyback PFC converter at 100 Vac

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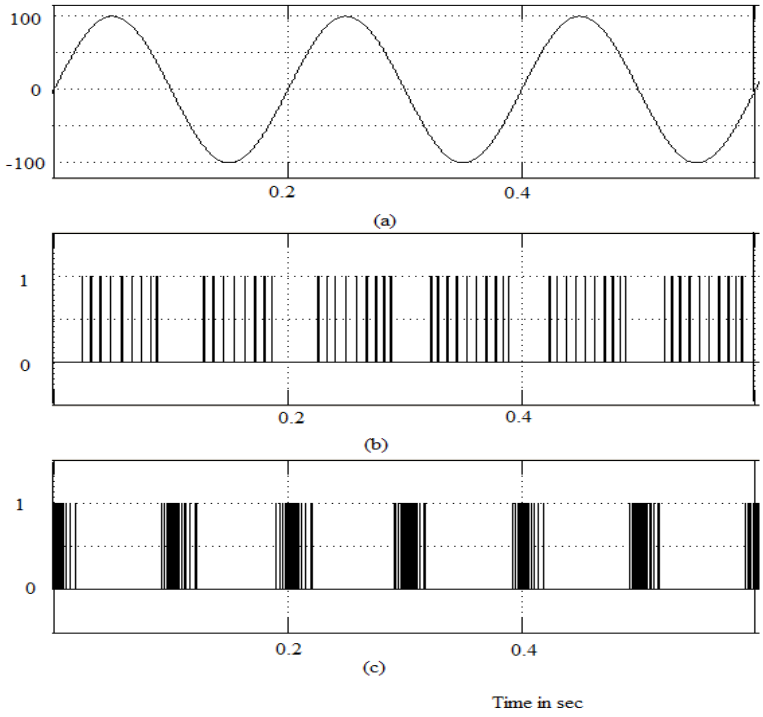

Fig .21 Input Voltage and generated switching Signals V_{g1} and V_{g2}

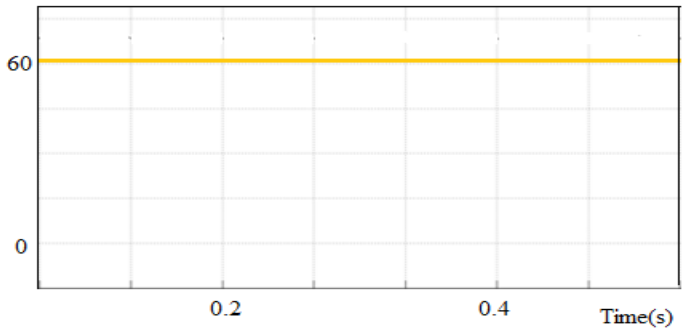

Fig .22 Output Voltage for 100 V_{ac}

V. EXPERIMENTAL RESULTS

Laboratory setup of the proposed Buck-Flyback converter prototype with 12V input supply is shown in Figure 23. A step down transformer was used to step down the input 230V to 12V input. PIC 16f877 microcontroller was used to generate the control signals for the buck and flyback switches.

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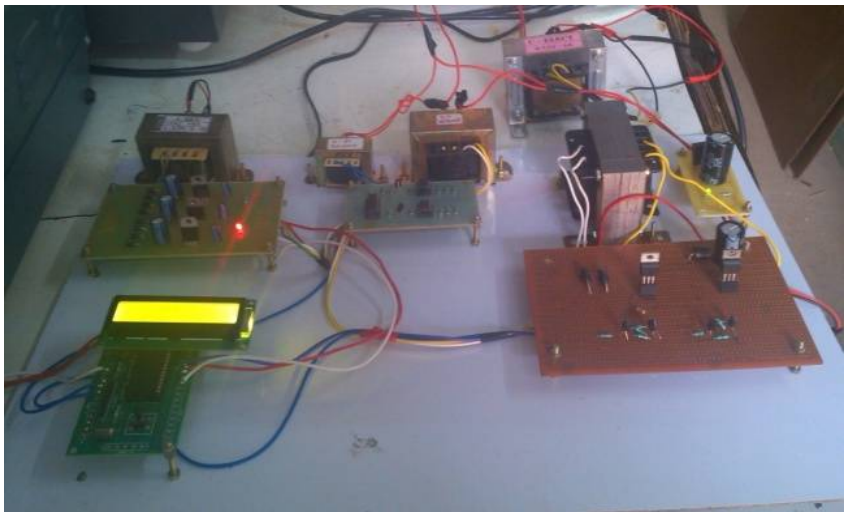

Fig .23 Laboratory Setup

VI. CONCLUSION

Power factor Correction converters with Constant On Time control(COT) are presented in this paper. Conventional buck PFC converter exhibits dead zones in its input current waveform. To overcome this problem improved buck converter and integrated non isolated buck–flyback PFC converter topology have been proposed. Improved buck converter operates either in buck mode or buck-boost mode depending on whether the input voltage is greater than or less than the output. Integrated buck-flyback converter operates in flyback mode when the input voltage is lower than the output voltage and operates in buck mode when the input voltage is higher than the output voltage. In this way, there will not be any dead zones in the input current of the proposed converters. Therefore can achieve high power factor and pass the IEC61000-3-2 Class C limits easily. Conventional Buck PFC converter and improved converters are simulated using MATLAB/Simulink. A 10W laboratory prototype of integrated Buck-flyback power factor correction converter with 12V input voltage was setup. PIC 16F877 is used to generate controlled switching signals for buck and flyback switches. Compared to conventional PFC topologies obviously the proposed converter can improve the PF greatly particularly at low line voltage.This topology could achieve high PF of 0.96. This proposed topology is very suitable for high-power non isolated LED drivers with high PF requirements. The proposed integrated non isolated buck–flyback PFC converter topology can also be extended to isolated topology by replacing the buck part with an isolated buck-type topology such as forward converter.

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