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# Post Silicon Recovery from Clock-Domain Crossing Failures in Multiclock SoCs

[1] E.Priyanga,[2] D.Jessintha

PG Scholar, Dept. of ECE, Easwari Engineering College, Chennai, Tamilnadu, India[1]

Assistant Professor, Dept. of ECE, Easwari Engineering College, Chennai, Tamilnadu, India[2]

**ABSTRACT:** Modern SoCs are very complex and work under different clock domains. Data is transferred from one domain to another domain, which needs to be synchronized. These signals produce Clock Domain Crossing Faults in fabricated chips. The careful post-silicon testing for multiclock circuits. Even when robust design methods based on synchronizers and design verification techniques are used, process variations can introduce subtle timing problems that affect data transfer across clock-domain boundaries for fabricated chips. This paper introduces methods for Detecting and locating the CDC faults and Post Silicon Recovery from CDC failures is ensured. In the proposed method, CDC faults are Detected using Scan Flip-flops and located using a CDC-fault dictionary, and their impact is masked using post-silicon clock-path tuning. To quantify the impact of process variations in the transfer of data at clock domain bound- aries of multiclock circuits and to validate the proposed error- recovery method, we conducted a series of HSpice simulations using a 45-nm technology. These results ensure the effectiveness of Post silicon Recovery in Multi Clock circuits.

**KEYWORDS**: Clock domain crossing, error recovery, fault detection, fault diagnosis.

## I. INTRODUCTION

Modern SOC integrated circuits now a days offers immense functionality and contain billions of transistors. However, high-speed communication between core blocks remains a major challenge. This problem is exacerbated when cores operate in separate clock domains and at different clock frequencies. In multiclock designs, a clock-domain crossing (CDC) occurs whenever data is transferred between clock domains. Depending on the relationship between the sender and receiver clock frequencies, there are lot of problems may arise when gets transferred from one module to another. Propagation of metastability, data loss, and data incoherency are three fundamental problems of multiclock design, all of which are caused by CDC faults [2].

To reduce the probability of a design, we need to design synchronizers and need to place them across the clock boundaries. Inorder to avoid data loss and to get proper transmission and reception of data in multiclock designs, designers also rely on appropriate CDC protocols. Data incoherency, which mainly occurs where CDC signals reconverge, can be avoided by making the architecture design more vulnerable to the variable delays which occurring at the reconvergent paths[3]. Verification techniques and commercial verification tools enable designers to check designs for CDC-associated problems and verify the correct- ness of functional behavior [4]–[6].

If CDC errors are not identified at the early stage of design means, it will lead to the functional errors during post silicon level. To avoid the metastability that occurs in multiclock circuits, and also to increase the mean time between failures (MTBF), designers typically employ different types of synchronizers, among which the most commonly used is a pair of flip-flops residing on the clock boundaries.

As we move toward higher integration levels and even smaller technology nodes, errors that occur due to process variations, design margin limitations, and operating conditions are begin to play more important role in multiclock circuits. Consequently, circuits that were deemed to be fault free through CDC analysis during presilicon validation may exhibit CDC errors after fabrication.

Therefore, the effect of process variations on correct operation of multiclock circuits must be investigated, and there is a need for testing techniques for CDC faults. A scan flip-flop method, which is used for detecting CDC faults, was recently proposed in [7]. A commercial ATPG tool and a popular logic simulator were used to extract, from a pattern repository, a set of test patterns that detect CDC faults. However, repeated conjuration of the simulator

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leads to long runtimes. Moreover, the tests derived in [7] do not target at-speed transfer of transition of data required between the clock domains; hence, their effectiveness for high-speed circuits is questionable.

## II. RESOLVING METASTABILITY

Synchronizers are used to veil the effect of metastability in multiclock circuits [3]. It is expected that in a design, including synchronizers, the output of a flip-flop rarely becomes metastable, e.g., only once in every MTBFs years, typically, 20 years for clock frequencies of 400 MHz [8]. However, for faster clocks, the probability of observing metastability at the outputs of flip-flops increases rapidly, e.g., the MTBF drops to 1 min for a clock frequency of 1 GHz [8].

In existing method both asynchronous and synchronous handshaking mechanisms between different clock domains has been used to avoid metastability problems. In the asynchronous handshaking mechanism, for each data transmission, a request needs to be first sent from the sender to receiver. After sending the request, the sender sends the data to the receiver. After getting data from sender the receiver will need to send an acknowledgement to the sender. After that receiving the acknowledgement, the sender can send another request to start next transmission. To inoculate the handshaking process against the metastability of the request and acknowledge signals, synchronizer flip-flops are inserted in the circuit [9].

The two flip-flop synchronizers is most commonly used in multiclock circuits to avoid metastability [8]. However, fast clocks, low supply voltages, and extremely low or high temperatures decrease MTBF and necessitate the use of additional synchronizer flip-flops. To decrease MTBF, four flip-flop synchronizers may be used in clock boundaries [8].

The flip-flops used as synchronizers must be more complicated to variations in process, temperature, and voltage. Ideally, the setup and hold time of synchronizer flip-flops should be zero. However, it is costly to use synchronizer flip-flops.

## III. CDC FAULT MODEL

The proper operation of flip-flops in a synchronous circuits mostly based on the stability of its input signal for a certain period of time before (setup time) and after (hold time) its clock edge. If setup and hold times are contravene, then the flip-flop output may oscillate for an indefinite amount of time, and may or may not settle to a stable value before the next active clock edge. The unstable behavior of signal lines is known as metastability. Fig. 2(a) shows an example of a multiclock circuit in which signal $S$ is transmitted by $Clk_1$, and needs to be received by $Clk_2$. As shown in Fig. 2(b), if a transition on $S$ signal arises very close to the active edge of $Clk_2$, a setup-time violation occurs, which may lead to metastability on $Q_2$ .CDC faults mainly occur due to setup and hold-time violations on flip-flops residing at clock boundaries. If a flip-flop experiences a setup-time violation, it does not sample a change in value at its data input. In a hold-time violation, however, it may incorrectly capture a data change at its input. We next describe the fault model for each case.

### A. Setup-Time Violation

Fig.2 illustrates sample waveforms for the CDC circuit of Fig. 1(a). As shown in Fig. 2(a), if signal $S$ experiences an unexpected delay and its value changes during the setup- time window of the receiver flip-flop, the receiver flip-flop may capture the value 0 even though the expected value is 1. Since the output of the sender flip-flop does not change in the subsequent clock cycle, $Q_2$ gets its expected value of 1 in the next clock cycle. In this case, the setup-time violation of the receiver flip-flop can be modeled as a slow- to-rise fault with a delay of one clock cycle. However, if the width of the transition on the output of the sender flip-flop is not long enough, the receiver flip-flop will not capture that transition, and remains unchanged. In this case, the setup-time violation of the receiver flip-flop can be modeled by a slow- to-rise fault with infinite delay. In practice, safe passage of one CDC signal between two clock domains through a two- flip-flop synchronizer requires that the CDC signal be 1–1.5 times wider than the receiver clock period [16].In general, if a value change of a CDC signal $S$ violates the setup time of the receiver flip-flop, then the faulty behavior can be modeled as a transition (slow-to-rise or slow-to-fall) fault with a delay of $k$ clock cycles, where $k$ = 1 if the pulse observed in signal $S$ is at least 1.5 times wider than the receive

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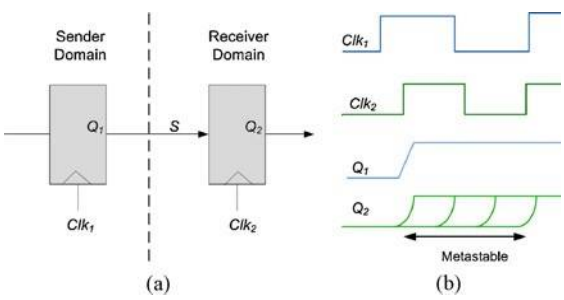


Fig. 1. Example of a CDC circuit and metastability. (a) CDC circuit. (b) Metastability on $Q_2$

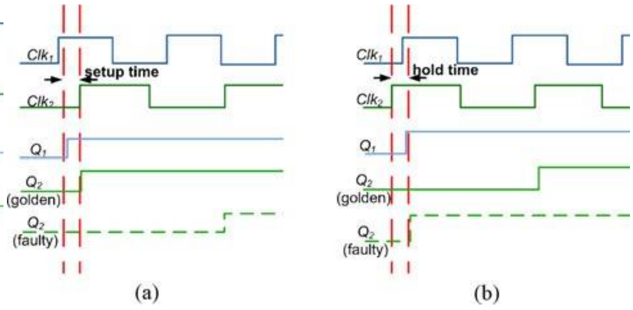


Fig. 2. Timing waveforms showing setup and hold-time violations for the circuit in Fig. 2(a). (a) Setup-time violation. (b) Hold-time violation

clock period. Otherwise, $k = \infty$. In the rest of this paper, a CDC fault arising due to setup-time violations will be referred to as a S-CDC fault.

### B.Hold-Time Violation

If a flip-flop experiences a hold-time violation, data changes on its input may be incorrectly sampled. Fig. 2(b) shows another sample waveform for the CDC circuit of Fig. 1(a). If signal $S$ changes during the hold-time interval of the receiver flip-flop, an incorrect change on the output may be observed. The receiver flip-flop gets an output value of 1 one clock cycle earlier than expected. In this case, the hold-time violation at the receiver flip-flop can be modeled as a transient fault with a duration of one clock cycle. Similarly, if the output of the sender flip-flop changes before the next active edge of the receiver flip-flop, the receiver flip-flop captures the transition of signal $S$, and the hold-time violation of the receiver flip- flop can be modeled as a transient fault with a duration of one clock cycle. H-CDC faults used to refer to the CDC fault arising due to hold-time violations. In this paper, we focus on S-CDC faults and leave the treatment of hold-time violations for future work.

## IV. FAULT DETECTION METHOD

The setup time CDC(S-CDC) faults are mostly concentrated in this paper. Here TDF ATPG tool cannot be used to detect S-CDC faults. It typically launches a transition at the fault site and propagates it to an observable output, i.e., either a scan flip- flop or a primary output. While these steps are also necessary to detect S-CDC faults, they are not sufficient. The detection of S-CDC faults requires fault excitation and propagation through paths from the sender domain. However, this requirement is not always met when TDF ATPG tools are used for test generation.

There are two famous methods of TDF which are used todetect S-CDC faults. They are Launch-on-shift (LoS) and launch-on-capture (LoC). In LoS, the second pattern of a two-pattern test is obtained by a one-bit shift of the first pattern. However, in the LoC scheme, the second pattern is obtained from the circuit response to the first pattern. Although LoS usually provides higher delay-fault coverage and offers ease of test-generation compared to LoC, it requires significant design effort to achieve at-speed switching of the scan-enable signal. Therefore, due to the area overhead and design-time overhead of the LoS method, LoC is preferred to LoS [17]. In this paper, we only consider LoC for detecting S-CDC faults.

### A. Test Generation Process

In this section, we discuss our test-pattern generation method, which is referred to as CDC-oriented triple-capture (CoTC). To describe the testing method to detect S-CDC faults, we use the simple multiclock domain circuit, shown in Fig. 4. In this circuit, for the sake of clarity, only the flip- flops at clock boundaries are shown. Note that throughout this paper, we consider a single-fault model. In this paper, no assumptions are made or restrictions are placed on the clocking scheme. The clock signals are fed either by different PLL sources, or by a common PLL source but with different phases and frequencies. We assume that the frequency of the clock signal of the sender (receiver) domain is an integral multiple of the clock frequency of the receiver

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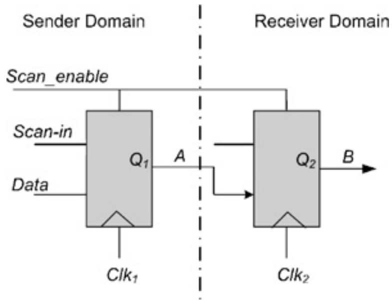


Fig. 3. CDC example for illustrating the proposed ATPG method.

(sender) domain. Accordingly, the phase difference between sender and receiver clocks may not lead to any setup and hold- time violation problem if there is no such violation in the first few clock cycles. To resolve the violation that may occur in the first few clock cycles due to the small related phase of sender and receiver clocks, the use of conflict detectors have been proposed in literature [8]. A conflict detector identifies when the sender and receiver clocks are dangerously close to each other. In the case of imminent problem, the clock signal of the receiver domain is delayed.

Assume that we want to target the S-CDC fault modeled by a slow-to-rise fault at the output of the receiver flip-flop (signal $B$) in the circuit, shown in Fig. 4. To detect this fault, first a rising transition must be generated on $A$, and then this transition must be propagated to $B$ in the next active edge of $Clk_2$. Note that the transitions on $A$ and $B$ must be at-speed with respect to $Clk_1$ and $Clk_2$, respectively. The clock frequencies of the sender and receiver domains, $F_S$ and $F_R$, respectively, must be considered in CoTC to generate test-patterns targeting S-CDC faults. We assume that these frequencies are specified by the designer, and therefore are known during test-pattern generation. We next describe the steps for each case. In each step, $A$ and $B$ keep their values, unless otherwise mentioned. Note that, in this paper, we consider separate scan-chain for each clock-domain. To apply detection, diagnosis, and recovery procedures for CDC faults, we merge all the scan-chains by connecting the scan- out of each chain to the scan-in of another chain. A small amount of multiplexing is assumed so that the scan-in and scan-out signals can be kept separate if the clock domains are to be tested separately for intra-domain faults. The hardware overhead is negligible because the multiplexing is done only for the scan signals and not for the functional I/Os. In addition, test-mode and test-clock input pins of each scan-chain are fed by the common test-mode and test-clock signals, respectively.

***1*)case 1: $F_S = F_R$*:** The first case deals with test- pattern generation for multiclock circuits in which the flip-flops residing in sender and receiver boundaries operate at same clock frequency, i.e., $F_S = F_R$. In this case, to ensure an at-speed transition on $A$ with respect to $Clk_1$, and an at-speed transition on $B$ with respect to $Clk_2$, we need to apply four test vectors instead of the two that are applied by the traditional LoC method. Steps 2 and 3 ensure that the transitions on $A$ and $B$ are at-speed with respect to $Clk_1$ and $Clk_2$, respectively. Fig. 5(a)–(d) shows the active paths highlighted in bold for the four steps needed to detect the CDC fault.

The four steps in CoTC to target the S-CDC fault modeled by a slow-to-rise fault on $B$ are as follows.

1) *Step 1)*: Shift vector $V_1$ to the circuit in scan mode such that $A$ and $B$ both get the value 0 in this step.
2) *Step 2)*: Switch to functional mode and generate vector $V_2$ such that $A$ and $B$ are both 0.
3) *Step 3)*: Operate in functional mode and generate vector $V_3$ such that in this step, the values on $A$ and $B$ are 1 and 0, respectively. This step ensures that a transition is launched at-speed across the CDC.
4) *Step 4)*: Operate in functi7onal mode and generate vector $V_4$ such that $B$ gets the value 1.

If the flip-flops residing in sender and receiver boundaries operate at the same clock frequency, the S-CDC fault modeled by a slow-to-rise fault on signal $B$ can be detected by applying vectors $V_1$ to $V_4$ (as discussed above) in four consecutive clock cycles. During scan mode (Step 1), a common shift clock signal is applied to both sender and receiver domains but in Steps 2–4; the circuit operates in functional mode and we apply $Clk_1$ and $Clk_2$ to the first and second clock domains, respectively. Note that each of vectors $V_1$ to $V_4$ includes two parts; the first part includes the values of the flip-flops and the second part includes the values of the primary inputs of the circuit in each step.

**2) Case 2: $F_R = M \cdot F_S$ :** In this case, the frequency of functional clock $Clk_2$ is an integer multiple of the frequency of functional clock $Clk_1$.To target the S-CDC fault modeled by a slow-to-rise fault on $B$ of Fig. 4, first a rising transition must be generated on $A$, and then this transition must be propagated to $B$ in the next active edge of

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$Clk_2$. The transitions on $A$ and $B$ must be at- speed with respect to $Clk_1$ and $Clk_2$, respectively. Therefore, to generate test-patterns to detect such faults, the following steps are necessary.

1) *Step 1*: Shift a vector to the circuit in scan mode such that $A$ and $B$ both get the value 0 in this step.
2) *Step 2*: Switch to functional mode and apply one functional clock cycle using $Clk_1$ and $M$ functional clock cycles using $Clk_2$. $A$ and $B$ should get the value 0 in these clock cycles. This constraint is ensured using a justification procedure. Note that in this case $F_R = M \cdot F_S$, and therefore while an at-speed transition is generated on $A$ with respect to $Clk_1$, $M$ clock cycles using $Clk_2$ are applied to the circuit as well.
3) *Step 3*: Operate in functional mode and apply one functional clock cycle using $Clk_1$ and one functional clock cycle using $Clk_2$. In this step, the values on $A$ and $B$ should be 1 and 0, respectively (ensured via justification).
4) *Step 4*: Operate in functional mode and apply one functional clock cycle using $Clk_2$. $B$ should get the value 1 in this step.

3) **Case 3: $\mathbf{F_S = N \cdot F_R}$:** The third case occurs when the sender domain operates $N$ times faster than the receiver domain, where $N$ is an integer. Similar to the previous cases, to detect the slow-to-rise S-CDC fault on $B$ of Fig. 4, first a rising transition must be generated on $A$, and then this transition must be propagated to $B$ in the next active edge of $Clk_2$. As noted above, the transitions on $A$ and $B$ must be at-speed with respect to $Clk_1$ and $Clk_2$, respectively. The steps taken in this case are as follows.

1) *Step 1*: Shift a vector to the circuit in scan mode such that $A$ and $B$ both get the value 0 in this step.
2) *Step 2*: Switch to functional mode and apply $N - 1$ functional clock cycles using $Clk_1$ and one functional clock cycle using $Clk_2$. $A$ and $B$ should get the value 0 in these clock cycles.
3) *Step 3*: Operate in functional mode and apply one functional clock cycle using $Clk_1$. In this step, $A$ should get the value 1.
4) *Step 4*: Operate in functional mode and apply one functional clock cycle using $Clk_2$. $B$ should get the value

Note that in all the cases discussed above, Step 2 ensures an at-speed transition on signal $A$. In practice, if $A$ does not drive any logic in the sender domain, any delay-fault that leads to a delayed transition on $A$ will not be detected if Step 2 is not taken.

***B.* Test Application Procedure**

To test a multiclock circuit using the test patterns generated by CoTC, the relative frequencies of sender and receiver domains should be considered. Similar to the test generation process that was discussed in Section V-A, based on the values of $F_S$ and $F_R$, different cases may arise for applying the CoTC patterns. In this section, we discuss the case where the sender and receiver domains operate at the same clock frequencies. Other cases can be treated using a similar procedure.

**Case 1: $\mathbf{F_S = F_R}$:** To test such circuits using the CoTC test patterns, the following steps should be taken.

a) *Step 1*: Set the circuit to scan mode. Scan in the initialization vector ($V_1$), and set the values on primary inputs.
b) *Step 2*: Switch to functional mode. Insert dummy cycles if needed to give scan-enable (*SE*) time to flip. Operate in functional mode and apply three functional clock cycles using $Clk_1$ and three functional clock cycles using $Clk_2$. Recall that we applied a total of three functional clock cycles using $Clk_1$ and three functional clock cycles using $Clk_2$ during test-pattern generation for this case (Steps 2-4 of Case 1 in Section V-A).
c) *Step 3*: Switch to scan mode and shift out the results.
This step can be overlapped with Step 1 to apply another test-pattern to the circuit.

## V. FAULT DIAGNOSIS AND RECOVERY

If a CDC fault is detected, post-silicon fault diagnosis and error recovery must be initiated to ensure correct operation. Fault diagnosis is necessary for the identification of manufacturing defects, and accordingly speeding-up yield ramp-up. Information provided by the diagnosis process is used in the physical inspections of the circuit. During the failure analysis process, it is important to locate the cause of failures quickly and accurately. Fault location may be required to analyze the defect causing the faulty behavior, reconfigure the circuit to mask the faulty behavior of the circuit, or replace the faulty sub circuit [18], [19].

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### A. Proposed Fault Diagnosis Method

Fault diagnosis methods can be categorized into two categories: cause–effect and effect–cause approaches [20]. In cause–effect methods, a fault dictionary is used for fault location. Effect– cause methods do not need a fault dictionary. These methods start from faulty outputs of the circuit under test and reason back through the logic to identify possible fault candidates. In this paper, we propose a cause–effect approach for the diagnosis of S-CDC faults, since it is potentially faster if a compact dictionary can be generated. Locating a fault using a fault dictionary requires applying the vectors included in the fault dictionary to the circuit-under- test (CUT) and comparing the responses of the observable outputs with the values stored in the fault dictionary. Full- dictionaries include the response of CUT to a given test set in the presence of each fault. Although fault diagnosis methods that use full-dictionaries provide high resolution, these methods suffer from the large size and high generation time of fault dictionaries [21].

To overcome the above problem, pass–fail dictionaries have been proposed in the literature [22]. A pass–fail fault diction -nary contains a single bit for each fault $F$ and test vector TV pair. This bit shows whether fault $F$ is detectable by applying test vector TV to the CUT. For large circuits, pass– fail dictionaries are preferred to full-dictionaries, even at the expense of some degradation in fault resolution.

**1) *Fault Dictionary Design:*** The proposed fault dictionary includes a set of test patterns, a signature of the expected response of the CUT to each test pattern, and the CDC faults that can be detected by each pattern. Obviously, this dictionary is smaller than a full-dictionary that includes the response of the CUT to each test pattern in the presence of each fault.

To generate the CDC-fault dictionary, the following steps should be taken.

a) *Step 1*: First, CoTC is applied to the CUT and up to 255 test patterns are generated for each detectable S-CDC fault. Although this method is general for any number of test patterns, 255 was deemed to be sufficient in our work. Set $P_i$ ($1 \leq i \leq N$ , $N$: number of S-CDC faults) includes all patterns generated by CoTC to detect S- CDC fault $\boldsymbol{f_i}$

b) *Step 2*: A subset of the patterns generated in Step 1 are selected such that by using the selected patterns, any two S-CDC faults $\boldsymbol{f_i}$ and $\boldsymbol{f_j}$ are distinguishable from each other. In this step, $P_{i,j}$ is generated for each pair of faults $\boldsymbol{f_i}$ and $\boldsymbol{f_j}$ and includes all the patterns generated by CoTC detecting exactly one among $\boldsymbol{f_i}$ and $\boldsymbol{f_j}$.

c) *Step 3*: In this step, a minimum set covering algorithm is applied to the set of test vectors generated in Step 2 for each pair of S-CDC faults to select a minimal set that distinguishes all S-CDC faults from each other. These patterns are stored in the CDC-fault dictionary.

d) *Step 4*: For each test pattern selected in Step 3, the expected response of the CUT is determined by logic simulation. The response includes the values of all observable points, including primary outputs and scan flip-flops.

e) *Step 5*: To reduce the storage required for the expected response of the CUT for each test pattern (evaluated in Step 4), a signature of the expected values of primary outputs and flip-flops is extracted and stored in the distinguishable dictionary along with each test pattern.

f) *Step 6*: Along with each test pattern and the expected response of the CUT to that pattern, a list of S-CDC faults that can be detected by that pattern is stored in the CDC-fault dictionary.

As discussed in Step 5, to reduce the size of the CDC-fault dictionary, instead of expected outputs of the CUT to each test pattern, a signature of those values are stored. We use a 64-bit cyclic redundancy check (CRC) code for response compaction and encode the sequence of primary outputs and the sequence of flip-flip outputs related to each test pattern, separately. The signatures and their related test patterns are stored in the CDC-fault dictionary.

**2) CDC Fault Diagnosis:** Using the fault dictionary generated by the method discussed in the previous section, all detectable CDC faults can be located. The CDC-fault dictionary generated for each circuit includes a number of test patterns (values that should be applied to the primary inputs, and initial state of flip-flops) along with a signature of expected values of the observable points of the circuit (primary outputs and scan flip-flops), while applying each test pattern to the circuit and the list of CDC faults that can be detected by applying each test pattern. To locate a CDC fault, the clock frequencies of sender and receiver domains should be considered. Based on the values of $F_S$ and $F_R$, different cases may occur. We discuss below the case where both sender and receiver domains operate at the same clock frequency. Other cases can be treated similarly (as in Section V). To locate a CDC fault, the test patterns included in the generated fault dictionary should be applied to the CUT, one after another, until the exact location of that CDC fault is diagnosed or no other test pattern is left in the fault dictionary.

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Before applying the fault diagnosis algorithm to the CUT to locate a CDC fault, all of the detectable CDC faults are included in the suspect list and are considered as the candidate locations. Then the following steps are taken while applying each test pattern included in the fault dictionary to the CUT.

a) *Step 1*: Set the circuit to scan mode. Scan in the initialization vector ($V_1$), and set the values on primary inputs.

b) *Step 2*: Switch to functional mode. Insert dummy cycles if needed to give Scan enable (*SE*) time to flip. Operate in functional mode and apply three functional clock cycles using $Clk_1$, and three functional clock cycles using $Clk_2$.

c) *Step 3*: Switch to scan mode and shift out the results. If the signature of the results matches the expected signature included in the fault dictionary for this test pattern, delete all the faults that are diagnosable by this test pattern from the list of suspect locations. This step can be overlapped with Step 1 to apply another test- pattern to the circuit.

As discussed above, all the test patterns included in the CDC fault dictionary are applied to the CUT, one after another. While applying each test pattern, if the results matches the expected results, the faults listed as diagnosable by that test pattern are excluded from the list of suspect faults. Note that in this section, we discussed the case where the sender and receiver domains operate at the same clock frequencies. Other cases can be treated using a similar procedure. In principle, using the proposed fault diagnosis method, all S-CDC faults are distinguishable from each other and the exact location of each S-CDC fault can be determined. However, due to the limitation of commercial ATPG tool that we employ in this paper, only a subset of the test patterns detecting each CDC fault (up to 255 patterns) is generated for that fault (Section VI-A). Due to this limitation, for a number of CDC faults, their exact location cannot be determined and instead, a list of suspect locations is reported. As an example, assume that set $TV_i$ and set $TV_j$ includes the set of test patterns generated by a commercial ATPG tool to detect CDC faults $f_i$ and $f_j$, respectively. The sets $TV_i$ and $TV_j$ do not include all the patterns detecting faults $f_i$ and $f_j$, i.e., each of $TV_i$ and $TV_j$ sets includes up to 255 test patterns. Although both these faults can be detected by test pattern $t_k$, due to the limitation of the commercial ATPG tool, $t_k$ may only be included in $TV_i$ (not in $TV_j$). Hence, even though CDC faults $f_i$ and $f_j$ are considered as distinguishable by applying vector $t_k$, they cannot be distinguished from each other on the basis of $t_k$.

**B. Error Recovery:**

To recover from errors that result from process variations, the use of post-silicon tunable-buffers has been proposed in the literature [23], [24]. These buffers can compensate for the effect of process variations. We consider such an approach to recover from CDC errors.

**1) Proposed CDC Error Recovery Method***:* As discussed in Section III, process variations may result in an incorrect transfer of data between different clock domains of a multiclock circuit. Equipping multiclock chips with clock- tuning circuits can enhance the reliability of these circuits and compensate the effect of process variations [25], [26]. As discussed in Section IV, if the setup time of a flip-flop is violated, its faulty behavior can be modeled as a transition fault. Accordingly, to recover from the erroneous behavior of a flip-flop when its setup time is violated, its clock signal can be delayed.

To recover a multiclock circuit from a S-CDC error, the receiver flip-flop of the faulty CDC pair should operate under a delayed clock signal. Therefore, external delay blocks can be inserted in the clock path of such a flip-flop depending on the slack-time between it and the flip-flops fed by it. Fig. 4(a) shows an example multiclock circuit in which the flip-flop residing in the receiver clock boundary operates under a delayed-clock signal. In this circuit, by inserting a buffer in the clock path of the receiver flip-flop (depending on the propagation delay of $BUF_1$ and the amount of setup-time violation of that flip-flop), S-CDC errors in the clock boundary can be avoided.

In general, to equip a multiclock circuit with a CDC error recovery mechanism, the circuit shown in Fig. 4(b) can be employed. If by applying the fault diagnosis scheme proposed in Section VI-A, the pair of flip-flops shown in Fig. 7(b) is reported as being faulty, *A* is set to value 1, and accordingly, $Clk_2$ signal propagates through gate $BUF_1$. Otherwise, *A* gets the value 0. As shown in this figure, to retain the timing relationship between $Clk_1$ and $Clk_2$, another tri-state buffer is inserted in the $Clk_1$ path. The circuit shown in Fig. 4(b) includes one flip-flip in the receiver side of the clock boundary. To equip this circuit

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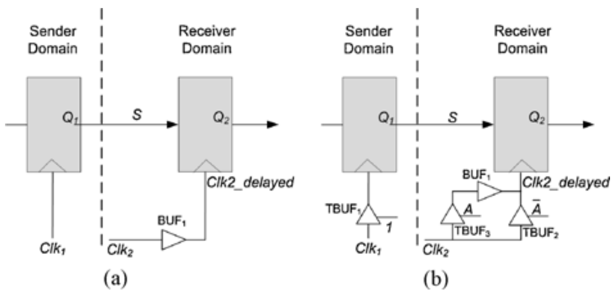


Fig. 4. Example of a CDC circuit (a) with delayed receiver-clock Signal and (b) equipped with an error recovery mechanism.

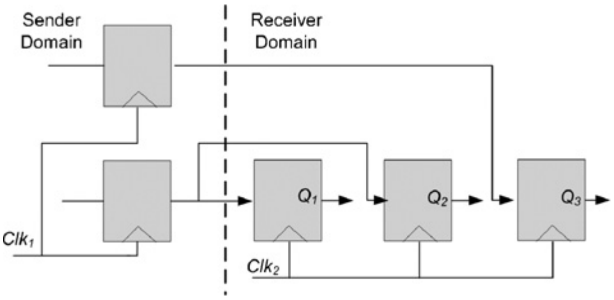


Fig. 5. Example of a CDC circuit with three flip-flops in the receiver clock- boundary.

with an error-recovery mechanism, one buffer, one inverter (to generate $\overline{A}$) and two tri-state buffers are inserted in the receiver domain. In addition, one tri-state is inserted in the clock path of the sender flip-flop. If the receiver domain includes $m$ flip- flops out of which $n$ flip-flops reside in the clock boundary, the error-recovery circuitry includes $n$ buffers, $2n$ tri-state buffers, and $n$ inverters. In addition, to reduce the number of input pins added to the original multiclock circuit, one shift register (including $\log_2(n+1)$ registers) and one decoder (with $\log_2(n+1)$ inputs) are also employed. One tri-state buffer is inserted in the sender domain and it feeds the clock input of all the flip-flops residing in this domain. Another tri-state buffer is located in the receiver domain feeding the clock input of all flip-flops other than those reside in the clock boundary.

Fig. 5 shows another example of a two-clock domain circuit that includes three flip-flops in the receiver side of the clock boundary and two flip-flops in the sender side of the clock boundary. In this figure, for the sake of clarity, only the flip- flops in the clock boundaries are illustrated and the other flip- flops have not been shown. Fig. 6 shows this circuit after insertion of the proposed error-recovery hardware.

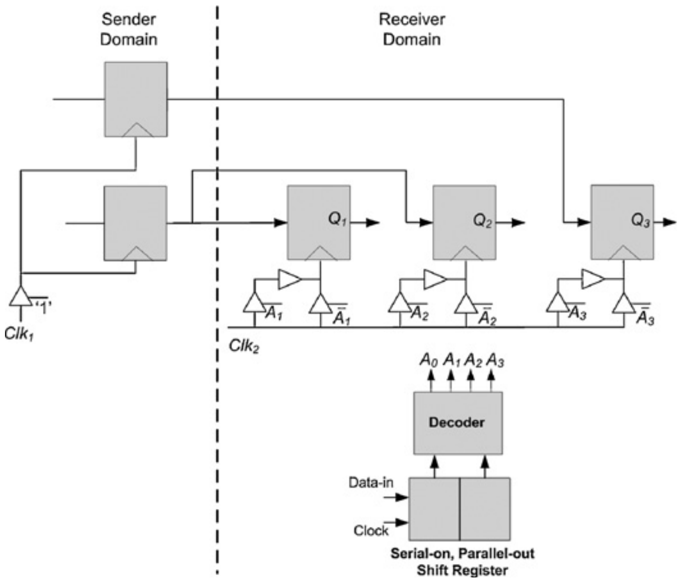


Fig.6 Error recoverable model of the circuit shown in figure 5 with one delay buffer in the clock path of the faulty flip-flop.

When error recovery is employed, the clock signal of the faulty flip-flop is delayed for $d$ ns, where $d$ is the propagation delay of one buffer gate. We can easily extend the proposed scheme and add more buffers in the clock path of a faulty flip-flop when insertion of only one buffer is not sufficient to recover from the CDC error occurred due to the setup time violation of that flip-flop.

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### VI. EXPERIMENTAL RESULTS AND ANALYSIS

In this section, the results of applying the proposed fault detection, diagnosis, and recovery methods to IWLS'05 bench- marks are presented and their significance are highlighted. The results are divided into four sets; the first set deals with the gate-level specification of each benchmark used in this study. The second set discusses the effectiveness of CoTC in detecting CDC faults. The third set evaluates the proposed fault diagnosis method. Finally, the fourth set evaluates the effectiveness of our error recovery scheme.

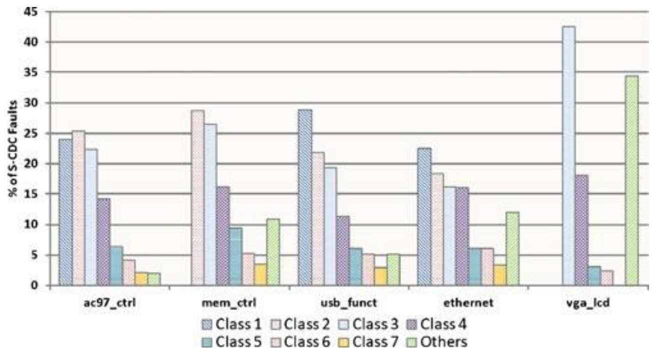


Fig. 7. Percentage of S-CDC faults classifying in each class of faults.

| Benchmark | S-CDC faults | # Testable S-CDC faults | # Detected by CoTC | #Detected by LoC/TDF | %Detected by CoTC |
|---|---|---|---|---|---|
| ac97–ctrl | 902 | 897 | 897 | 121 | 100 |
| mem–ctrl | 3,354 | 2,617 | 1,631 | 167 | 62 |
| usb–funct | 3,354 | 1,116 | 1,060 | 193 | 95 |
| ethernet | 4,862 | 643 | 529 | 391 | 82 |
| vga–lcd | 3,187 | 3,085 | 3,085 | 678 | 100 |

Table.1 Comparing CoTC and Traditional LoC Schemes in Terms of S-CDC Fault Detection

| Benchmark | # slow to rise faults | #detected by Loc/TDF | # Detected by CoTC + top- off ATPG | #Detected by LoC/TDF | # Detected by CoTC + top- off ATPG |
|---|---|---|---|---|---|
| ac97–ctrl | 40916 | 37154 | 37140 | 90.80 | 90.80 |
| mem–ctrl | 38086 | 17266 | 17482 | 45.33 | 45.33 |
| usb–funct | 40108 | 34718 | 34850 | 86.56 | 86.56 |
| ethernet | 160454 | 152098 | 152090 | 94.79 | 94.79 |
| vga–lcd | 382927 | 317092 | 317074 | 82.81 | 82.81 |

Table.2 Detected slow to rise faults

| Benchmark | Disgnostic Expectation |
|---|---|
| ac97–ctrl | 2.9 |
| mem–ctrl | 4.7 |
| usb–funct | 2.8 |
| ethernet | 4.0 |
| vga–lcd | 5.9 |

Table.3 Diagnostic expectation of CDC fault dictionary

| Benchmark | # of daley Buffers | Area of original circuit( in µm$^2$) | Area of circuit with error recovery (in µm$^2$) | % increase |
|---|---|---|---|---|
| ac97–ctrl | 7 | 35,002.4 | 10,885.7 | 31.1 |
| mem–ctrl | 50 | 23,258.7 | 6,419.4 | 27.6 |
| usb–funct | 16 | 32,151.7 | 3,311.6 | 10.3 |
| ethernet | 18 | 188,493.7 | 15,644.9 | 8.3 |
| vga–lcd | 38 | 307,111.6 | 1,842.6 | 0.6 |

Table.4 Area overhead incurred by proposed error recovery scheme

## VII. CONCLUSION

The robust design methods based on synchronizers and design verification techniques were used, process variations could introduce subtle timing problems that affect data transfer across clock-domain boundaries for fabricated chips, and also the high flow of current will lead to the chip burnout. Accordingly, modeling the incorrect behavior of multi clock circuits in the presence of CDC faults, detecting and locating such faults and recovery from CDC failures were necessary. In this project a scan flip-flop test generation method for detecting CDC faults. Fault diagnosis was performed by employing a CDC fault dictionary. While a CDC fault was located, its impact was masked using post-silicon by using tunable clock path circuits. This CDC fault detection, diagnosis, and recovery schemes to the asynchronous circuits with multiple clock domains. The results highlighted the effectiveness of the proposed methods in the recovery of multi clock circuits from CDC failures. This project mainly focuses on S-CDC faults and leaves the treatment of hold-time violations for future work.

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