



ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 7, July 2016

Prototype Development for Automation of Semiconductor Layer Growth Using Epitaxy

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ABSTRACT: In this paper, we describe automation of process using Programmable Automation Controllers (PAC). We have developed Graphical user interface on PC platform using LabVIEW. Code which is running on PAC is also developed on LabVIEW. LabVIEW is mostly used in development of GUI for data acquisition, instrument control and industrial automation since it provides inbuilt support for various devices and also has a rich library for GUI. We have used National Instruments make cRIO Programmable Automation Controller. cRIO has processor with real time operating system running, a FPGA module, reconfigurable input/output modules and an Ethernet expansion chassis. This work presents the extensive use of parallel nature of FPGA (FPGA hardware) using LabVIEW FPGA module to develop a real time system. LabVIEW is used to develop user interface for recipe, this recipe once finalised will be downloaded to PAC which will control and monitor the operation of reaction chamber of Semiconductor Layer Growth.

KEYWORDS: LabVIEW, LabVIEW FPGA module, programmable automation controller, real time system, compact reconfigurable input output system (cRIO).

I.INTRODUCTION

Epitaxy is the method of high quality crystal growth for numerous semiconductor materials. Epitaxy is referred as an arrangement of atoms in a crystal form upon a crystal substrate, so that the resulting added layer structure is an exact enlargement of the substrate crystal structure. This process of formation of epitaxy is carried out in reaction chamber of the system. In a reaction chamber substrate on which epitaxy is to be formed is first heated, a gas is allowed to pass over this heated substrate. When gas passes over the substrate, a semiconductor layer growth or formation of epitaxy layer through decomposition or by chemical reaction takes place[1].

This process involves careful heating of substrate and control of gas flow in a reaction chamber. The flow of gas is controller using operation of Mass Flow Controllers (MFCs) and solenoid valves. Solenoid valves act as a ON/OFF switch for gas flow where as flow rate of a gas can be precisely controlled with help of MFCs. The formation of multilayers on a substrate involves use of number of gases, with control over its flow duration & flow rate. It also involves sequencing of gases as well. To automate formation of multi-layer epitaxy we have developed user interface in form of recipe. This recipe preparation interface is developed on LabVIEW platform. This recipe will be downloaded to cRIO. On this cRIO another software reads steps specified in recipe and then it controls hardware of the system (Solenoid Valves, MFCs, etc). The software running on cRIO platform is developed on LabVIEW platform as well.

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II. ADVANTAGES OF USING PAC

Programmable Automation Controller (PAC) is a multiprocessor based device like a personal computer (PC) which is PC merged with a PLC using multitasking abilities to automate control of one or more piece of equipment. Although the PAC has PLC capabilities, its hardware architecture and software are software are designed to be more user friendly to IT/computer coder.[2]

Advantages of PAC over PLC are:

1. More open architecture
2. Modular design
3. More analog I/O options
4. Better process control capability
5. More built in communication port

Compact RIO is highly advanced PAC with more than 150 third party I/O modules, 24 controller and various communication protocol options. The NI cRIO-9068 consists of a dual-core processor, a reconfigurable FPGA, and eight slots for C Series I/O modules within single chassis. It has a 667 MHz dual-core ARM Cortex-A9 processor running NI Linux Real-Time OS and an Artix-7 FPGA[3]. FPGA is reprogrammable silicon chips. Hardware structure in the FPGA is not fixed so it is defined by the user. Although logic cells are fixed in FPGA, functions they perform and the interconnections between them are determined by the user and can be reprogrammed thousands of time. Many programmes can run simultaneously on it [4].

III. PROPOSED SETUP for AUTOMATION

In prototype development we have implemented recipe software which controls 8 solenoid valves and 8 MFCs. Proposed test set up consists of 8 LED's which will emulate valve ON/OFF as LED ON/OFF. The valve feedback signal is emulated using ON/OFF switches. For implementing MFC control command analog output port is used. Same analog voltage output is fed back to analog input port of cRIO and this voltage is indicated as flow of gas through MFC.

In order to control working of valves and MFCs the following set up done which is shown in Fig 1. The cRIO system is connected to computer through Ethernet. 8 channel Analog and digital input/output modules are connected to the cRIO chassis to control valves and MFCs. LabVIEW and FPGA modules are used for the development of software. The developed software is implemented on FPGA to generate signals through analog and digital I/O modules.

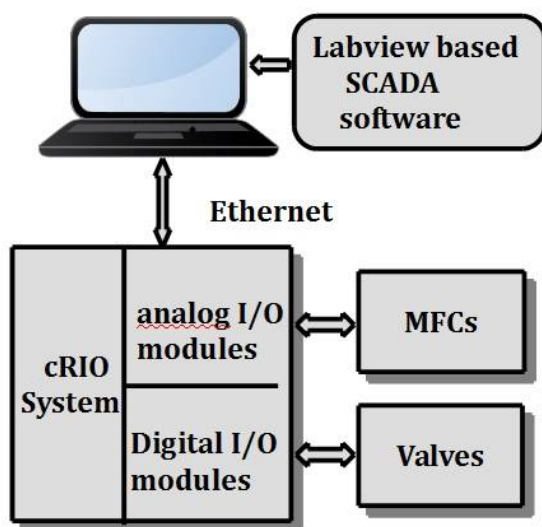


Fig.1: a. Block diagram of the Setup, b. Actual setup of block diagram



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IV. IMPLEMENTATION OF RECIPE SOFTWARE ON cRIO

The recipe software developed provide a graphical user interface which help the user to write the process in steps. These steps are than execute sequentially. It also help user user to monitor the state of recipe. This recipe software is divided in to two mode:.

- Edit mode:** In edit mode for data entry a table is provided in which user can write a recipe. A recipe involves the steps of process for sequential operation of valves and MFCs. These steps include the time period and input for the valves which is 0 or 1 and input voltage for MFCs between 0 to 10 Volts as per the flow requirement. User can enter the input in respective columns. An example of the recipe is shown in fig2 where the steps are written by the user. Various options such as save recipe, open recipe, new recipe and copy last step have provided.
- New Recipe:** This option facilitates the user to clear the table to write new recipe.
 - Save Recipe:** This option facilitates the user to save the written recipe for the future use.
 - Open Recipe:** This option facilitates the user to open the existing recipe which was saved earlier by the user.
 - Copy Last Step:** This option facilitates the userto copy the last step of the recipe in case user wants to repeat the steps.

Prototype Recipe Software For fabrication of Semiconductor wafer

Edit Mode **Execution Mode**

INPUT

	TIME(sec)	V1	V2	V3	V4	V5	V6	V7	V8	M1	M2	M3	M4	M5	M6	M7	M8
STEP1	9	1		1		1		1	1	2.2		3.3		4		7	8
STEP2	11		1		1		1		1		7		4		10		10
STEP3	2	1	1	1		1	1	1	1	4	8		5.5	3.3			9.6
STEP4	3				1	1	1	1	1	5			5		7		8
STEP5	5	1	1		1	1		1	1	2			3	3.5		8.8	9.9
STEP6	6		1	1		1	1	1	1	3.3		6.6		7.7		4.4	
STEP7	7	1	1		1		1	1	1	5.6	6.6		9.9		7.7		5.5
STEP8	8	1	1	1	1		1	1		5.5		6.6		8.3		3.3	
STEP9	9	1		1		1				3.3		8.9	7.7		5.5		8.8
STEP10	5	1	1	1	1	1				5.5	2.3		5.6		7.7		9.8

Buttons: Copy Last Step, New Recipe, Open Recipe, Save Recipe

Fig.2 An example showing recipe written in Edit Mode

Execution mode: In execution mode, **play button** is provided to execute each step of the recipe, the current state of the process execution is shown such as the **current step** shows the steps which is currently executing, **Time** shows the time for which valves and MFCs shall work. Led indicators are used to show which valve is working and numeric indicator shows the input voltage given to the MFCs. **Stop** button is provided to stop the process.

Prototype Recipe Software For fabrication of Semiconductor wafer

Edit Mode **Execution Mode**

Play Stop Time (ms) Current step

2000 3

V1 V2 V3 V4 V5 V6 V7 V8

M1 M5
4.00 3.30
M2 M6
8.00 0.00
M3 M7
0.00 9.60
M4 M8
5.50 0.00

Fig.3. an example showing the execution of recipe in Execution Mode

Using LabVIEW FPGA module the recipe is implemented on FPGA. To operate the valves and MFCs signals are



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generated by the cRIO. For this communication between HOST PC and cRIO is established via Ethernet. All data from HOST PC is sent to the real time processor in the cRIO using shared variable[5]. Shared variable for communication gives user an advantage that once the recipe is sent to real time processor, the cRIO can work stand alone even if PC crashes. To establish communication between host to cRIO programming is done on three level ie. first is on computer (**HOST VI**), second is on RT target (**RT target VI**) and third is on FPGA (**FPGA VI**) which shown in fig 4 [6].

- **HOST VI:** It is a recipe software which will provide user interface. In this VI user will add steps of the recipe which is send to the real time target in the form of arrays using shared variable.
- **RT Target VI:** In this VI the data coming from the host VI is read. This data is than passed to the FPGA in CRIO using read write control functions in a synchronised way with the help of single timed loop.
- **FPGA VI:** In this VI the data is read from read/write control functions on RT Target VI by the controls (boolean and Numeric) on the front panel of FPGA VI. This data is than fed into the digital and analog modules using input/output FPGA node. The FPGA I/O node used is configured for each channel of digital and analog modules.

When the data is read on FPGA VI the signals are generated and can be finally seen on execution mode as well as on the LEDs which are connected to the 8 channel digital input/output module. Out voltage from the 8 channel analog output module is fed back into the 8 channel analog input module and can be seen on execution mode.

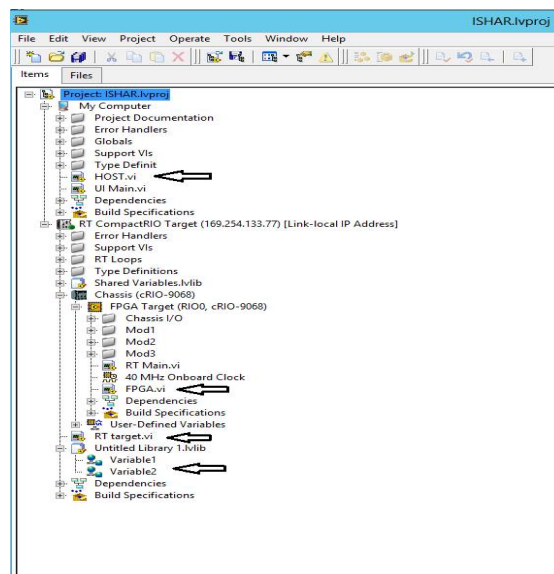


Fig.4: Project Explore window depicting Host VI, FPGA VI, RT target VI, Variable 1 and Variable 2

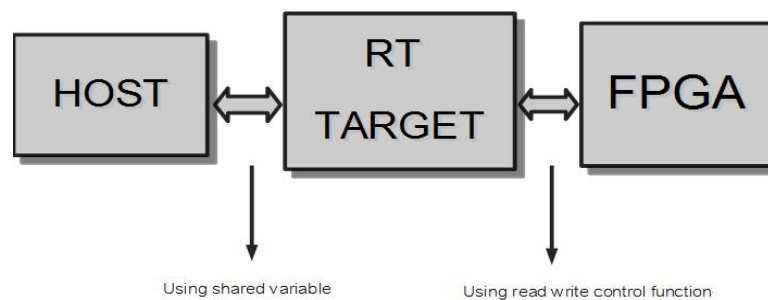


Fig.5. shows the flow of data



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V.RESULT

Recipe software developed using LabVIEW provides user a graphical user interface which provides user an easy way for recipe entry. Edit Mode in software provides user an easy way to write the steps in table for the sequential functioning of valves and MFCs. Execution mode shows the details of state of process such as current step in execution, valves and MFCs functioning in the current step and the time for which a particular valve or MFCs is working. By automation operational accuracy, efficiency, consistency of process is improved. It totally eliminates the delays and error caused by the human beings. Moreover it frees the personnel from tedious work of monitoring and controlling many valves and MFCs. This recipe software can customised for any process which requires sequential operation of valves and MFCs.

REFERENCES

1. **SCADA Software for Gallium Nitride Metal Organic Vapour Phase Epitaxy System** Shradha Tiwari, VirajBhanage, P.P. Deshpande, Tapas Ganguli, C.P. Navathe, S.M.Oak Raja Ramanna Centre for Advanced Technology, Indore
2. www.controleng.com
3. www.ni.com
4. Clive Maxfield, "FPGA:Instant Access".
5. LabVIEW FPGA Course Manual
6. www.ni.com/pdf/manuals/372596b.pdf