



A Survey on Instrumentation Amplifiers used for Biomedical Application

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ABSTRACT: This paper discusses the various types of BioInstrumentation amplifier designs for the amplification of bio signals fabricated using the CMOS technologies. The Bioamplifiers play an important role in biomedical implant devices like hearing aids, pacemaker etc. Those amplifiers are surveyed based on different techniques used for circuit design and fabrication methodologies. The different techniques such as level shifting, cascading, cascading and multistage amplifiers have been used to reduce the power consumption and also to achieve high gain and CMRR, which are discussed in this work. The comparison for existing bio amplifiers in terms of CMRR, voltage gain, noise level and bandwidth are carried out in this paper.

KEYWORDS: Amplifier, Bio signals, CMRR, voltage gain, low power.

I. INTRODUCTION

Bio-signals such as EEG, ECG, pulse rate, heartbeat rate are weak signals which have to be amplified for measurement and testing purposes in the bio-medical field. This amplification process is accomplished using bio-amplifiers such as operational amplifiers basically instrumentation amplifiers. Instrumentation amplifiers serve as an important signal conditioning block at the front end for the amplification of bio signals [1]. The instrumentation amplifier can be defined as a precision closed loop gain block that has a pair of differential input terminals and a single ended output that works with respect to a common or a reference terminal. An in-amp needs to be able to amplify microvolt-level signals and at the same time rejecting volts of common mode (CM) signal at its inputs. In-amps have very high common mode rejection ratio (CMRR) making it useful for amplification. The CMRR ranges between 70 to 100dB and can be varied according to the usage of the amplifier.

Bio potential signals like EEG, ECG, and heartbeat rate of human are weak signals (few mV to 100 μ V) and have to be amplified. Operational amplifiers can also be used but instrumentation amplifiers are widely used to meet the required performances. According to AAMI, CMRR has to be greater than 90dB and the voltage gain higher than 80dB, thus IA is widely used for the amplification of these signals [2]. IA possesses unique properties like Low dc offset, high CMRR, High gain and compact size, also providing accuracy and stability required for the amplification process.

Instrumentation amplifier with high common mode rejection ratio (CMRR), low input referred noise voltage and low dc offset as well as very low power consumption are required. Designing of such circuits of low power consumption with reduced noise has been a difficult task from a long time. These amplifiers are fabricated using the CMOS technology [3]. The CMOS methodologies such as TSMC, BSIM3V3, SIMC processes have been used for the fabrication of the IC using 90nm, 160nm, 0.35 μ m, 0.18 μ m fabrications which vary depending on size and area requirement of the chip. Thus the main purpose of using various fabrication technologies is to reduce the power consumption, the number of transistors used (to reduce the chip area), the thickness of the IC chip, to increase the gain without altering the basic characteristics of the IA.

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In this paper Different techniques have been presented for low power bio amplifiers. The structure of the rest of this paper is organized as follows: prior work of different bio amplifiers is presented in Section II, different amplifier performance and results are shown in Section III and the conclusion is presented in Section IV.

II. DIFFERENT BIO-INSTRUMENTATION AMPLIFIERS

Martinet *al* says that current feedback amplifier [4]. 16 instrumentation amplifiers have been used to build the acquisition system with an overall CMRR of 100dB. Such a high CMRR along with low power and low noise is possible due to the usage of current feedback amplifier [5]. The instrumentation amplifier circuit using the current feedback amplifier is shown.

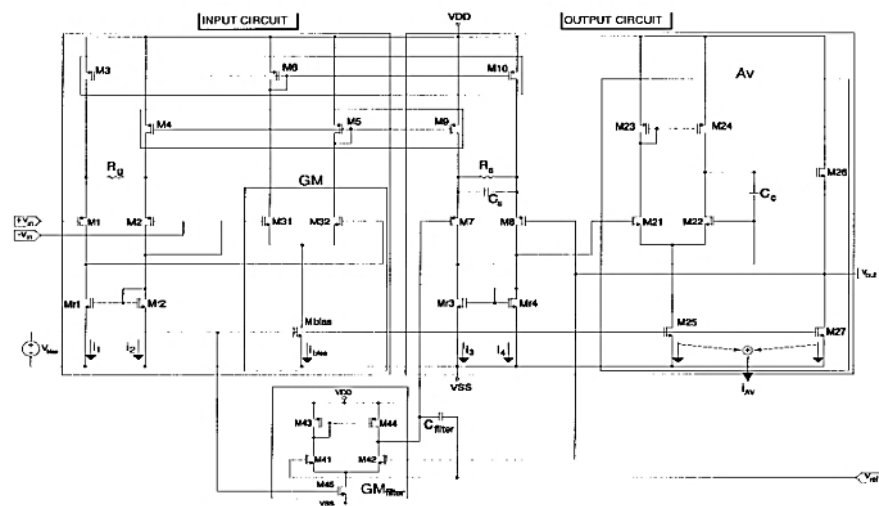


Figure 1: Schematic of amplifier using CFA[4].

In Figure1, the input circuit acts as a trans conductance amplifier and the output circuit acts as a trans resistance amplifier. Mirroring of the current of the input branch with that of the output branch the IA relation is achieved. Band pass filter has been incorporated in this circuit in order to reduce the input referred noise to a minimum. This circuit has been implemented in the standard CMOS technology with a power consumption of 500 μ W. Through stimulation a CMRR equal to 100dB and the total input referred noise were kept below 1.5 μ V to increase the performance of the amplifier. This amplifier aims at reducing the noise and at the same time increasing the CMRR to obtain a better gain.

In neural recording application the signals generated will be of weak signals and hence it should be amplified by rejecting large dc offset generating at the electrode tissue interface with low noise and low power. Harrison *et al* has designed such an amplifier circuit, implemented with 1.5 μ m CMOS technology[6].

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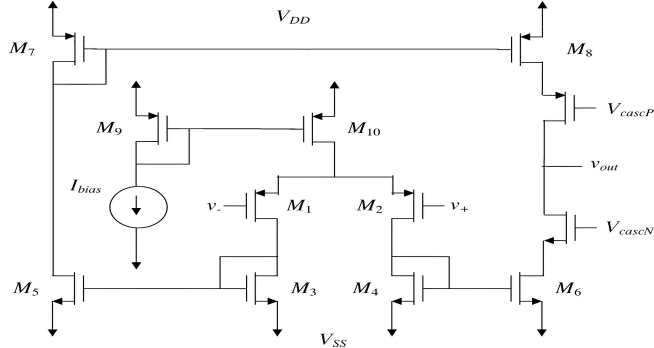


Figure 2: Schematic of the OTA used in neural amplifier[6].

In this circuit (Figure 2) OTA (operational trans conductance amplifier) is depicted, which is used in the amplifier, is designed with the capability of driving the capacitive load transistor. Sizing of the transistor is done to achieve low noise with low power consumption. In this amplifier, two MOS bipolar devices are connected in series to reduce the distortion. Through stimulation, this amplifier has achieved a high gain of 40dB and CMRR of 88dB with the power supply of $\pm 2.5V$.

Baghinet *al* designed low power bio amplifier using current balancing technique [4][7], implemented with multi project test chip $0.35\mu m$ mixed mode CMOS process through MOSIS.

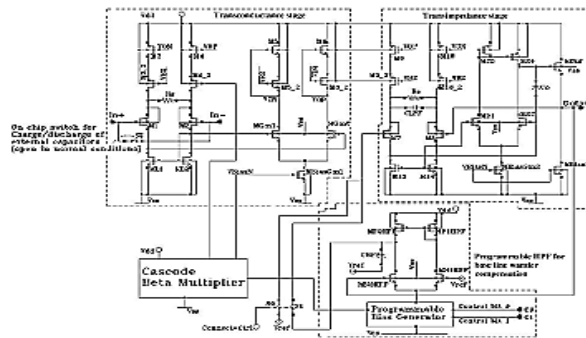


Figure 3: Schematic of the low power amplifier[3].

In the above circuit (Figure 3) 2 stages are implemented. First stage is implemented using the trans conductance MGm1 and MGm2. Here the transistors ML1 and ML2 acts as low to input transistors M1 and M2. MGm1 and MGm2 has feedback path for the input through cascade current mirror technique. This Cascade current mirror is used to achieve high CMRR [7]. When applying differential voltage trans conductance amplifier is unbalanced at the trans impedance stage the transistors M7 and M8 is linearized with operational amplifier by converting current to voltage across the resistors thus the output voltage obtained will be amplified. A CMRR of 100dB is obtained with $9\mu A$ power supply[3]. In this the low power designing and sizing of the circuit is discussed.

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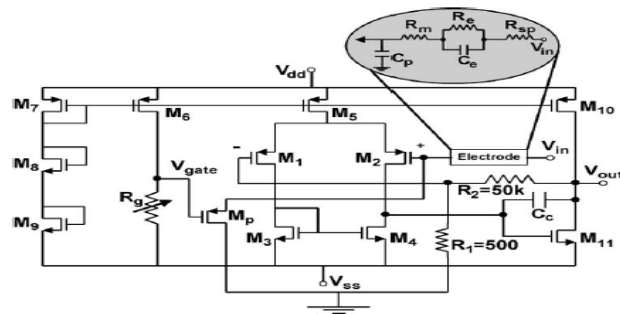


Figure 4: Bandpass operational amplifier[4].

Mohseni *et al* presented a bandpass operational amplifier for neural recording with low noise and low power consumption[8]. A gain of 39.3 dB at 1Hz is achieved with two stages of CMOS amplifier in a closed loop resistive feedback circuit[9][10]. The circuit is implemented with AMI 1.5 μ m double-poly double-metal n-well CMOS process.

In this Figure 4, the circuit is provided with PMOS subthreshold input to reduce the large and random DC offsets that exists at the electrode – electrolyte interface with the frequency of 9.1 kHz .In this circuit, DC response is controlled with the channel resistance $M_p(r_{ds})$. V_{gate} is the controlling parameter for M_p operation. With these in-vitro measurements in saline electrode and micro- machined probe, functionality of the amplifier withlow power dissipation of 115 μ W is designed to achieve low noise and high gain of 39 Db.

Chow *et al*[11] proposed circuit with high CMRR and PSRR implemented using the UMC 0.18 μ m CMOS technology

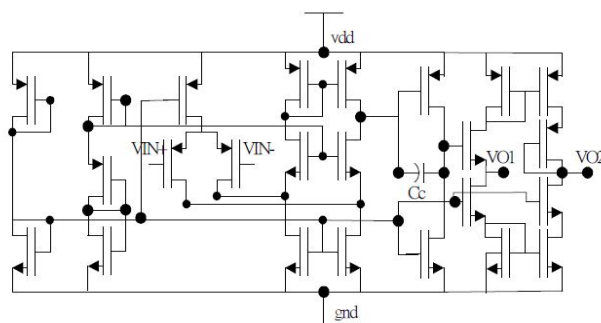


Figure 5: Amplifier with High CMRR[11].

for biomedical applications.

In the above Figure 5, the proposed instrumentation amplifier is implemented with three operational amplifier current mirror transistors and few resistors [12]. V_+ and V_- are the input signals by sensing the biomedical voltage from human skin. In this circuit four stages of operation is performed, first stage for biasing, second stage for increasing the open loop gain and adjusting the common mode voltage [13], using folded cascade configuration, third stage is used to achieve high gain and final stage for output voltages. Through these stages of amplification the author has achieved a CMRR of 166.69dB with 1.8V power supply and low dc offset input voltage.

Baghini *et al*[14] designed a chip fabricated with 0.35 μ m mixed mode CMOS TSMC process to present a three channel low power analog processor for ECG monitoring devices. By using the current balancing technique [7][15][3], analog signal conditioning functions are implemented in the Instrumentational amplifier. With the low power supply of 3V, it achieves CMRR of 100 Db with the gain of 600V.

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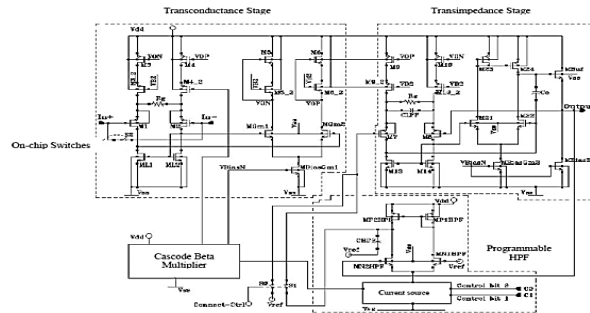


Figure 6: Low power analog chip for ECG recording[14].

In Figure 6, current balancing technique is implemented. By using cascade current mirror technique in this circuit, resistance achieved will be high hence power consumed will be low, thus increasing the CMRR. R_g and R_s are used to reduce external components. This technique of implementing integrated signal conditioning reduces complexity of the circuit.

The amplifier designed by Zhang *et al* [15] provides low dc offset at the skin electrode interface and also has low power consumption. The IC consists of a low offset op-amp along with a current reference circuit. This design is implemented in SMIC 0.18 μ m IP6M CMOS technology.

Figure 7 shows the architecture of the CMOS amplifier which includes the current reference, bias generator and the

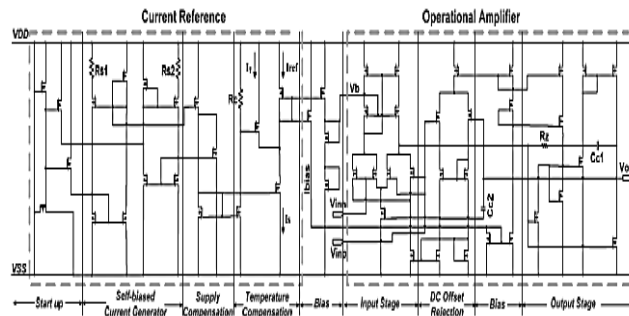


Figure 7 : Schematic of the integrated CMOS amplifier[15].

low offset amplifier[17][18]. Proper biasing of the circuit is achieved using the bias generator. The depicted amplifier consists of the DC offset rejection ratio, the input stage and the output stage. Continuous-time asymmetrical differential input structure with DC offset rejection circuit [16] has been used to minimize the input offset. This amplifier provides an open loop voltage gain of 60dB with a CMRR > 85dB. Power dissipation of 37.8 μ W with input offset voltage of 80 μ V(max) has been obtained with a 1.8V supply.

To achieve low power, Tseng *et al* [19] designed a bio-potential front end amplifier with voltage supply of 0.4 – 0.8v and 0.23-1.86 μ A current and was fabricated using the TSMC 0.18 μ m CMOS technology.

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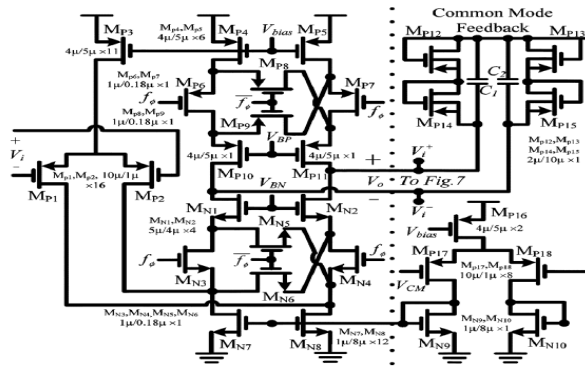


Figure 8: Schematic of folded cascade amplifier[19].

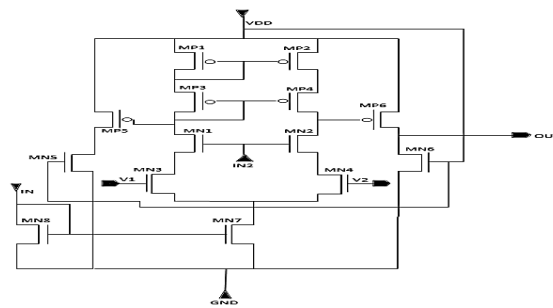


Figure 9: Schematic of the folded cascode amplifier[22].

In Figure 8, the conventional Instrumentation amplifier is designed with the op-amp consisting of folded cascade amplifier with choppers to reduce noise and CMFB(Common Mode Feedback) [20]. To reduce the flicker noise and to increase the range of the input common mode voltage, PMOS transistors (Mp1-Mp3) are used. With the transistors (Mp6-Mp9) PMOS and (Mn3-Mn6) NMOS, the residual offset is eliminated, hence low power is acquired [21]. With the low power supply of $0.09\mu\text{W}$, CMRR of 125 dB is achieved and with high gain of 40.70dB, this circuit is suitable for bio-signal recording.

Goel *et al's* [22] amplifier contains 2 amplifiers at the input and a Folded Cascode amplifier at the output. Gain is increased by the usage of the folded cascode amplifier [23]. It has been implemented in the **0.18μm CMOS technology**, providing a gain of 67dB and a CMRR of 92dB. It exhibits power consumption of $263\mu\text{W}$, which is lower when compared to other amplifiers also being an ideal condition for bio-medical application.

Figure 9 depicts the 2 stage Folded cascode CMOS op-amp. A cascode is a cascade of the common source (CS) and the common gate (CG) amplifier whose main advantage is increased gain. As shown in fig 9, the transistors Mn3 and Mn4 acts as the differential pair which senses the voltage difference at the input, operating in the saturation region instead of the triode region. The op-amps at the input operates in the buffer configuration and the folded cascode amplifier operates in the differential configuration. Active impedances have been employed to reduce the power consumption.

A CMOS amplifier with differential input and output was designed by Hsia *et al* [2]. The circuit is implemented in the $0.35\mu\text{m}$ CMOS technology. 3 stage of amplification has been employed to increase the gain and the CMRR. The first stage provides a high CMRR, second and the third stage have been used to increase the voltage gain. Both the common and the differential modes have been employed to increase the overall performance of the amplifier.

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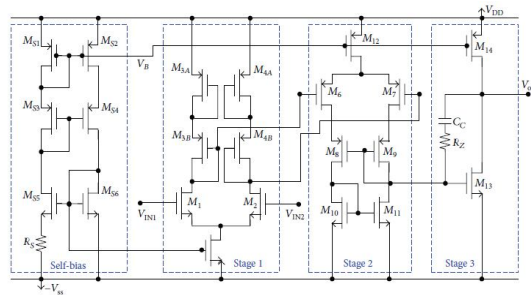


Figure 10: Schematic of the 3 stage amplifier[2].

As shown in Figure 10, transistors M1 to M5 consists of the first stage, M6 to M12 comprises the second stage. These stages act either as OTA [24,25] or as a folded cascode amplifier [26]. The third stage consists of M13 and M14, which acts as a common source amplifier for driving the load. It provides a gain of 80dB and a high CMRR of 130dB. Power dissipation <1mW has been obtained at 3.3V input supply.

III. ANALYSIS OF DIFFERENT BIOINSTRUMENTATION AMPLIFIER

Various bio-amplifier that have been discussed in Section II and the comparison has been provided in Table 1.

Table No. 1: Comparison of the different bio-amplifiers

S.no	Author	Year	Technol-ogy used	Supply voltage	Gain	Band width	CMRR	Noise	Power Dissipation
1.	Martins et al	1998	Standard CMOS	±4.5V	Variable gain		99dB	1.4µV	500µW
2.	Harrison et al	2003	1.5µm CMOS	±2.5V	40dB	7.2kHz	≥88dB	2.2µVrms	80 µW
3.	Baghini et al	2004	0.35µm CMOS	±5mV	55.6dB	200Hz	100dB	0.3µV/Hz	9µW
4.	Mohseni et al	2004	AMI 1.5µm CMOS.	3v	39.3dB	9.1kHz	>29dB	7.8µVrms	115µW
5.	Chow et al	2007	UMC 0.18µm CMOS	1.8V	50dB	972Hz	167.18dB	6.29µV/H _z	3.196 mW
6.	Lal et al	2008	0.35µm CMOS TSMC	3V	56dB	200Hz	100dB	10µV RMS	66µW
7.	Zhang et al	2009	SMIC 0.18µm CMOS	1.8V	60dB	2.82MHz	≥85dB		37.8µW
8.	Tseng et al	2012	0.18µm CMOS TSMC	0.4V – 0.8V	40.70dB	Variable	125dB		0.09mW
9.	Goel et al	2013	0.18µm CMOS	5mV	92dB	1.1MHz	67.7dB	1.75pV/H _z	263mw
10.	Hsiao et al	2013	0.35µm CMOS	3.3V	80dB	10KHz	130dB		1 mW



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Thus from Table 1 it can be said that the bio-amplifier designed based on the cascading technique has provided high CMRR of 125dB, the cascading technique has produced a high gain of 92dB and tri-stage amplifier gives a high performance along with reduced noise and is independent on process variations. Thus by combining these methodologies a bio-amplifier with high gain, high CMRR and reduced noise along with low power consumption can be designed and analysed based on these amplifiers.

IV. CONCLUSION

This paper presents the various bio amplifiers implemented using different CMOS technologies. The comparison of all the amplifiers is done depending on the technology, technique used and also the basic parameters of the instrumentation amplifier. Various methods have been employed to increase the performance of the amplifiers for biomedical applications. Thus, further research would lead to a high performance amplifier implemented in CMOS technology with increased gain and CMRR along with low power consumption.

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