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FPGA Implementation of Novel High Speed Vedic Multiplier

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ABSTRACT: Now a day's almost all DSP and Communication applications require high speed processors. The speed of a processor is mainly given in terms of performance of ALU and in turn in terms of MAC unit. MAC (multiplier and accumulator unit) is the main arithmetic processing unit of ALU. The demand for high speed processing necessitates high speed multiplier architecture. In this paper, a novel high speed 8-bit Vedic Multiplier is proposed using the Ancient Indian Vedic Mathematics technique. It uses four 4X4 multipliers designed using Urdhwa Tiryagbhyam sutra for partial product generation. This stage is optimized in terms of delay and power by using novel high speed 4:2 compressor architecture. The partial product addition stage is accomplished by using three modified Ripple Carry Adders. Final result is just the Concatenation of specific output bits of Ripple Carry Adders. The coding of the proposed multiplier is done in VHDL and simulated using Xilinx ISE 14.7. The design is synthesized using Xilinx-XST. The design is implemented on FPGA (field programmable gate array) kit, Spartan-6 (XC6SLX45) series. The results presented in this paper are compared with 8-bit conventional multiplier architectures. The efficiency of proposed architecture is given in terms of reduced area, low critical path delay and low hardware complexity. Results shown in this paper proves that the proposed 8-bit multiplier is 1.11 times faster than the normal 8-bit Vedic multiplier.

KEYWORDS: 4:2 compressors, Ripple Carry Adder, Urdhwa Tiryagbhyam sutra, Vedic multiplier, VHDL.

I.INTRODUCTION

In all signal processing applications, the operations like filtering, convolution, DCT, DFT, DWT and FFT/IFFT etc are accomplished by repetitive multiplication and addition operation. As the speed of multiplication and addition determines the execution speed and overall performance of ALU, the high speed multiplier is therefore necessary. An efficient multiplier is the one which satisfies all three performance determining criteria: speed, power and area.
This leads to several multiplier architectures like Array, Booth [1], Modified Booth, Wallace Tree multiplier [2], Baugh-Woolley multiplier etc. from last few decades. But these algorithms involve several time consuming intermediate operations for calculations of partial products before reaching the final answer. This in turn reduces the speed of multiplier exponentially. To overcome drawbacks of these algorithms, the multiplier based on Vedic mathematics is discussed in this paper. A comparison table given in[3] is as below:

Parameter	Array Multiplier	Wallace Tree Multiplier	Booth Multiplier	Vedic Multiplier (Urdhwa Tiryagbhyam Multiplier)
Operating Speed	Less	High	Higher	Highest (it has less devices)
Delay	More	Less	Less	Very Less
Power Consumption	Consume more power	Consume more power	Consume less power	Consume less power
Area	Greater Area (many adders used)	Medium Area (computation stages reduced)	Minimum Area	Minimum Area (Least number of adders)
Structure	Regular	Irregular	Irregular	Regular
Complexity	Less Complex	More Complex	More Complex	Less Complex (less logic devices)
Logic Levels	More	Less than Array structure	Increases	Reduced to great extent
Types of operand	Unsigned and signed	Unsigned and signed	Unsigned and signed	Unsigned and signed
FPGA Implementation	Efficiency Less	Not Efficient	Most Efficient	Most Efficient

Table1: Performance comparison of different multipliers with Vedic Multiplier

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Shri Bharati Krishna Tirthaji (1884-1960), a popular mathematician in India rediscovered Vedic mathematics from the ancient Indian scriptures between 1911 and 1918 [4]. He bi-furcated the whole mathematics into 16 simple sutras (formulae) and 16 sub-sutras which are the backbones of Vedic mathematics. The greatest advantage of Vedic maths is that it reduces the complex calculations in conventional mathematics into simple ones thereby optimizing processing time, area and delay. Out of many methods of Vedic multiplication, the Urdhwa Tiryagbhyam method is preferred as it can be applied to all cases of arithmetic. In this method, the partial products required for multiplication are obtained in parallel and well in advance thus saving very important processing time.

Section II in this paper discusses the Urdhwa Tiryagbhyam sutra in detail with its 4X4 bit multiplier implementation. Section III describes a novel approach of using ultra low power 4:2 compressor adder. It gives minimum critical path delay [4] and replaces the half adders and full adders in existing Vedic multipliers. Section IV discusses design of proposed 8-bit Vedic multiplier using four 4X4 Urdhwa multipliers and modified Ripple Carry Adder. Section V gives the results of simulation performed in Xilinx ISE 14.7 and comparison table.
Section VI is the Conclusion.

II. VEDIC MATHS- URDHWA TIRYAGBHYAM SUTRA

The term Urdhwa Tiryagbhyam is derived from two Sanskrit words “Urdwa” and “Tiryakbhyam” which mean “Vertically” and “crosswise” respectively. This method is well explained in the line diagram as shown below. The line diagram for multiplying two 4 bit numbers say a3a2a1a0 (multiplicand) and b3b2b1b0 (multiplier) using Urdhwa Tiryakbyam method is shown in figure1.

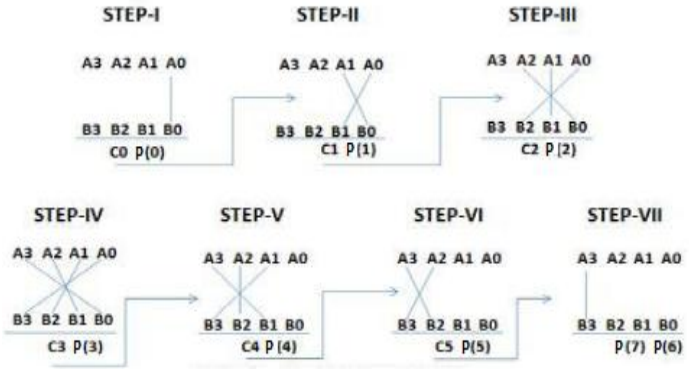

Figure1: Line diagram for 4X4 bit Urdhwa Tiryakbyam method of multiplication

The important steps in Urdhwa Tiryagbhyam sutra are:

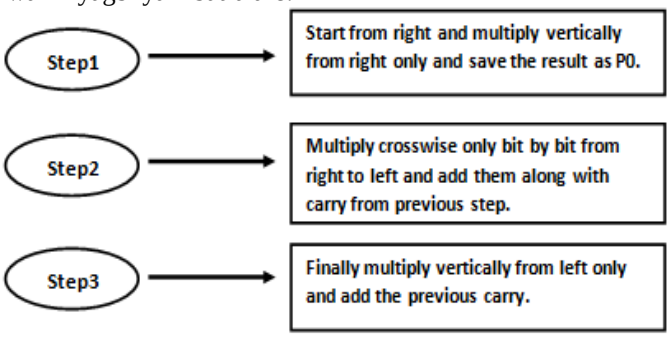

Figure2: Steps in Urdhwa Tiryagbhyam sutra

The equations (1) to (8) representing the line diagram are as below,

$P0 = a0b0$ **(1)**

$C1\ P1 = a1b0+a0b1$ **(2)**

$C2\ P2 = a2b0+a1b1+a0b2+C1$ **(3)**

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C3 P3 = a3b0+a2b1+a1b2+a0b3+C2 **(4)**
C4 P4 = a3b1+a2b2+a1b3+C3 **(5)**
C5 P5 = a3b2+a2b3+C4 **(6)**
C6 P6 = a3b3+C5 **(7)**
P7 = C6 **(8)**

P= P7P6P5P4P3P2P1P0 being the final product.

These equations are implemented using number of Half adders and Full adders in conventional Vedic multiplier. But, from equations (1) to (8), it is clear that few equations require more than 3 bits to be added at the same time to generate partial products, which is not possible by full adder. This idea invents a new kind of hardware architecture which can add more than 3 bits at a time also with increased efficiency in terms of speed.

III. COMPRESSOR ADDER

A compressor adder is a logical circuit which improves computational speed of addition of 4 or more bits at a time. Compressor is an effective replacement for the combination of several half adders and full adders. Thus it reduces the critical path delay during partial product addition stage thereby reducing the power consumption.
The compressor used in this paper is a 4:2 compressor adder as shown in figure3 below.

Figure3: Black box of 4:2 Compressor Adder

It adds four inputs (X1, X2, X3, and X4) along with carry (Cin) and produces two outputs Sum (S) and Carry (C) along with Cout. **It is called compressor as it compresses the four partial products into two.** If numbers of 4:2 compressors are connected in cascade, Cout is the output to the next stage compressor and connected to Cin of neighboring 4-2 compressor. Thus without propagating the carry to the higher bit, the 4:2 Compressor can add four partial products because the Cout is independent of the Cin. This makes it a **carry-free adder** stage.

Out of many architectures of 4-2 compressor given in [5] and [7], the XOR-XNOR based architecture shows significant improvement in delay and is therefore used in this paper as given below in figure 4.

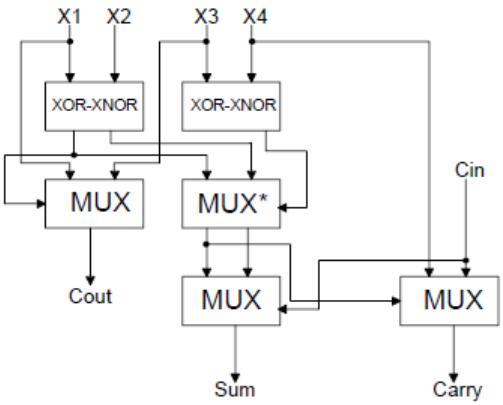

Figure4: Proposed 4:2 Compressor- 3Δ

The critical path delay of this proposed implementation is Δ-XOR + 2*Δ-MUX = 3Δ

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The set of equations for the Cout, Sum and Carry are;

$$Cout = (X1 \oplus X2)\,X3 + \overline{(X1 \oplus X2)}\,X1 \quad \textbf{(9)}$$

$$Sum = [(X1 \oplus X2)\,\overline{(X3 \oplus X4)} \oplus \overline{(X1 \oplus X2)}\,(X3 \oplus X4)]\,\overline{Cin} + \overline{[(X1 \oplus X2)\,\overline{(X3 \oplus X4)} \oplus \overline{(X1 \oplus X2)}\,(X3 \oplus X4)]}\,Cin \quad \textbf{(10)}$$

$$Carry = (X1 \oplus X2 \oplus X3 \oplus X4)\,Cin + \overline{(X1 \oplus X2 \oplus X3 \oplus X4)}\,X4 \quad \textbf{(11)}$$

The overall equation for 4:2 Compressor is, X1+X2+X3+X4+Cin=Sum+2*(Carry +Cout) **(12)**

Thus the novel approach of combining 4-2 compressor adders in 4X4 Urdhwa Tiryagbyam Vedic multiplier [6] gives the following implementation as shown in figure6 with a simple flowchart in figure5.

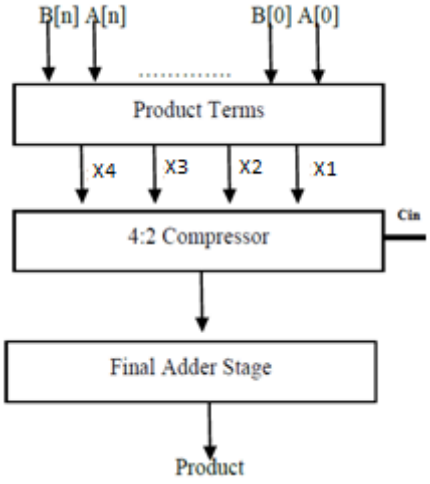

Figure5: Flowchart for Urdhwa Tiryagbhyam Vedic Multiplier with 4:2 Compressor

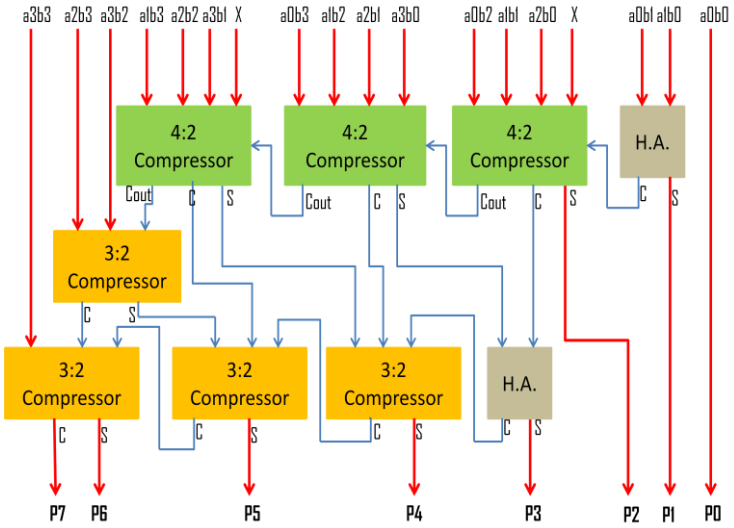

Figure6: Compressor based 4X4 bit Urdhwa Tiryagbhyam Vedic multiplier

The 3-2 compressor is just the replacement for full adder.

IV. PROPOSED MULTIPLIER

The block diagram of proposed 8X8 multiplier architecture is as shown in figure7 below.

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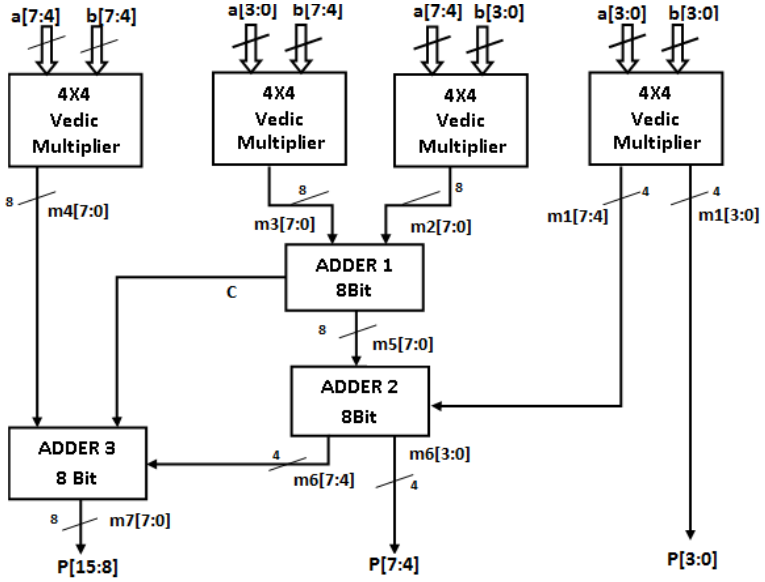

Figure7: Proposed 8-bit Vedic multiplier

The 8-bit multiplier proposed in this paper is implemented into following three stages:

1. **Partial Product Generation:** using **four 4x4 Compressor based Urdhwa Tiryagbhyam Vedic multipliers.** Initially, the 8-bit multiplier and multiplicand is divided into four blocks of 4-bit each: a [3:0], a [7:4], b [3:0], b [7:4]. These are given as input to 4-bit Compressor based Vedic multiplier proposed in previous section. The partial products obtained from four 4X4 multipliers are again divided into four regions as m1, m2, m3, m4 as shown in figure8.

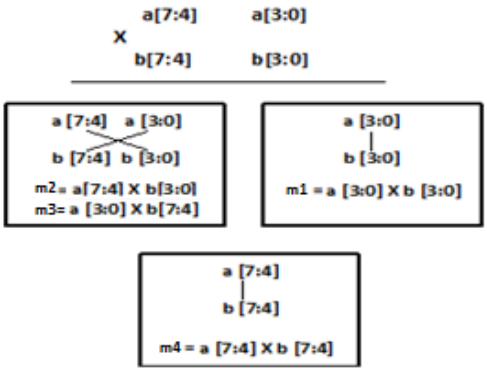

Figure8: Separation of Partial Products

2. **Partial Product Addition:** The 4 blocks of partial products generated i.e. m1, m2, m3, m4 are added using overlapping logic by using 3 modified Ripple Carry adders (ADDER1, ADDER2, and ADDER3).

3. **Final Result Generation:** The final result is just concatenation of P [15:8] and P [7:4] and P [3:0].

V. SIMULATION RESULTS

The proposed 8-bit multiplier is coded using VHDL, simulated using Xilinx14.7 ISim simulator and synthesized using Xilinx XST for Spartan 6: **XC6SLX45-** FPGA. This FPGA has speed grade of -5 and package is **CSG324C**. Inputs are

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generated using VHDL test bench and outputs are verified. The simulation results for following set of inputs are as shown in the Figure 9.

CASE - 1: inputs_1 = "11011011",
input_2 = "10101010"
Result = "1001000101101110"

CASE - 2: inputs_1 = "11111111",
input_2 = "11111111"
Result = "1111111000000001"

CASE - 3: inputs_1 = "00110101",
input_2 = "00010101"
Result = "0000010001011001"

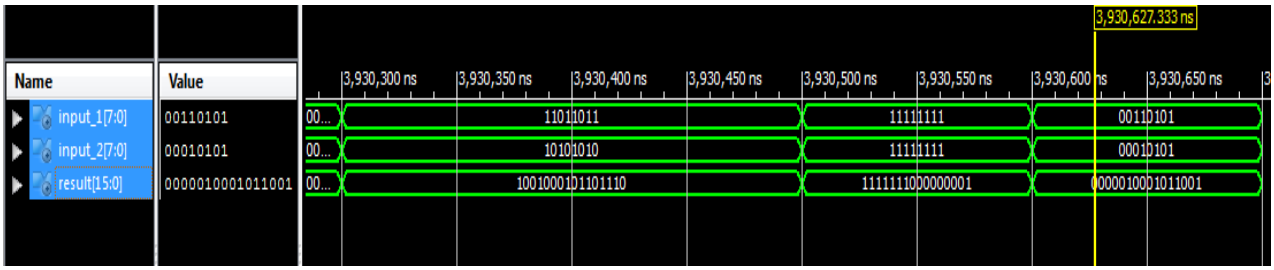

Figure 9: Simulation result for Case-1, 2, 3

Figure10 below gives the RTL schematic of proposed 8 bit multiplier with reference to the design in figure7.

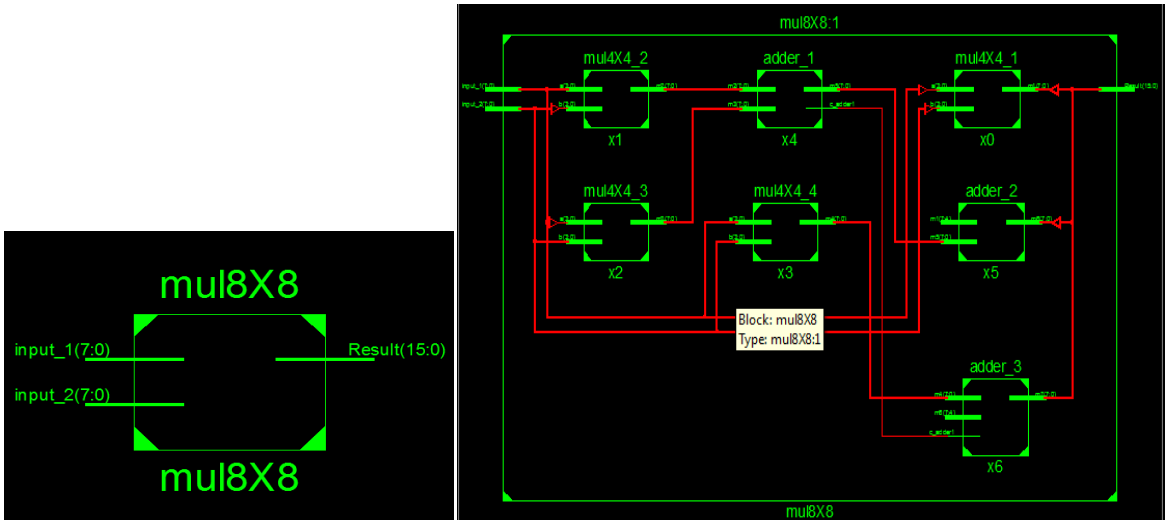

Figure10: RTL schematic of proposed 8X8 Vedic Multiplier

Comparison with Various Architectures:
Comparison of the proposed 8-bit multiplier with Normal 8-bit Vedic and other conventional architectures is given in Table-2. Comparison is done in terms of total delay, logic delay, route delay and number of logic levels.

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Multiplier Type	Proposed 8-bit multiplier	Normal 8-bit Vedic multiplier	8-bit array multiplier using CSA	8-bit Wallace tree Multiplier
Total Delay(ns)	15.700	17.430	17.533	15.969
Logic Delay (ns)	5.822	6.030	6.026	5.823
Route Delay (ns)	9.878	11.400	11.507	10.146
Logic Levels	12	13	13	12

Table-2: Comparison of proposed multiplier architecture with other popular architectures

Total delay is the sum of Logic and Routing Delay. From Table-2, it is clear that the proposed design performs well than conventional multiplier architectures.

V. CONCLUSION

In this paper, we have proposed the novel high speed 8 bit multiplier. The design of 8-bit multiplier is implemented using four 4-bit multipliers and modified ripple carry adders. The 4-bit multipliers combine the Urdhwa TIryagbhyam method of Vedic multiplication with novel 4:2 compressor adder. The novel XOR-XNOR based architecture of 4:2 compressors is better in terms of delay and power. Thus combing the advantages of Compressor adders with ancient Vedic mathematics methodology serves our purpose of increasing speed of calculations while being area efficient. The proposed multiplier architecture can be used for high speed complex number multiplication.

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