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Implementation of BAUGH-WOOLEY Algorithm and Compressors in signed Multipliers

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ABSTRACT: The BAUGH-WOOLEY algorithm is a different scheme for signed multiplication, but is not so widely adopted because it may be complicated to deploy on irregular reduction trees.
The implementation of different types of compressors are employed in multiplier design to optimize the power, area, and timing, which are compared.

KEYWORDS:BAUGH-WOOLEY, Compressor, Multiplier, Critical path, Power, Delay, Area.

I.INTRODUCTION

As multipliers plays a major role in computation. It is necessary to design an efficient multipliers that is it should be fast enough and consumes less power and occupies less area.
Normally in the multipliers partial product is summed with the help of full adders and half adders. It produces a results which takes large delay, power and area as the size of multiplier increases. And also there are many algorithms for unsigned numbers multiplication to do fast computation. But, very few in signed multiplication.
BAUGH-WOOLEY algorithm is used for signed multiplication. As well as compressors are used to reduce the delay, power and delay for large bit multipliers. So, efficient signed bit multipliers are designed using BAUGH-WOOLEY algorithm with compressors is observed from the results. Which makes computations so fast in our computers along with power efficient.

II.IMPLEMENTATION OF BAUGHWOOLEY ALGORITHM IN MULTIPLIER

Baugh-Wooley algorithm is simplified multiplication for signed numbers. Whenever the most significant bit of multiplicand is multiplied with the multiplier each partial product generated then these partial products are shifted and as per their bit orders and added.In similar way, when MSB of multiplier is to be multiplied with bits of multiplicand take not of multiplicand bit, then AND(logically) with MSB of multiplier.Add one full adder in n+1 column with inputs as MSB of both multiplier and multiplicand, and a high at 2n+1 column for an n nit multiplier.

III.IMPLEMENATION OF COMPRESSORS

There are two types of implementations of compressors either cascading two three to two compressors or design four to two compressor with reduced number of levels. The second type gives better results shown in table2, which is implemented in 8x8 and 12x12 multipliers. Whereas the cascading method is nothing but will give result of replacing all full adders in normal multiplier with a three to two compressor. So, type1gives more timing delay and is shown in table1, which is implemented in 4x4 multiplier.
A three to two compressor is similar to the full adder. And a four to two compressor is similar to two full adders in a column. Whereas a five to two compressor is similar to three full adders in a column of normal unsigned multiplier. The timing (delay) decreases in type2 compared to type1 because the critical path is decreased.

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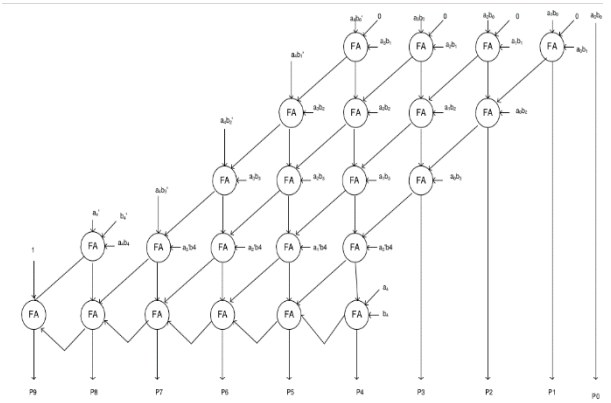

Fig1.4x4 baughwooley multiplier without compressors

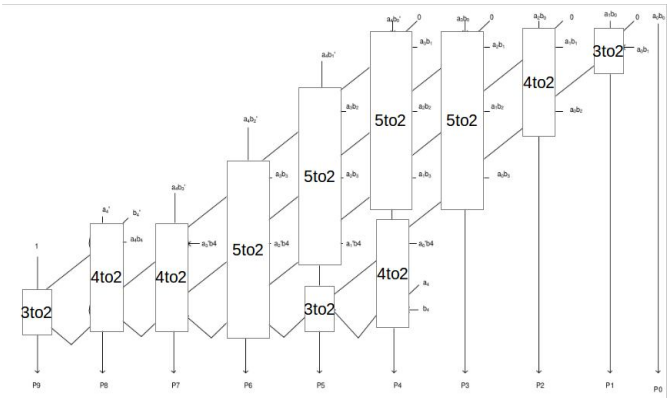

Fig2. 4X4 baughwooley multiplier with compressors

A)IMPLEMENATION OF THREE TO TWO COMPRESSOR

A three to two compressor circuit is shown below which serves the purpose of full adder, but reduces the powerconsumption not the timingbecause of same critical path in both full adder and three to two compressor.

B) IMPLEMENATION OF FOUR TO TWO COMPRESSOR

A four to two compressor circuit is shown below which serves the purpose of two full adder, but reduces the power consumption because of using multiplexers and timing because of less critical path in four to two compressor.

C) IMPLEMENATION OF FIVE TO TWO COMPRESSOR

A five to two compressor circuit is shown below which serves the purpose of three full adder, it reduces the power consumption because of using multiplexers and timing because of less critical path in five to two compressor.

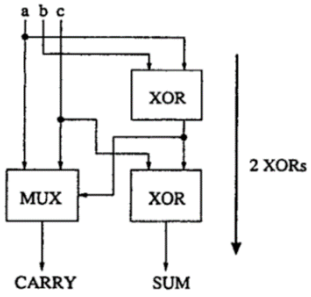

Fig 3 three to two compressor

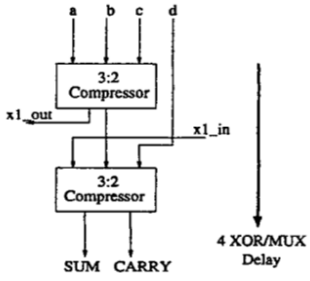

Fig 4. Type 1 four to two compressor

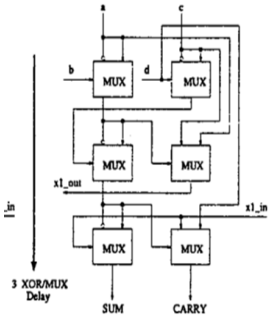

Fig 5. Type 2 four to compressor

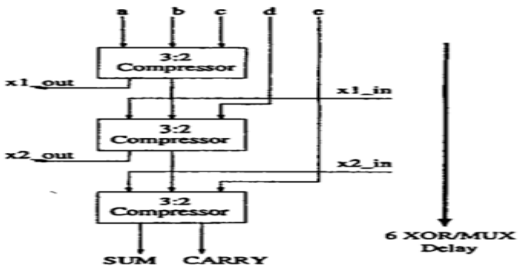

Fig 6. Type 1 five to two compressor

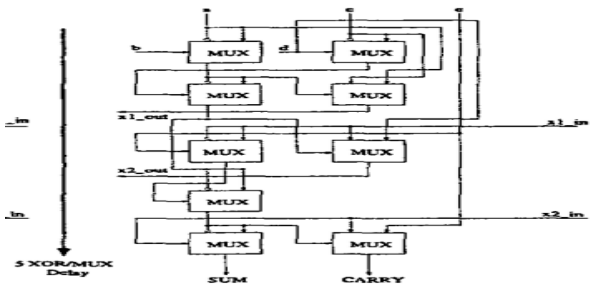

Fig 7. Type 2 five to two compressor

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IV.DESIGNING MULTIPLIER

It is observed that number of combinations of bits of multiplier and multiplicand is equal to r. if r<=n; 2n-r if r>n.
Number of carry inputs from previous column is equal to the number of combinations of bits of multiplier and multiplicand +1if r<2n; 2 if r=2n+1.
Number of full adders=r-1ifr<=n;r=n if r=n;r=2n-r if n+1<r<2n-1; r=2 if r=2n, 2n-1.
According to number of full adders we have to choose the combinations of compressors such that the number of levels is less.

V.RESULT

When Verilog code signed multipliers with and without compressors is simulated in cadence software the results of the area, power and timing came are shown in table1,2,3.

4x4 multiplier	4x4 multiplier without compressors	4x4 multiplier with compressors Type 1	4x4 multiplier with compressors Type 2
Area(um2)	582.10	597.643	522.85
Power(nW)	31744.872	25105.437	24428.483
Timing(pS)	2945	3760	2651

Table1.showing the details of area, power and timing of 4x4 multiplier.

Here the timing is increased in 4x4 multiplier with compressor because we implemented type1 compressors, which has critical path greater than that of type2. Whereas the power decreases because we implemented compressors using multiplexers. But the area is increased because of the type1 implementation of compressors.

8x8 multiplier	8x8 multiplier without compressors	8x8 with compressors Type 2	8x8 with compressors Type 1
Area(um2)	2013.782	1754.827	1998.259
Power(nW)	141272.180	124576.834	131723.203
Timing(pS)	5235	5002	7190

Table1.showing the details of area, power and timing of 4x4 multiplier.

Here the timing is decreased in 8x8 multiplier with compressor because we implemented type2 compressors, which has critical path greater than that of type2. Whereas the power decreases because we implemented compressors using multiplexers. But the area is decreased because of the type2 implementation of compressors.

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12x12 multiplier	12x12 with compressors type2	12x12 with compressors type1
Area(um2)	3731.213	4267.469
Power(nW)	331100.414	368527.187
Timing(pS)	10402	13740

Here we have implemented the 12x12 with compressors of type2 and the results are observed.

VI.CONCLUSION

Different compressors are used to speed up the multiplication process. 4-2 compressors and 5-2 compressors are used in multipliers successfully. Performances of Multipliers are compared with and without compressors.

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