An Improved Active-Clamped DC-DC Converter with Modified PI Controller

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ABSTRACT: A new dual active-clamping dc-dc converter is proposed to obtain high efficiency. The proposed converter employs a dual active-clamping technique, while a resonant voltage doubler rectifier scheme controls the output voltage with the pulse width modulation technique. The dual active-clamping circuit serves to recycle the energy stored in the leakage inductor or the magnetizing inductor and provides zero-current turn-off switching. The voltage stresses of the main switches are clamped. The voltage transient spikes across the dual active-clamping circuit and the current stress of the current-fed side switches are limited by auxiliary dual active-clamping circuits on both sides, and zero-current switching is achieved. Also, to reduce the output voltage variation, a modified PI controller is suggested.

KEYWORDS: Converter, active-clamping, voltage doubler rectifier, high-efficiency, zero current switching (ZCS).

I. INTRODUCTION

The global demand for electrical energy has continuously increased over the last few decades. Environment and energy have become serious concerns in today’s world. Alternative sources of energy generation have drawn more and more attention in recent years. Photovoltaic (PV) sources are predicted to become the biggest contributors to electricity generation among all renewable energy generation candidates by 2040[1]. The PV module needs a high step-up dc-dc converter to interface the low dc voltage to the high dc voltage before making it to ac for grid-tie applications. A step-up dc-dc converter is needed with a high step-up ratio and high-efficiency. Among the investigated topologies, the active-clamped step-up dc-dc converters are gaining its popularity. The intention of this paper is to propose a high-efficiency dc-dc converter for the photovoltaic module integrated (PV-MIC) system[3] where a high step-up dc-dc converter and low power inverter are attached at the back of each panel.

For a power level around 250-W in the PV-MIC system applications, several high step-up dc-dc converters were proposed for the power conversion form low dc voltage to high dc voltage. The half-bridge dc–dc converter has been presented to reduce switching power losses at high-voltage side[4]. The output diodes are turned OFF at zero current by using the voltage doubler rectifier. However, an additional half-wave rectifier is needed, which increases switching power losses. Alternatively, the active-clamped dc–dc converter has been used for low-voltage PV sources[5]. It uses the active-clamping circuit and the resonant voltage doubler rectifier. However, the active-clamping circuit increases the voltage stress of power switches at low-voltage side, causing high switching power losses. Additionally, thermal management problems should be considered for a practical design of the PV MIC system. Although, the soft-switched half-bridge dc–dc converters and active-clamped dc–dc converters were proposed but they do not have a high step-up voltage conversion ratio, thus requiring a high turns ratio. High turns ratio is not favoured due to high leakage inductance at the secondary side, which causes high switching losses at the output diodes.

In this paper, an improved active-clamped dc–dc converter[6] is presented by dual active-clamping circuit. The proposed converter uses the dual-active clamping circuit and the voltage-doubler rectifier[7] in order to achieve a high step-up ratio and soft switching operation. The output diodes in the proposed converter can be turned off at zero-current, which can reduce the switching power losses at high output voltage applications. The leakage inductance of the transformer and the resonant capacitor of the voltage doubler rectifier are utilized for the series-resonant circuit to achieve zero current switching of the output diodes. Furthermore, the output voltage stress can be clamped as output voltage, which reduces the voltage rating of the output diodes. To reduce the output voltage variation, a modified PI controller is presented to reduce zero current stress of the output diodes.

II. PROPOSED CONVERTER ARCHITECTURE

The proposed converter is shown in Figure 1. It consists of a modified PI controller, a high step-up dual active-clamping converter, a resonant voltage doubler rectifier, and an output filter. The modified PI controller is used to reduce the output voltage variation. The high step-up dual active-clamping converter is used to achieve high efficiency. The resonant voltage doubler rectifier is used to clamping the output voltage and reduce the voltage rating of the output diodes. The output filter is used to filter the output voltage and reduce the output voltage variation.
controller is suggested. The performance of the proposed converter evaluated on a 200-W PV-MIC system. A high-efficiency of 97.5% is achieved to generate 350V high output voltage from 50-V low PV module voltage.

II. CONVERTER OPERATION

Figure.1 shows the circuit diagram of proposed dc-dc converter. The step-up dc-dc converter consists of a boost type of a dual active-clamping circuit (S_2, S_3, C_e), a transformer T, and the resonant voltage doubler rectifier (L_{1K}, C_r, D_{o1}, D_{o2}). Also, the converter consists of main switches (S_1, S_4) and auxiliary switches (S_2, S_3) operate complementarily with a short dead time. All switches are the MOSFET’s. (D_{s1} - D_{s4}) Are the body diodes of switches (S_1 - S_4) and (C_{x1} - C_{x4}) are the output capacitors of switches (S_1 - S_4), respectively. The transformer T has the magnetizing inductor L_m and leakage inductor L_{1K} with the turn’s ratio of 1: N, where N = \frac{N_p}{N_m}. C_i is the input capacitor. C_e is the clamping capacitor. C_o is the output capacitor. The capacitors C_i, C_e and C_o are large enough so that their voltages V_i, V_c and V_o are considered constant, respectively. L_{1K} is assumed to be much smaller than L_m. The capacitor C_r is the resonant capacitor. C_r Resonates with the leakage inductor L_{1K}. Thus, the resonant capacitor voltage V_r is not considered constant for one switching period.

Figure.1 Circuit diagram of proposed dc-dc converter.

Figure.2 shows the switching waveforms of the proposed converter during one switching period T_s. Figure.2 (a) shows the switching waveforms at primary side. Figure.2 (b) shows the switching waveforms at secondary side.
The proposed converter has six switching modes during $T_s$:

**Mode 1 [$t_0, t_1$]:** At $t = t_0$, $S_1$ and $S_4$ are turned ON. Since $V_{Lm} = V_i$, the magnetizing inductor current $i_{Lm}$ increases linearly as

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{V_i}{L_m}(t - t_0) \quad (1)$$

At the secondary side, when $N V_i$ is applied to the secondary winding of $T$. The output diode $D_{o1}$ is turned ON. The series-resonant circuit consisting of $L_{ik}$ and $C_r$ is formed. Series resonance between $L_{ik}$ and $C_r$, the energy stored in $C_r$ is transferred to $C_o$, the angular resonant frequency $\omega_r$ is

$$\omega_r = \frac{2\pi f_r}{\sqrt{L_{ik}C_r}} \quad (2)$$

Where $f_r$ is the resonant frequency. By referring $i_{d_{o1}}$ to the primary side, the primary current $i_p$ is expressed as

$$i_p(t) = i_p(t_0) + \frac{V_i}{L_m}(t - t_0) - N i_{d_{o1}}(t) \quad (3)$$

The output diode current $i_{d_{o1}}$ is given by

$$i_{d_{o1}}(t) = \frac{V_o - N V_i - V_r}{Z_r} \sin \omega_r(t - t_0) \quad (4)$$

The resonant impedance $Z_r$ is expressed as

$$Z_r = \frac{L_{ik}}{\sqrt{C_r}} \quad (5)$$

**Mode 2 [$t_1, t_2$]:** At $t = t_1$, the half-resonant period of the series resonance is finished. The output diode current $i_{d_{o1}}$ is zero before $D_{o1}$ is turned OFF. ZCS of $D_{o1}$ is achieved without any reverse recovery current.

**Mode 3 [$t_2, t_3$]:** At $t = t_2$, $S_1$ and $S_4$ are turned OFF. The primary current $i_p$ charges $C_{s1}$ and $C_{s4}$ and discharges $C_{s2}$ and $C_{s3}$. $V_{s1}$ and $V_{s4}$ increases from zero to $V_i$. $V_{s2}$ and $V_{s3}$ decreases from $V_c$ to zero. Since the switch output capacitor $C_s$ is very small, the time interval is considered as negligible comparing to $T_s$.

**Mode 4 [$t_3, t_4$]:** At $t = t_3$, $S_2$ and $S_3$ are turned ON. Since $V_{Lm} = -V_c$, the magnetizing inductor current $i_{Lm}$ decreases linearly as

$$i_{Lm}(t) = i_{Lm}(t_3) - \frac{V_c}{L_m}(t - t_3) \quad (6)$$

When $N V_c$ is reversely applied across the secondary winding of $T$. The output diode $D_{o2}$ is turned ON. The series resonant circuit between $L_{ik}$ and $C_r$ is formed again. By referring the output diode current $i_{d_{o2}}$ to the primary side, $i_p$ is expressed as

$$i_p(t) = i_p(t_3) - \frac{V_c}{L_m}(t - t_3) - N i_{d_{o2}}(t) \quad (7)$$

Where the output diode current $i_{d_{o2}}$ is given by

$$i_{d_{o2}}(t) = i_{d_{o2}}(t_3) - \frac{N V_c + V_r}{Z_r} \sin \omega_r(t - t_3) \quad (8)$$

**Mode 5 [$t_4, t_5$]:** At $t = t_4$, the half-resonant period of the series resonance is finished. The $i_{d_{o2}}$ is zero before $D_{o2}$ is turned OFF without any reverse recovery current.

**Mode 6 [$t_5, t_6$]:** At $t = t_5$, $S_2$ and $S_3$ are turned OFF. The primary current $i_p$ charges $C_{s2}$ and $C_{s3}$ and discharges $C_{s1}$ and $C_{s4}$. $V_{s2}$ and $V_{s3}$ increase from zero to $V_c$. $V_{s1}$ and $V_{s4}$ decrease from $V_i$ to zero. Since the capacitor $C_s$ is very small, time interval is negligible as compared to $T_s$.

By the voltage-second balance relation on the magnetizing inductor $L_m$, the voltages $V_c$ and $V_r$ are expressed as

$$V_c = \frac{D}{1-D} V_i \quad (9)$$

$$V_r = (1-D)V_o \quad (10)$$

For the voltage-second balance relation on the secondary winding of $T$ during $T_s$, the following relation between the output voltage $V_o$ and the input voltage $V_i$ is obtained as
The maximum voltage stress of $S_1$ and $S_2$ is confined to the input voltage $V_i$. The voltage stress of $S_3$ and $S_4$ is confined to the clamping capacitor voltage $V_c$. Figure 3 shows the relation between the clamping capacitor voltage $V_c$ and the duty ratio $D$. The dual active-clamping is used in the proposed converter. The clamping capacitor voltage in case of the dual active-clamping circuit is always lower than the clamping capacitor voltage in case of the conventional active-clamping circuit. It means that the switch voltage stress of the proposed converter is always lower than the switch voltage stress of previous converter [5] using the conventional active-clamping circuit. Especially, when the duty ratio is below 0.5, the clamping capacitor voltage can be lower than the input voltage $V_i$. It is critically beneficial in low-voltage PV applications where more than 50% of power losses are lost as switching power losses.

III. CONTROL STRATEGY

A. A modified PI controller is to reduce output voltage variation:

The output voltage $V_o$ is controlled with duty ratio $D$. Then, the duty ratio $D$ is represented by

$$ D = D_n + D_c $$

(12)

Where $D_n$ is a nominal duty ratio and $D_c$ is a controlled duty ratio. The nominal duty ratio $D_n$ and the controlled duty ratio $D_c$ can be respectively, represented as

$$ D_n = 1 - \frac{NV_i}{V_o} $$

(13)

$$ D_n = \frac{N\mu\Delta I_m}{V_o T_s} $$

(14)

Then, the duty ratio $D$ becomes

$$ D = D_n + D_c = 1 - \frac{NV_i}{V_o} + \frac{N\mu\Delta I_m}{V_o T_s} $$

(15)

To regulate the output voltage for the output load variation, the conventional PI controller can be used for the controlled duty ratio $D_c$ as

$$ D_c = K_p e + K_i \int e \, dt $$

(16)

$$ e = V_o^* - V_o $$

(17)
Where $V_o^*$ is the reference output voltage, $e$ is the voltage error between $V_o^*$ and $V_o$, and $K_p$ and $K_i$ are the PI control gains of the controller, respectively. The regulated output voltage is an important factor achieving high performance. The PV MIC system should provide a fast dynamic response for grid power demand in case of the distributed generation using the renewable energy sources. Where the local load power increases or decreases abruptly, the output voltage of the dc-dc converter fluctuates as the inverter load changes. It might cause grid current harmonic distortion, damaging the grid-connected power generation systems. However, because the conventional PI controller controls the output slowly, the output voltage variation exists. To reduce the output voltage variation, a modified PI controller is suggested.

The suggested controller is

$$D_c = K_p e_m + K_i \int e_m \, dt$$

(18)

$$e_m = (V_o^* - V_o) \times (1 + \frac{|V_o^* - V_o|}{\alpha})$$

(19)

Where $e_m$ is the modified error between $V_o^*$ and $V_o$, $\alpha$ is the scaling factor. The error term $\frac{|V_o^* - V_o|}{\alpha}$ is included as comparing to the conventional PI controller. Figure 4 shows the difference between the error terms of the conventional PI controller, the error term of the suggested PI controller in case of $\alpha = 15$, and the error term of the suggested PI controller in case of $\alpha = 20$. The horizontal axis shows the difference between $V_o^*$ and $V_o$. The vertical axis shows $e_m$ and $e$. Due to the term $\frac{|V_o^* - V_o|}{\alpha}$, a large error between $V_o^*$ and $V_o$ increases $e_m$ more than $e$. Thus, if the voltage error is large, the output voltage can be rapidly controlled as the suggested controller has large gain. In contrast, if the voltage error is small, the suggested controller gives almost the same characteristic as the conventional PI controller.

B. Digital implementation:

Fig. 5 shows the control block diagram of the output voltage controller. The voltage error $e$ is calculated by comparing the reference output voltage $V_o^*$ to the measured output voltage $V_o$. The modified error $e_m$ is generated through the modified error calculation. Then, the PI controller is used to generate the duty ratio to control the power switches. The controlled duty ratio $D_c$ of the voltage controller only generates the output voltage drop required to regulate the output voltage. With the addition of the nominal duty ratio $D_n$ to the converter, the relation between $D_c$ and $\Delta I_{Lm}$ of the converter becomes a first-order linear dynamic system with easy controllability. Thus, the addition of the nominal duty ratio $D_n$ relaxes the burden of the voltage controller, improving the dynamic performance.

Figure 4. difference between the clamping capacitor $V_o$ and the duty ratio $D$: (a) in case of the conventional active-clamping circuit and (b) in case of dual active-clamping circuit. Figure 5. Control block diagram of the output voltage controller.
IV. EXPERIMENTAL RESULTS

Figure 6 shows the primary current $i_p$ and switch voltages $V_{s1}$ and $V_{s3}$ for 200-W output power at 50-V input voltage. As shown in figure 6, $V_{s1}$ and $V_{s3}$ are clamped at the input voltage respectively. Figure 7 shows the primary current $i_p$, clamping capacitor voltage $V_c$, and switch voltages $V_{s2}$ and $V_{s4}$ for 200-W output power at 50-V input voltage. The clamping capacitor voltage $V_c$ is 48 V. $V_{s2}$ and $V_{s4}$ are clamped at 48 V. Which is even lower than the input voltage $V_i$. The voltage stress of power switches is significantly reduced. Figure 8 shows the output diode voltages $V_{d01}$ and $V_{d02}$ and output diode currents $i_{d01}$ and $i_{d02}$ for output load.

Figure 6. Experimental results: primary current $i_p$: 10 A/division; switch voltage $V_{s1}$: 10 V/division Switch voltage $V_{s3}$: 10 V/division, 10 μs/division. Figure 7. Experimental results: primary current $i_p$: 10 A/division; clamping capacitor voltage $V_c$: 50 V/division; switch voltage $V_{s2}$: 10 V/division Switch voltage $V_{s4}$: 10 V/division, 10 μs/division.

Figure 8. Experimental results: Output diode voltage $V_{d01}$: 10 V/division; Output diode current $i_{d01}$: 1 A/division; Output diode voltage $i_{d02}$: 1 A/division, 10 μs/division at 50-V input voltage. Figure 9. Experimental results: measured efficiency of the proposed converter compared with the efficiency of the previous converter at 50-V input voltage. Figure 9 shows efficiency comparison at 50-V input voltage.
The proposed converter achieves the efficiency of 97.5% for 200-W output power. The previous active-clamped converter achieves the efficiency of 97.2% for 200-W output power. The efficiency of 0.3% is improved by the proposed converter at 50-V input voltage for 200-W output power. The previous half-bridge converter achieves the efficiency of 97.0% for 200-W output power. Figure 10 shows the output voltage $V_o$ and output load current $i_o$ in case of the conventional and modified PI controller.

Figure 10. Experimental results (output voltage $V_o$: 50V/division; output load current $i_o$: 0.1A/division): (a) in case of conventional PI controller, (b) in case of modified PI controller.

V. CONCLUSION

A dual active-clamping circuit with high efficiency has been proposed. Analysis, design, and simulation and experimental results for the proposed converter have also been presented. This proposed converter combines the dual active-clamping circuit and the resonant voltage doubler rectifier circuit across the power transformer with the topology proposed for soft switching dc-dc converter. The resonant voltage doubler rectifier circuit provides two resonant-current paths formed by the leakage inductance of the power transformer and the resonant capacitor. In addition, the ZCS mechanism of the switches by dual active-clamping and auxiliary switches, they reduce the switching losses and the reverse-recovery losses. The modified PI controller is suggested to reduce the output voltage variation. The proposed converter achieves a high-efficiency of 97.5% at 50-V input voltage for 200-W output power.

REFERENCES

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