



ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 7, July 2014

[DOI: 10.15662/ijareeie.2014.0307041](https://doi.org/10.15662/ijareeie.2014.0307041)

Adaptation of DSP Processors for 3G and 4G Wireless Communication

Vinni Sharma¹, Tanuja Kashyap²

Associate Professor, Dept. of E&TC, Bhilai Institute of Technology, Durg, Chhattisgarh, India^{1&2}

ABSTRACT: Technological advancements have resulted in significant changes in the processor architecture of mobile phones, transforming the typical mobile phones of 1990's to modern smart phones. The next generation of mobile computing requirements will increase due to higher data rates, increased complexity algorithms, and greater computation diversity but the power requirements will be just as stringent to ensure reasonable battery lifetimes. The design of the next generation of mobile platforms must address three critical challenges: efficiency, programmability, and adaptivity. This paper presents analysis of mobile signal processing applications and advanced signal processing architectures to deal with the rigorous requirements. This paper illustrates the role of Digital Signal Processors for Third generation (3G) mobile systems and DSP architectures for 4G wireless communication.

KEYWORDS: Processor architecture, RISC processors, VLIW, SoC, ARM processors

I. INTRODUCTION

The first-generation (1G) cellular wireless mobile systems were analog and were based on frequency-division-multiple access (FDMA) technology. The second boost for the cellular industry came from the introduction of the second-generation (2G) digital technology standards, including Global System for Mobile (GSM), IS-136 (Time Division Multiple Access, TDMA), and Personal Digital Cellular (PDC) [1]. In the transition from 1G to 2G in mobile communications, new standards are deployed which are digital in nature. So, due to the need to operate on larger data streams, more MAC (complex multiply and accumulate) and ACS (Accumulate compare and select) operations are required. It is here that DSP plays a role in wireless communication. Signal processing has always played a critical role in the research and development of wireless communication systems. As the demand for high capacity and high reliability systems increases, signal processing has an even more important role to play. Today's programmable DSPs are universal in the wireless handset market for digital cellular telephony.

DSPs cover a very wide range of architectural modifications for applications. DSPs can be divided into three general classes, i.e. Application Specific DSPs, Domain Specific DSPs, General Purpose DSPs.

AS-DSPs are typically customized to an application to serve high-end application performance requirements, or to minimize die size/cost. Generally the market volume must allow for a custom solution to be developed, and customizing is carried out to gain market advantages. However, time-to-market constraints must allow for a long design cycle. Examples of AS-DSP can be found e.g. for speech coding. Application customizing can be found in the data path, address generation, bus architecture, memory, and Input output.

DS-DSPs are designed to a wider application domains, as cellular modems. They can be applied to a variety of applications. Due to special instructions and additional hardware they can run domain specific algorithms efficiently e.g.



ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 7, July 2014

DOI: 10.15662/ijareeie.2014.0307041

Viterbi algorithm and equalizers. A DS-DSP is designed for a market with a volume high enough to allow specialized solutions. Its specific advantage over an AS-DSP is its fast availability.

GP-DSPs have evolved from the classic FFT/filtering multiply-accumulate design model. Examples are TIC50, Lucent 16xx, Motorola 563xx, ADI 21xxx and DSP-Semi's Oak/Pine. GP-DSPs are freely available, are extensively applicable, and have a large software base. They lack in performance as compared to more customized solutions for specific applications.

II. RELATED WORK

Qi Bi et. el.[1] concluded that at the start of the 21st century, the wireless mobile markets were witnessing unprecedented growth fueled by an information explosion and a technology revolution. In the radio frequency arena, the trend was to move from narrowband to wideband with a family of standards tailored to a variety of application needs. Byoung-Woon Kim et.el. [6] described a 16-bit programmable fixed-point digital signal processor called MDSP-II for mobile communication applications. The instruction set of MDSP-II was determined after a careful analysis of the Global System for Mobile communications (GSM) baseband functions. Alan Gatherer et. el.[7] proposed a parameterized DSP data path design and the parameterized DSP design flow . The proposed parameterized DSP was composed of DSP itself along with special blocks designed for communication systems.

Sorin Zoican et.el. [11] illustrated the role of Digital Signal Processors for third generation mobile systems. They discussed global objectives and attributes that include worldwide roaming, universal connectivity, high data transmission rates, location service capability, and support for high-quality multimedia services. B.G.Evans et.el.[12] discussed the limitations of 3G and drivers for 4G.Manoj Kumar Jain et.el [13] analyzed that the design and deployment of mobile processors over the years is affected by Communication, performance, low-power operation and the development in mobile processors is driven by factors such as low-power consumption, user interface performance, time to market, etc. R. Ramakrishna et. el [18] proposed a design of a variable point FFT processor using FPGA in which OFDMA Technology is applied. The FFT processor use Verilog HDL language to describe the circuit, use Quartus II 7.2 software to build the model, and use ModelSim SE 6.2b software to verify the timing function.

III. PROPOSED METHODOLOGY

The paper is organized in the following way. In the next section we categorize mobile processors according to domains of their applications. After that in section V we have discussed programmable digital signal processors for 3G mobile. In this, firstly we have discussed the requirements of Third Generation Mobile Systems and then DSP Architectures for 3G Mobile Communications Systems. Next, in section VI, we have covered most relevant technologies for 4G Mobile Processors. In this we have discussed the architectures of various DSP processors.

IV. WIRELESS APPLICATION SPECIFIC DSPS

Due to the growing importance of the wireless market there are now several DSPs that have been designed with wireless applications. Initially in the case of GSM and IS-136, DSPs have only been applied to specific areas such as speech codec because of their limited performance. To avoid the drawbacks, a number of application specific DSPs have been developed. For example, Lucent's DSP 1618 performs the Viterbi decoding using a coprocessor [2], which supports various decoding modes with control registers at the cost of chip area. Similarly TMS 320C54X supports specific instructions for the Viterbi decoding [3], which makes it useful for mobile communication. But it has only one multiplier, so it is difficult to handle the multiplication and accumulation of complex numbers, which is used in such applications as channel equalization. Several



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 7, July 2014

DOI: 10.15662/ijareeie.2014.0307041

DSPs that can support two MAC operations per cycles were developed, for example, very-long-instruction-word based TMS320C6X which don't have a dedicated MAC unit but has two multipliers and six arithmetic units. It performs MAC operations by using separate multiply and add instructions [4]. Also, the dual MAC unit in Lucent's DSP 1600 performs two multiplications and two accumulations in one cycle and support instructions for the Viterbi decoding [5].

One example of application specific DSP is the DSP with a special block called the Mobile Communication Accelerator (MCA) developed using the MetaCore framework. It is a design framework for generating application-specific instruction set processor for DSP applications, with the generator set for software tools such as compiler, assembler and instruction-set simulator. Example is MDSP-II, a 16-bit DSP [6]. The special functional block as well as an instruction set is improved toward the mobile communication applications. So, the remaining processing power becomes available for other features such as echo cancellation and speech recognition. The remaining processing power helps to reduce, the power consumption to make such DSPs more modest for portable applications, by performing the same functionality at the reduced clock rate. The GSM base-band functions, which need 53 million instructions per second (MIPS) on the general-purpose Digital Signal Processors, can be done with 19 MIPS.

In DSP evolution, VLIW processors are developed to support a compiler-based programmer-friendly environment [7]. Examples include TIs TMS320C6X [8], ADIs Tiger-SHARC [9], and Lucent and Motorola's Star Core [10]. These VLIW processors use apparently parallel instruction computing (EPIC) with prediction and assumption to help the compilers. The processors are statistically scheduled, multiple issue operations to exploit the instruction-level parallelism intrinsic in many DSP applications., these devices allow very efficient compilation of higher-level code, hence the need for DSP-specific assembly level coding of algorithms is reduced. The trend of wireless toward an open application-driven system will make this kind of DSP more convincing as a multimedia processor in the handset.

V. PROGRAMMABLE DIGITAL SIGNAL PROCESSORS FOR 3G MOBILE

A. Requirements of the Third Generation Mobile Systems

Most applications require audio, video and communications processing capabilities, the requirements placed on processors used in base station and mobile stations have become more computationally and bandwidth intensive. Both RISC microcontrollers (MCU) and DSPs have served these applications. While RISC processors are architected to enable efficient asynchronous control flow, DSPs are architected to perform well for synchronous, constant-rate data flow. Since both control and media processing are required in many embedded applications. DSPs and MCUs are typically used together either at the board level or in system-on-chip (SoC) integration. The RISC processors and DSPs unite as the perfect processing engine for a wide variety of multimedia applications and products, such as cellular telephones, digital cameras, portable networked audio/video devices.

Key base-station areas that require high-performance DSPs will include:

- Antenna Arrays with Adaptive Digital Beam-Forming (in BS- Base Station)
- Power Control (in both BS and MS – Base and Mobile Stations)
- Voice Processing (in BSC: Base-Station Control)
- Base Band Modem (in BTS: Base Transceiver Station)

Digital signal processors [11] are required both in BS and MS as we can observe in figures 1 and 2. Nowadays, there are some emerging technologies for example:- DSP– based Internet telephony which link between PSTN and packet network (VoIP gateway); the DSP advancements in processing power, smaller footprint, and reductions in power dissipation have extended number of channels carried on VoIP gateways.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 7, July 2014

DOI: 10.15662/ijareeie.2014.0307041

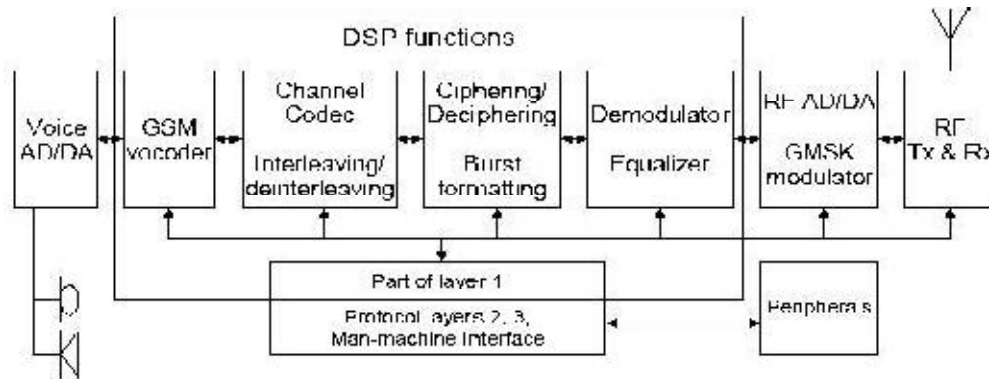


Figure 1: The GSM Mobile station

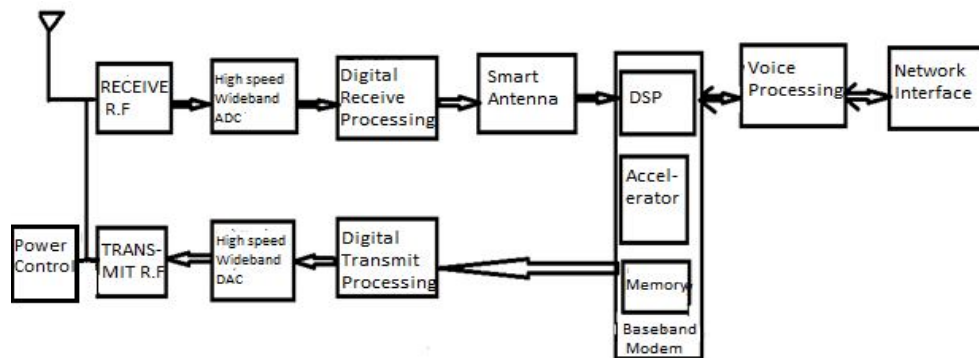


Figure 2. The Base Station

The requirements of 3G mobile systems are presented below:

Smart Antennas: Digital beam-forming algorithms are designed to target source locations in a noisy environment. Beam-forming in 3G systems may be integrated with the Rake receiver, where the signal is operated on to combat fading and multipath effects. For these algorithms, the TigerSHARC's rapid performance of floating-point computations makes it a good option.

Power Control: The computations required for power control are multiply-accumulate intensive. The computation is multiply-accumulate intensive. For such applications, ADSP-21065L SHARC is a processor of choice.

Voice Processing: DSPs are the traditional choice for speech processing within the cellular system. The ADSP-21mod980, with its 8 DSP cores, capable of 600 MMACS (Million MACs per second), is the ideal candidate for this portion of the signal chain.

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 7, July 2014

DOI: 10.15662/ijareeie.2014.0307041

Base Band Modem: The 3G standard is expected to be an essential factor that enables applications involving the transmission of wideband signals.

Rake, Channel-Encoding/Decoding Hardware-Software Tradeoffs: Because of the variability of the parameters, data-rates, and memory referencing, these functions are ideally suited to DSP for manipulation

Glueless Homogeneous and Heterogeneous Multiprocessing:

The TigerSHARC DSP provides several options for high-speed communication, including on-chip DMA (direct memory-access) and SDRAM support, along with dedicated user programmable link ports.

B. DSP Architectures for 3G Mobile Communications Systems:

The choice of a DSP to obtain the required computation speed is not a direct matter of specifying the highest clock speed Architecture and instruction sets greatly affect the speed of algorithm execution. “MIPS”(millions of instructions per second). Another aspect to consider is the class of DSP architecture employed.

Two recently introduced new classes to consider are: very long instruction word (VLIW) and static superscalar .VLIW tries to reduce cost and increase execution speed by reducing hardware complexity. The sequencing mechanism in VLIW depends on an instruction format. In VLIW, all operation latencies in a particular implementation are fully open to software. The TMS320C6x series from Texas Instruments is an example of VLIW architecture. Static superscalar architectures apply a consistent and functionally well-defined programming model, and the schedule is determined prior to run time. The TigerSHARC™ DSP from Analog Devices is an example of a static superscalar architecture.

The TigerSHARC Architecture

The TigerSHARC DSP [19] as shown in figure 3(a) permits multiple instructions per line and therefore reduces the overall cycle count required to perform 3G related functions such as channel decoding, de-spreading, and path searches. Since the acceleration capabilities reside in software rather than in static hardware blocks or coprocessors, TigerSHARC DSPs provide the flexibility, scalability, and interoperability needed in today’s highly competitive market. TigerSHARC DSP provides all the processing capacity to enable a single high speed 3G data channels.

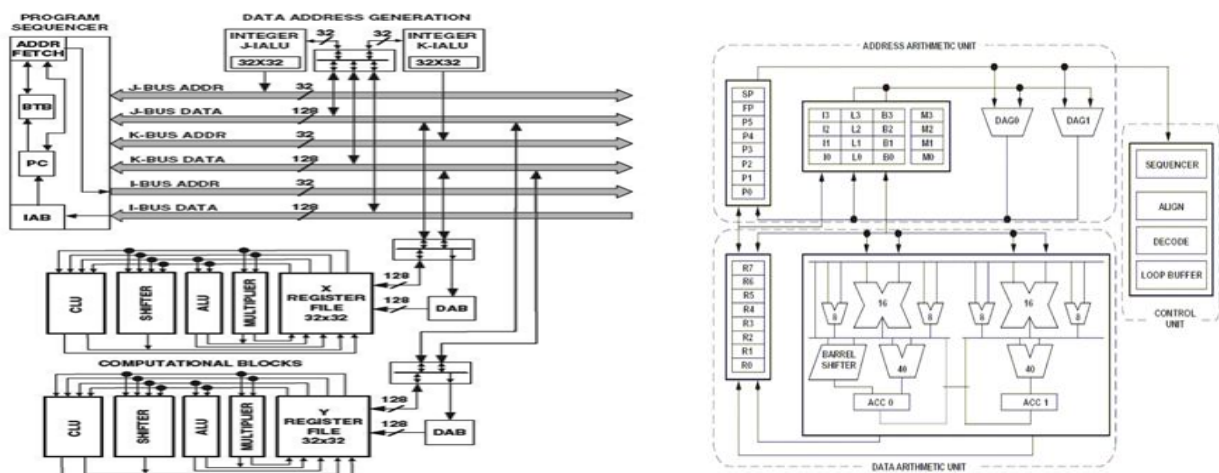


Figure 3 (a) TigerSHARC block diagram & 3(b) Blackfin processor core (Analog Devices)



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 7, July 2014

DOI: 10.15662/ijareeie.2014.0307041

The figure 3(b) illustrates the Blackfin architecture [20]. Blackfin takes the unique step of architecturally combining media processing attributes like dual MACs (multiply-accumulate engines, commonly used for high performance DSP applications) and classic RISC characteristics like a memory management capability that facilitates simplified, enterprise-level programming modes and styles. The device has DSP features not found on any RISC microcontroller and important microcontroller characteristics not typically on DSPs.

VI. PROGRAMMABLE DIGITAL SIGNAL PROCESSORS FOR 4G MOBILE

A. DSP processors for 4G

3G supports multimedia Internet-type services at better speeds and quality compared to 2G. The W-CDMA based air-interface has been designed to provide improved high-capacity coverage for medium bit rates (384kbit/s) and limited coverage at up to 2 Mbit/s (in indoor environments). Statistical multiplexing on the air also improves the efficiency of packet mode transmission. There are certain limitations [12] with 3G as follows:

- Higher data rate is difficult with CDMA due to excessive interference between services.
- It is difficult to provide a full range of multi-rate services,

4G is highly dynamic in terms of support for: the user's traffic, air interfaces and terminal types, radio environments, quality-of-service types and mobility patterns.

4G, puts more demand with adjustable and built-in intelligence. Thus a software system rather than a hard-and-fixed physical system is required. A 4G system [13] is required to provide a comprehensive and secure all-IP based mobile broadband solution to laptop, computer, wireless modems, smartphones, and other mobile devices. Facilities such as ultra-broadband Internet access, IP telephony, gaming facilities, may possibly be provided to manipulators. In modern DSP's, architecture can be extended by duplicating the processor cores. Enhanced DSP's utilizes SIMD operations, while multiple-issue DSP's may implement either VLIW or superscalar architectures

System on Chip (SoC) based architectures Mobile device processor architecture became simple with SOC designs. Real time responsiveness in mobile devices can be managed by using an improved DSP hybrid chip. dropping the voltage of the chip enables low power operation in mobile devices. Martin et al [14] proposed reconfigurable processor architecture for mobile phones. Dynamically Configurable System on Chip (CSoC) architecture has been enhanced for mobile communications. CSoC's are modified for a specific application. Its architecture consists of processor core, memory, ASIC cores, and on-chip reconfigurable hardware units. Most of the smart phones are single or dual-core SoC's. For mobile applications, faster dual-core CPU provides better performance than quad-core SoC's. Future SoC's for mobile will become more sophisticated providing better performance.

ARM Processors for Mobiles ARM based processors are the most widely used in modern Smart phones. ARM is a 32-bit instruction set architecture based on RISC architecture [15]. ARM processors are specially used in Smart phones because of its low power consumption and great performance. Different ARM architectures used in Smartphone are ARMv5 used in low-end devices, and ARMv6, ARMv7 used in high performance devices. ARMv7 has a hardware floating-point unit (FPU) providing improved speed. The 32-bit ARM architecture, such as ARMv7-A, is the most extensively used architecture in mobile devices. ARM architecture is the main hardware architecture for many of the operating systems of mobile devices such as iOS, Android, Windows Phone, Windows RT, Bada, Blackberry OS/Blackberry10, MeeGo, Firefox OS, Tizen, Ubuntu Touch, Sailfish and Igelles OS.

ARM Cortex Processors ARM Cortex processors cores are categorized into the following variants:

Cortex-A Processors (ARM Application Processors)

Cortex-R Processors (ARM Embedded Real-time Processors)



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 7, July 2014

DOI: 10.15662/ijareeie.2014.0307041

Cortex-M Processors (ARM Embedded Processors)

Qualcomm Snapdragon Processors Snapdragon is a family of mobile system on a chip (SoC) processor architecture provided by Qualcomm. In the year 2013, Qualcomm Snapdragon 800 processor with Krait 400 CPU cores providing 2.3 GHz clock speed outperformed all other processors in the mobile segment.

Nvidia Tegra Processors Tegra is a SoC series for mobile devices developed by Nvidia. It assimilates ARM architecture CPU, graphics processing unit (GPU), memory controllers, etc. on a single package. High performance and low power consumption for audio/ video applications is provided. It was found that Nvidia's Tegra 4 SoCs better than Qualcomm Snapdragon processor in terms of performance. Nvidia has launched next generation mobile processor, Tegra K1. It is a mobile processor with 192 graphics cores for mobile gaming applications. Nvidia K1 was launched with a support for two versions: traditional 32-bit "4+1" ARM cores like Tegra 4, and dual core 64-bit version. Tegra K1 is assumed to be more powerful than either the Xbox 360.

B. A Variable point FFT processor for 4G Standards:

IMT-Advanced varieties of the exceeding binary ethics are developing. In all suggestions for 4G, the CDMA spread spectrum wireless technology cast-off in 3G systems and IS-95 is replaced by OFDMA and former frequency-domain equalization. This is combined with MIMO (Multiple In Multiple Out), e.g., multiple antennas, dynamic channel allocation and channel independent scheduling. Orthogonal Frequency Division Multiple Access (OFDMA) is a cellular air interface used in 4G communications networks such as WiMAX.

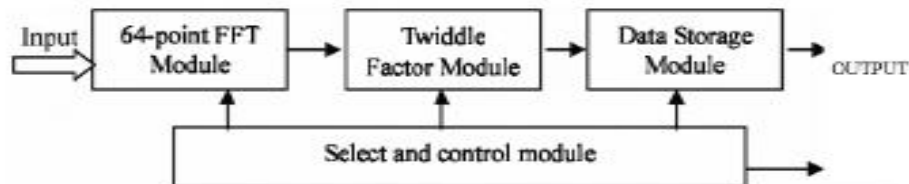


Figure 4: Block diagram of design of FFT Processor

OFDMA has several benefits ranging from increased flexibility to improved throughput and robustness [16]. By assigning sub-channels to specific subscribers, transmissions from several subscribers can occur simultaneously without interfering, thus minimizing an effect known as Multiple Access Interference (MAI). Furthermore, sub channelization enables the concentration of transmit power over a reduced number of subcarriers.

Another technique to cope with multipath disappearing is spaced carrier OFDMA [17]. It is OFDMA with code division multiplexing (CDM) such that the robustness increases. A variable point FFT processor [18] may be designed using FPGA in which OFDMA Technology is applied. The FFT processor uses Verilog HDL language to describe the circuit, Quartus II 7.2 software to build the model, and ModelSim SE 6.2b software is used to verify the timing function. This design completes the main computing modules in the OFDMA system, when applied to real-time signal processing system,

VII. CONCLUSION

This paper discusses various processor architectures for 3G and 4G wireless communication. Figures 1 and 2 show the GSM mobile station and base station requirements. Many solutions for base station or mobile station have been implemented over the years, and each solution required a combination of two components, ASICs, and DSPs.



International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 7, July 2014

DOI: 10.15662/ijareeie.2014.0307041

TigerSHARC DSP provides all the processing capacity to enable a single high speed 3G data channel. TMS320C6x series tries to reduce cost and increase execution speed by reducing hardware complexity. Figure 3 shows the TigerSHARC and Blackfin architectures. We have discussed advanced functionality in mobile devices from the major manufacturers, and with fourth generation (4G) wireless broadband. For 4G various DSP processors available are System on Chip (SoC) based architectures, ARMv-5, ARMv-6, ARMv-7, Cortex-A, Cortex-R, Cortex-M Processors, Qualcomm Snapdragon Processors, Nvidia Tegra Processors and Variable point FFT processor. Figure 4 shows the block diagram of FFT Processor.

The computational power of DSP architectures has greatly improved due to advancements in chip fabrication. As shown in Table 1 below, the same DSP chip was providing approximately 5 GIPS (Giga Instructions per Second) in 2000, in contrast to 5 MIPS in 1980 and it has grown to 50 GIPS in the year 2010. Considering other factors also, the advancements in DSP integration is quite significant. Mobile high definition video, cost effective and power efficient support for these applications will be required in the very near future.

| Parameter | 1980 | 1990 | 2000 | 2010 |
|--------------------------|-------|--------|-----------|------------|
| Die Size (mm) | 50 | 50 | 50 | 5 |
| Technology (micrometers) | 3 | 0.8 | 0.1 | 0.02 |
| MIPS | 5 | 40 | 5000 | 50000 |
| MHz | 20 | 80 | 1000 | 10000 |
| RAM (bytes) | 256 | 2000 | 32000 | 1000000 |
| Price (dollars) | 150 | 15 | 5 | 0.15 |
| Power (mW/MIPS) | 250 | 12.5 | 0.1 | 0.001 |
| Transistors | 50000 | 500000 | 5 million | 50 million |
| Wafer Size (inches) | 3 | 6 | 12 | 12 |

TABLE 1: DSP INTEGRATION OVER THE YEARS
Source: Past and Projected Evolution of DSP (Gene 2000)

VIII. ACKNOWLEDGMENT

We would like to acknowledge the experts of DSP processors whose sources we have used and whose analysis we appreciate: Texas instruments, Qi Bi, Byoung-Woon Kim, Sorin Zoican and R. Ramakrishnan, etc.

IX. FUTURE TRENDS

A dominant embedded and mobile devices operating system has still to emerge, for the new generation of mobile devices. Future mobile processors will incorporate more parallelism in superscalar designs. VLIW and SIMD architectures will become more popular, because they allow to reduce the frequency and voltage of the processor chips without losing performance. In the future all these trends will lead to more efficient and powerful embedded and mobile devices. The big challenge is to still keep the power usage at a low level. One possibility is to embed many small processors in office and city environment, which can assist the mobile devices and reduce their power needs.

REFERENCES

- [1] Qi Bi, George I. Zysman, and Hank Menkes, Lucent Technologies, "Wireless Mobile Communications at the Start of the 21st Century", IEEE Communication Magazine, 2001.



ISSN (Print) : 2320 – 3765
ISSN (Online): 2278 – 8875

International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering

(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 7, July 2014

DOI: 10.15662/ijareeie.2014.0307041

- [2] “DSP 1618 Digital Signal Processor”, AT&T Data Sheet, Feb. 1994.
- [3] H Hendrix, “Viterbi decoding techniques in the TMS320C54x family”, TI Application Rep. June 1996.
- [4] “TMS320C62x/C67x CPU and instruction set Texas Instruments, reference guide”, SPRU198C, March 1998.
- [5] M. Levy. (Apr. 1998). EDN’s 1998 DSP-architecture directory.[Online].
- [6] Byoung-Woon Kim, Jin-Hyuk Yang, Chan-Soo Hwang, Young-Su Kwon, Keun-Moo Lee, In-Hyoung Kim, Young-Hoon Lee, Chong-Min Kyung, “MDSP-II: A 16-Bit DSP with Mobile Communication Accelerator”, IEEE Journal of Solid-State Circuits, Vol. 34, no. 3, March 1999.
- [7] Alan Gatherer, Trudy Stetzler, Mike McMahan, and Edgar Auslander, Texas Instruments, “DSP Based Architectures for Mobile Communications: Past, Present and Future”, IEEE Communications Magazine, pp. 84-90, January 2000.
- [8] <http://www.ti.com/sc/docs/products/dsp/c6000/index.htm>.
- [9] <http://www.analog.com/industry/dsp>.
- [10] <http://www.starcore-dsp.com/>
- [11] Sorin ZOICAN, Politehnica, “The Role of Programmable Digital Signal Processors (DSP) for 3G Mobile Communication Systems” Volume 49, Number 3, 2008 ACTA TECHNICA NAPOCENSIS, Electronics and Telecommunications.
- [12] B. G. Evans, K. Baughan, “Visions of 4G”, Electronics & Communication Engineering Journal, December 2000.
- [13] Mahendra Pratap Singh, Manoj Kumar Jain, “Evolution of Processor Architecture in Mobile Phones”, International Journal of Computer Applications (0975 – 8887) Volume 90 – No 4, March 2014.
- [14] Martin Vorbach, Gurgun Becker, “Reconfigurable processor architectures for mobile phones”, Parallel and Distributed Processing Symposium, 2003. Proceedings. International.
- [15] Leonid Ryzhyk: “The ARM Architecture”.
- [16] L Liu, “Uplink access scheme for LTE-advanced,” IEICE Trans. Commun., vol. E92-B, no. 5, May 2009.
- [17] P. Dharmawansa, N. Rajatheva, and H. Minn, “An exact error probability analysis of OFDM systems with frequency offset”, IEEE Trans. Commun., vol. 57, pp. 26-31, Jan. 2009.
- [18] R. Ramakrishnan, Vankayala Chethan Prakash, R. S. Raghav, Logesh R, Jaya Cyril Britto, “Design of a Variable point FFT processor for 4G Standards”, International Journal of Advanced Research in Computer and Communication Engineering, Vol. 3, Issue 3, March 2014.
- [19] Analog Devices, “ADSP-TS201 TigerSHARC Processor Hardware Reference”, 2005
- [20] Analog Devices “ADSP-BF53x Blackfin Processor Hardware Reference”, 2007

BIOGRAPHY



Vinni Sharma received the M.Tech degree in Instrumentation and Control Engineering from the CSVTU University in 2007. She is currently working as an Associate Professor from the year 2004 in the Department of Electronics and Telecommunications Engineering, Bhilai Institute of Technology, Durg (C.G). Her research interest includes signal processing architectures and embedded systems for wireless communications



Tanuja Kashyap received the M.E. degree in Electronics and Communications Engineering from the CSVTU University in 2009. She is currently working as an Associate Professor in the Department of Electronics and Telecommunications Engineering, Bhilai Institute of Technology, Durg (C.G). Her research interest includes Signal Processing and Digital Image Processing.